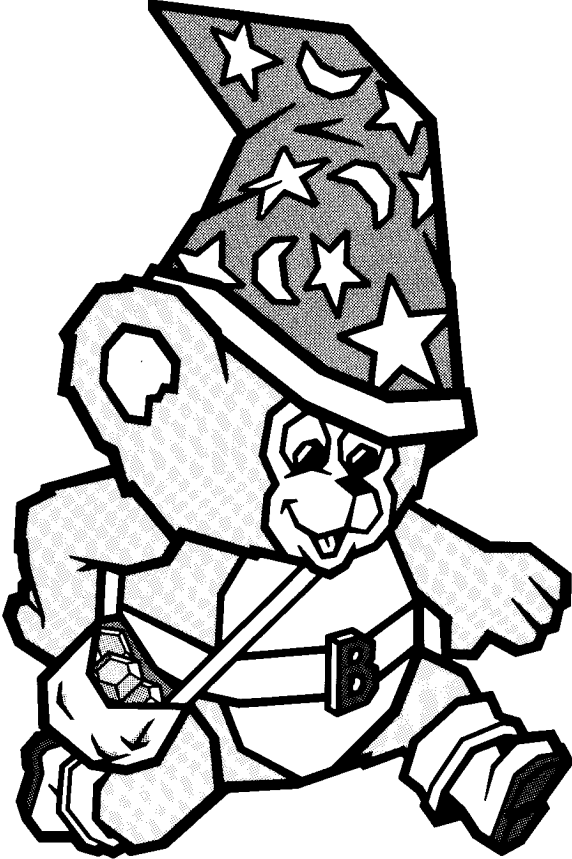
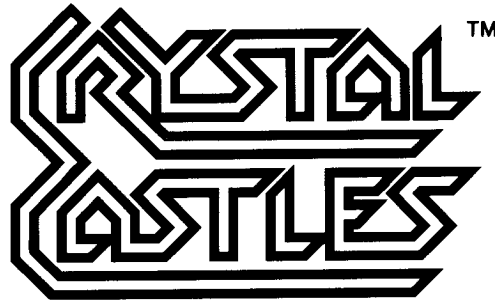


NOTE

Remove this staple to separate the schematic diagrams from the Troubleshooting Guide.



Schematic Package Supplement to



Operators Manual

Includes
Troubleshooting Guide

7M



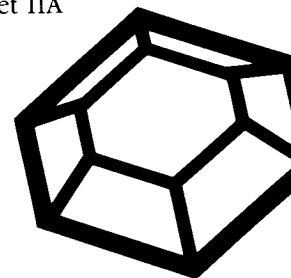
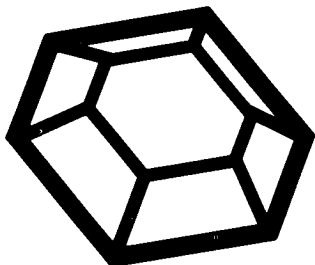
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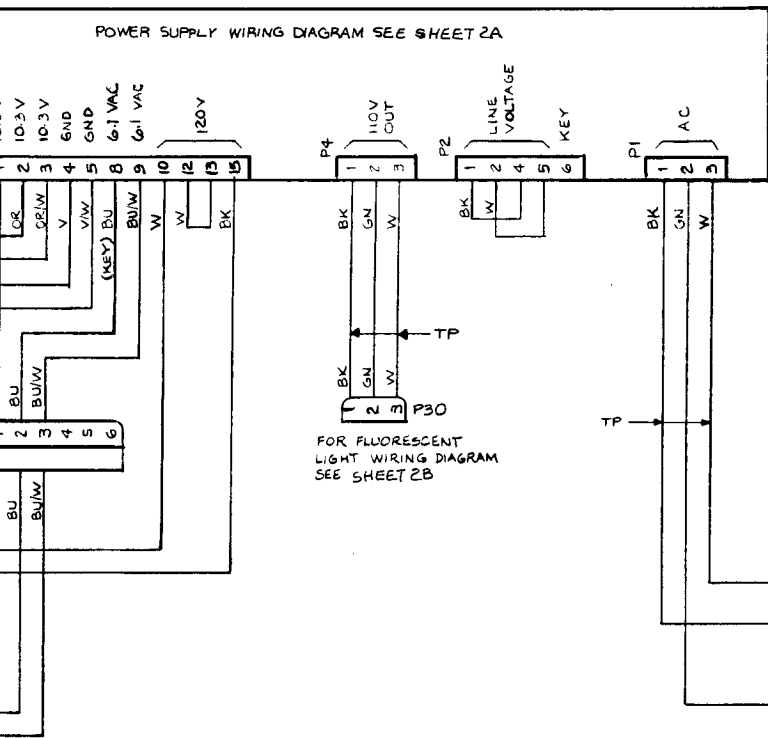
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Crystal Castles Coin Door Wiring Diagram (A037542-01 E), Utility Panel Wiring Diagram (A038004-01 F), Fluorescent Light Wiring Diagram (035833-01 A)	Sheet 2B
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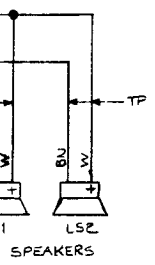
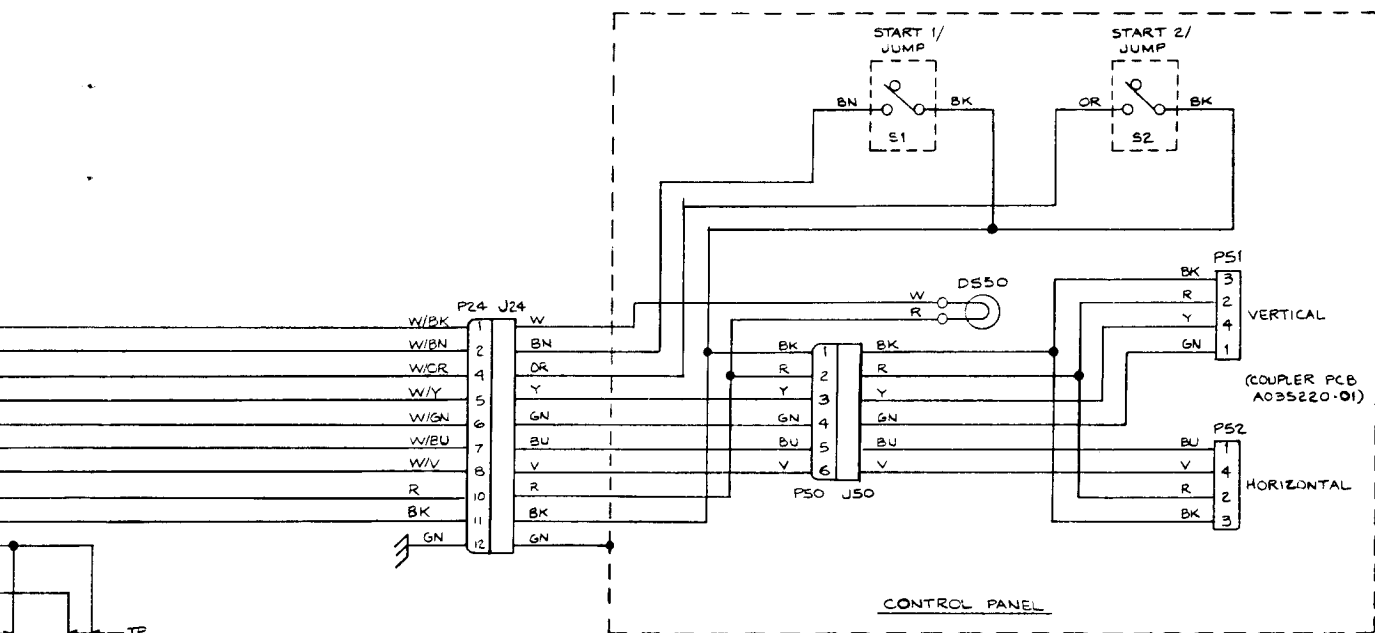
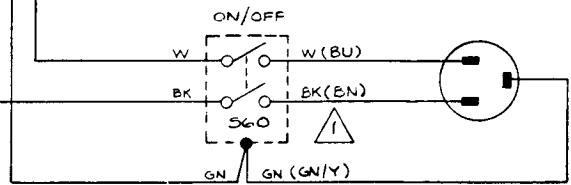
NOTE

A Crystal Castles Troubleshooting Guide is included as part of this Schematic Package Supplement. The Troubleshooting Guide contains Atari CAT Box troubleshooting procedures.





NOTES
 ▲ ALTERNATE WIRE COLORS ARE IN PARENTHESES ().



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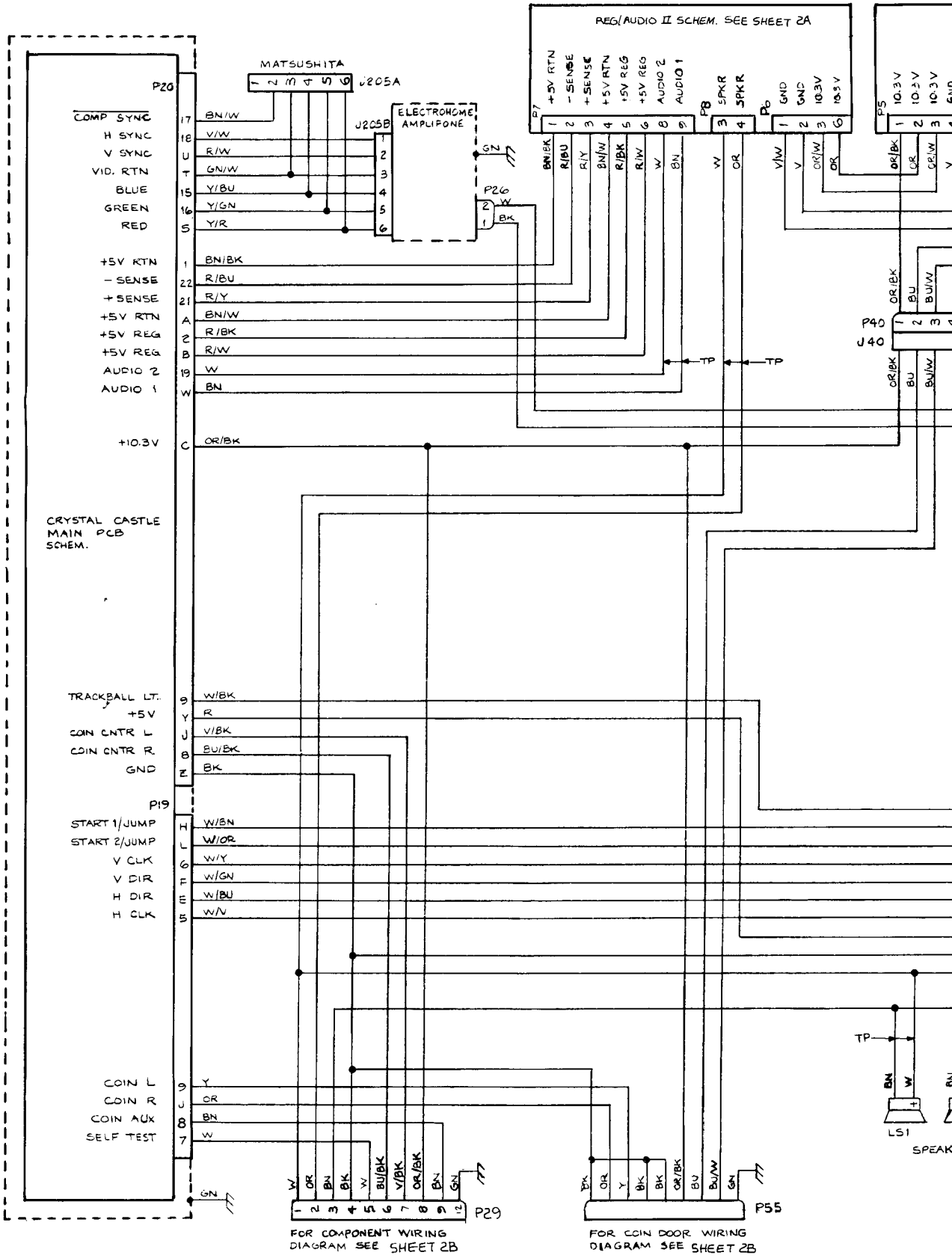
Crystal Castles Main Wiring Diagram

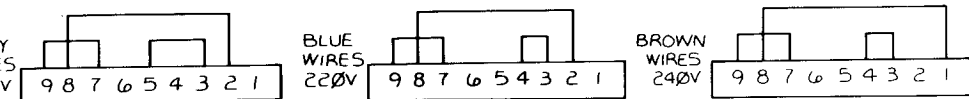


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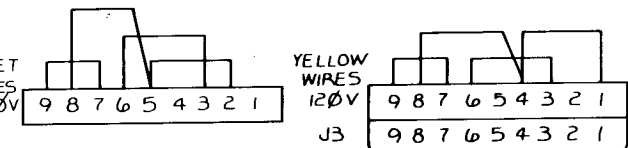
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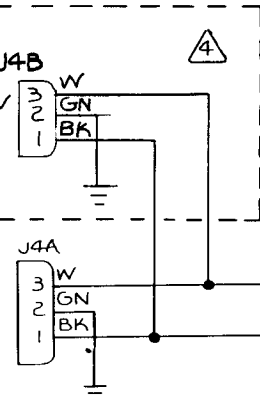
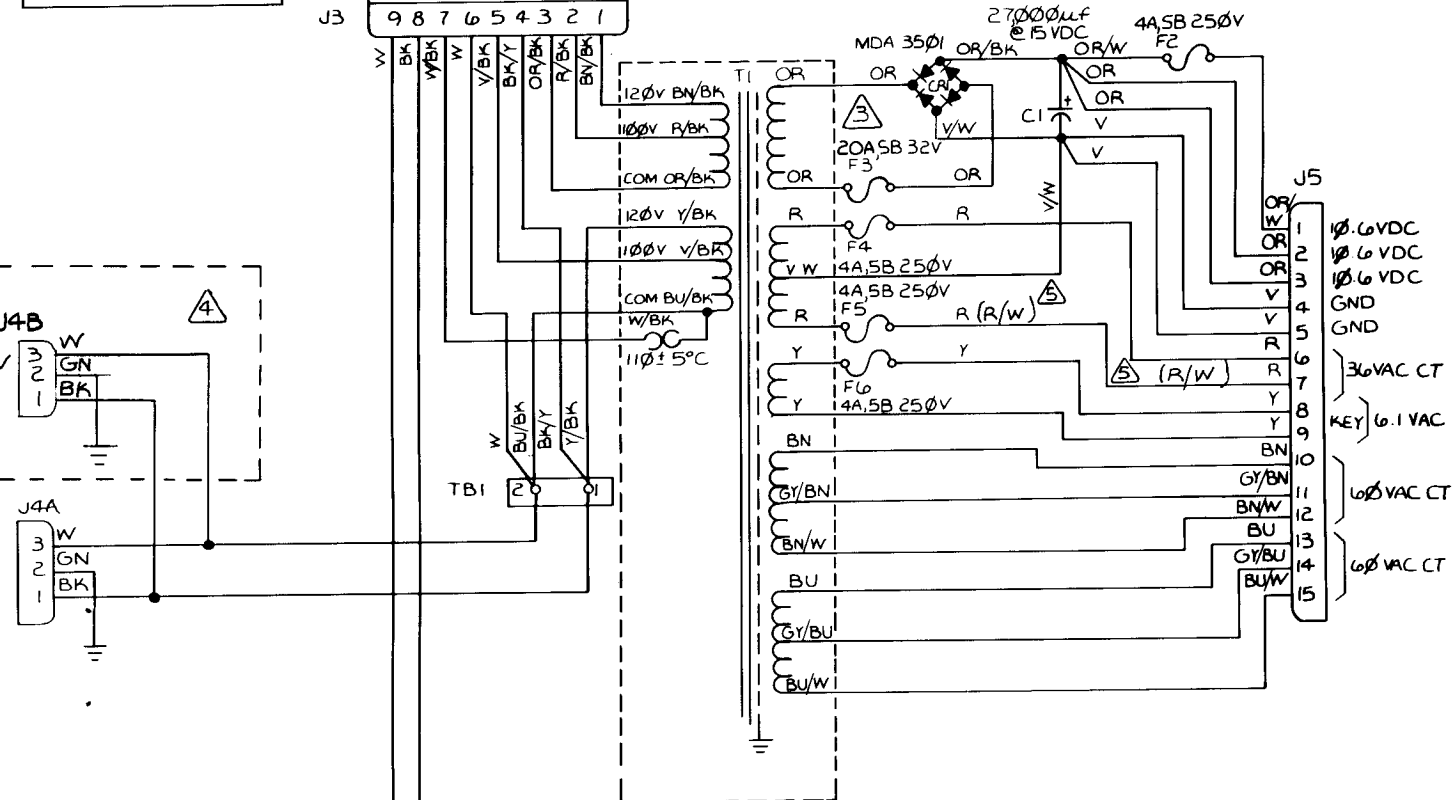




VOLTAGE SELECTION BLOCKS

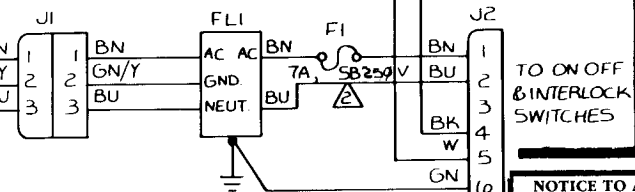


Color Raster Power Supply Wiring Diagram



NOTES:

- ⚠ USE 25 AMP SB 32 FUSE AT F3 FOR -04, -05, & -06 VERSION OF A037671-XX POWER SUPPLY.
- ⚠ J4B USED IN -07 THROUGH -12 VERSION OF A037671-XX POWER SUPPLY ASSY.
- ⚠ ALTERNATE WIRE COLOR IS IN PARENTHESES ().
- ⚠ POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).
- ⚠ USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY)



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Crystal Castles Regulator/Audio II PCB and Power Supply Diagrams

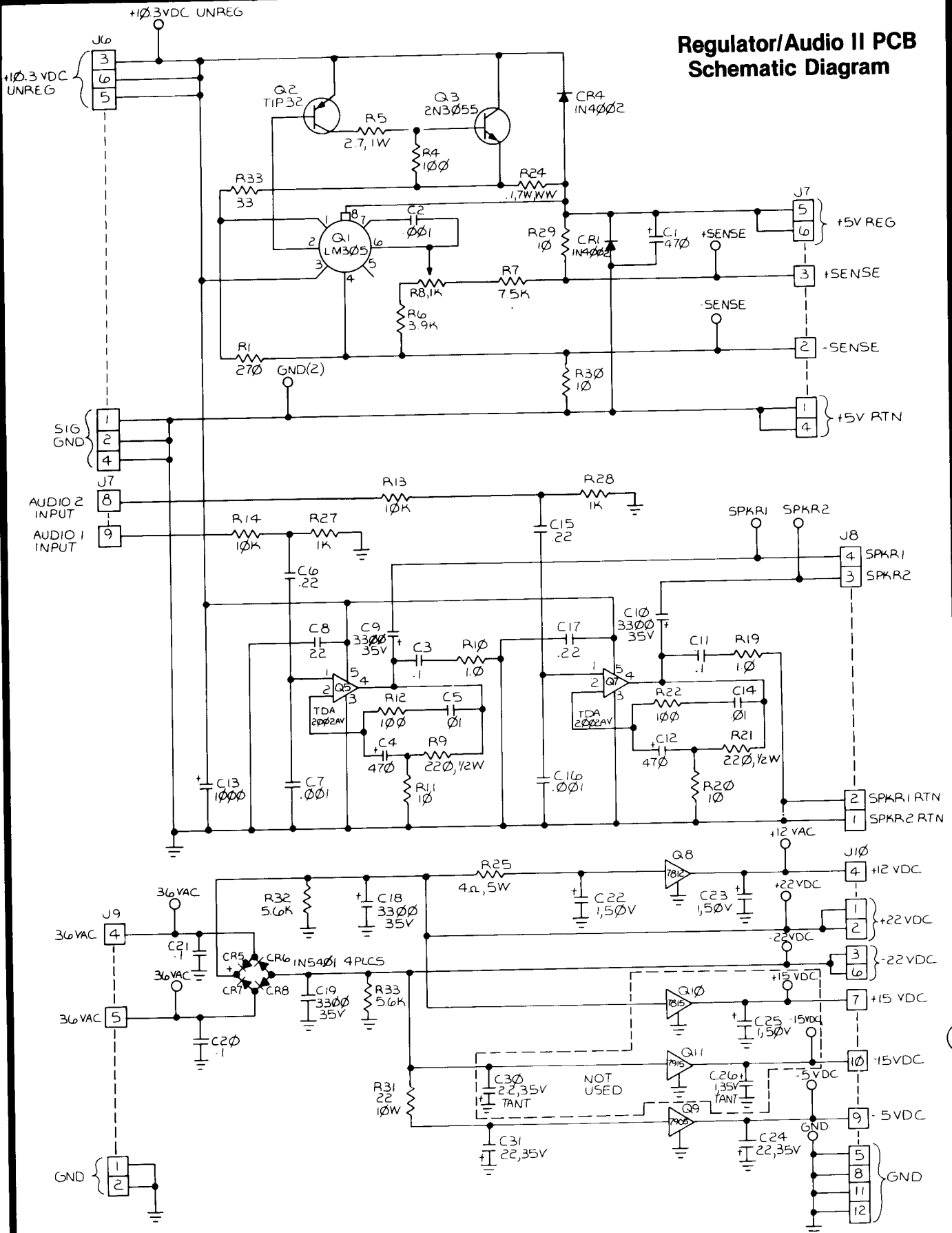


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Regulator/Audio II PCB Schematic Diagram



GRAY WIRES 200V 9

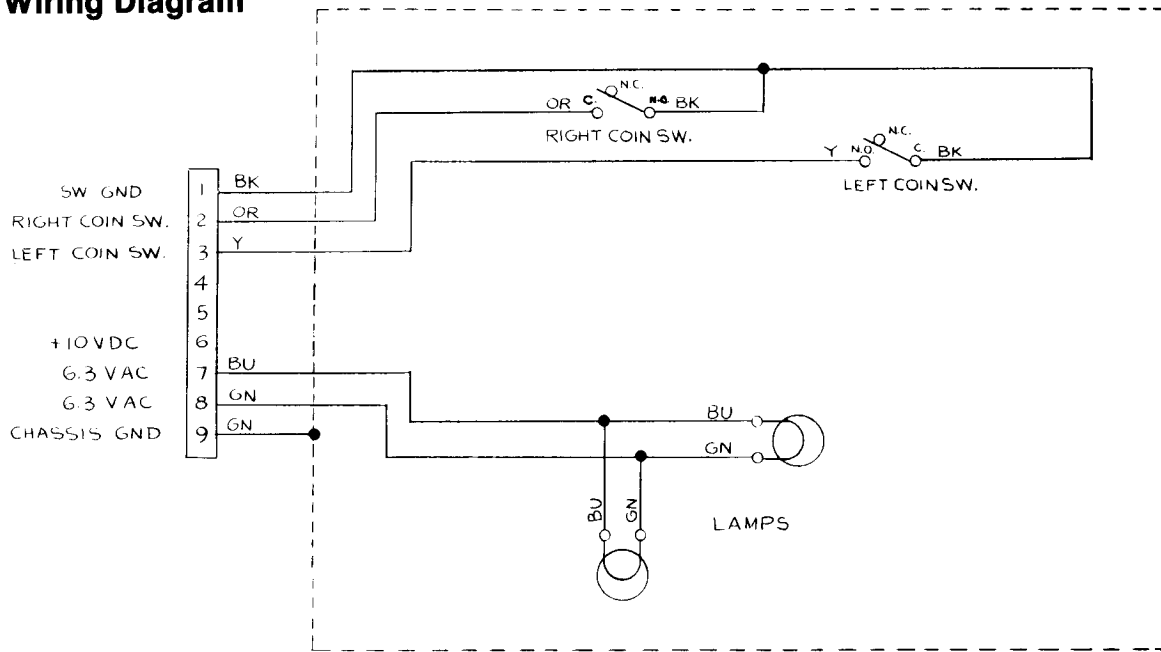
VIOLET WIRES 100V 9

J4B
120V AC OUT 3 2 1

J4A
120V AC OUT 3 2 1

J10
BN 1
GN/Y 2
BU 3
PLUG

Coin Door Wiring Diagram



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Crystal Castles Game Interfaces

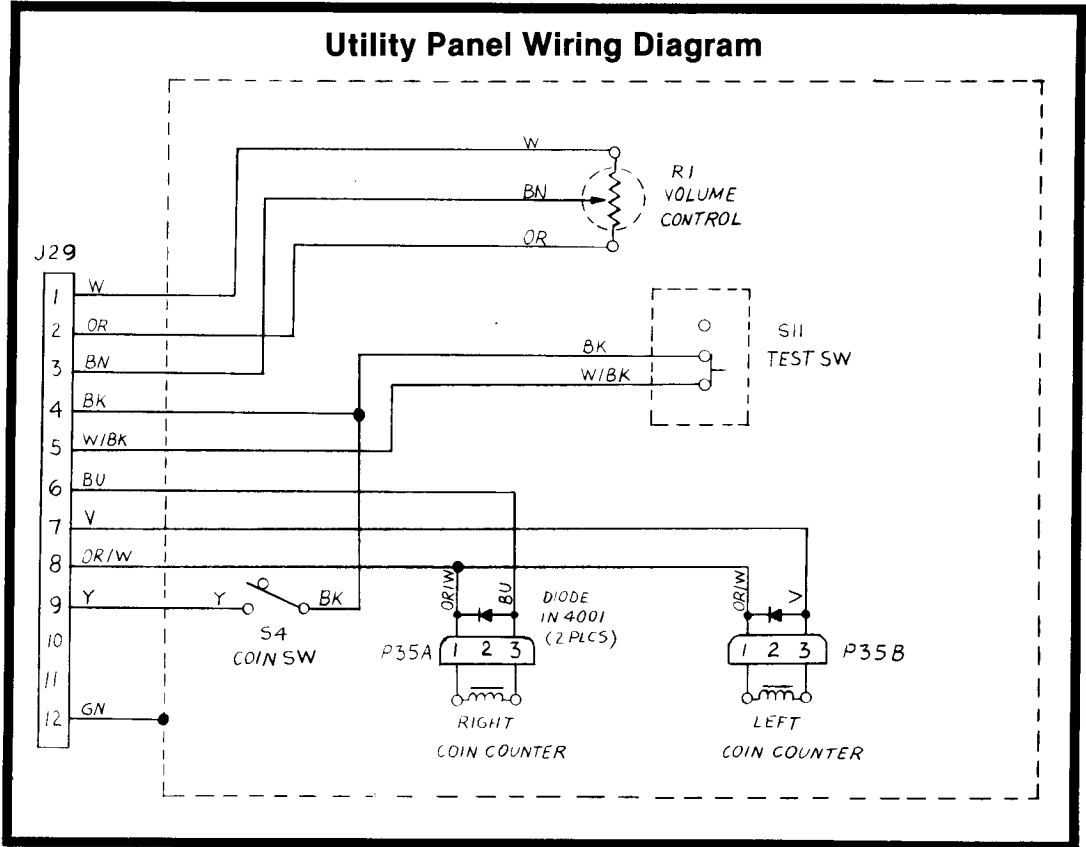


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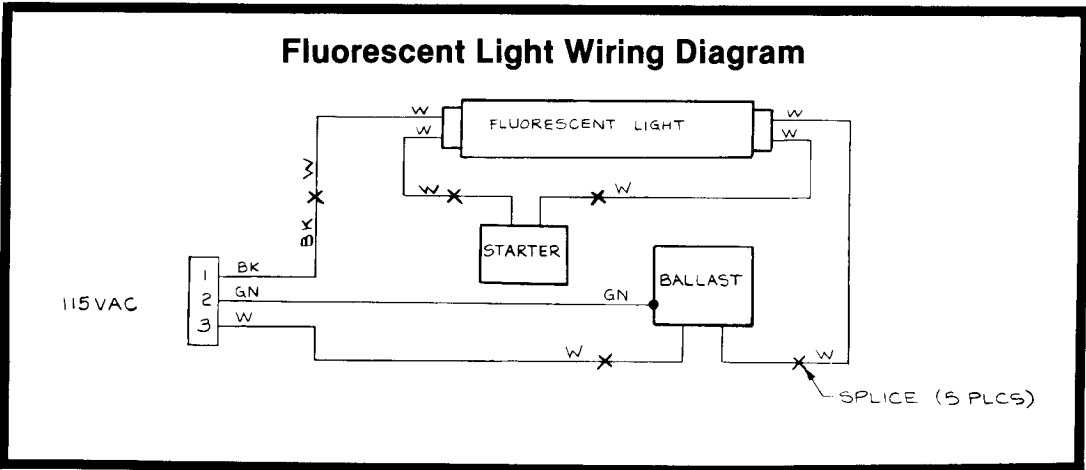
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Utility Panel Wiring Diagram



Fluorescent Light Wiring Diagram



	FUNCTION
X D D D D	X COORDINATE Y COORDINATE BIT MODE WORKING RAM (DRAM) SCREEN RAM WORKING RAM (STATIC) MOTION OBJECT BUF 2
D D D D	MOTION OBJECT BUF1 MOTION OBJECT PICTURE MOTION OBJECT VERTICAL MOTION OBJECT PRIORITY MOTION OBJECT HORIZONTAL
D D	NOVRAM TRAK-BALL INO COIN R COIN L COIN AUX SLAM SELF TEST SPARE JMP 1 JMP 2
D D D	CI/O 0 CI/O 1 OPTION SW SPARE SPARE COCKTAIL RECALL
D D D D D D D D D D D D D	HOR SCROLL CNTR LOAD VERT SCROLL CNTR LOAD INTERRUPT ACKNOWLEDGE WDOG OUT 0 TRAK-BALL LIGHT STORE LOW STORE HIGH SPARE COIN CNTR R COIN CNTR L BANK0-BANK 1 OUT 1 AX AY XINC YINC PLAYER 2 SIRE BOTHRAM BUF1/BUF2 COLORAM PROGRAM ROM

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Crystal Castles Memory Map

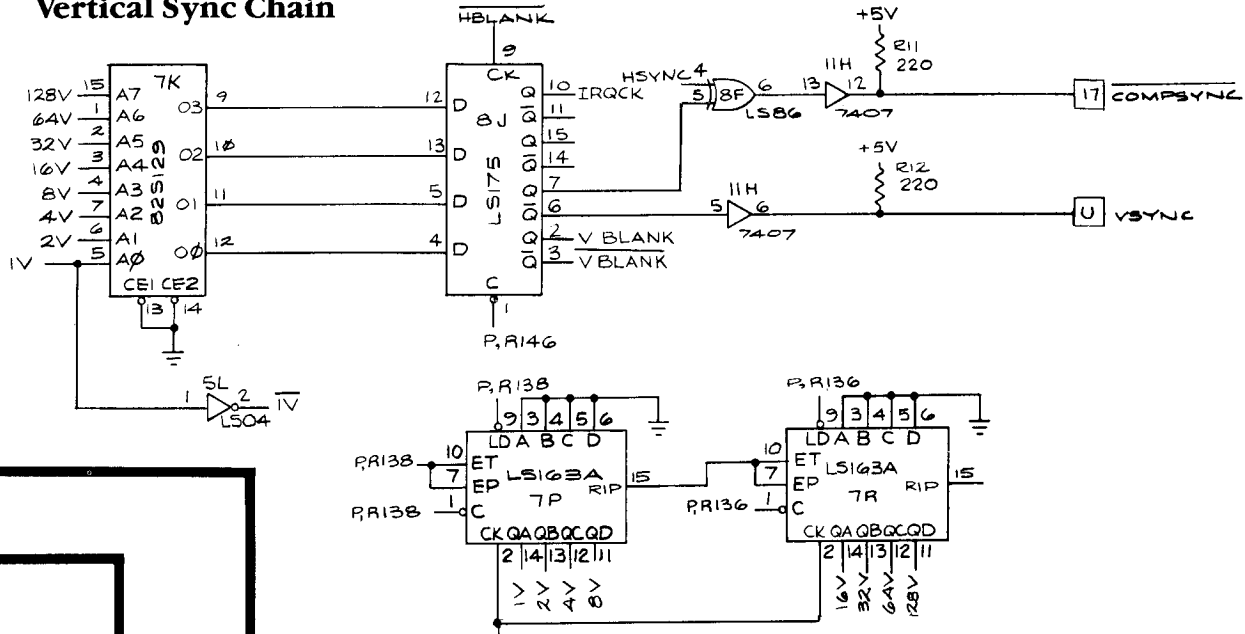


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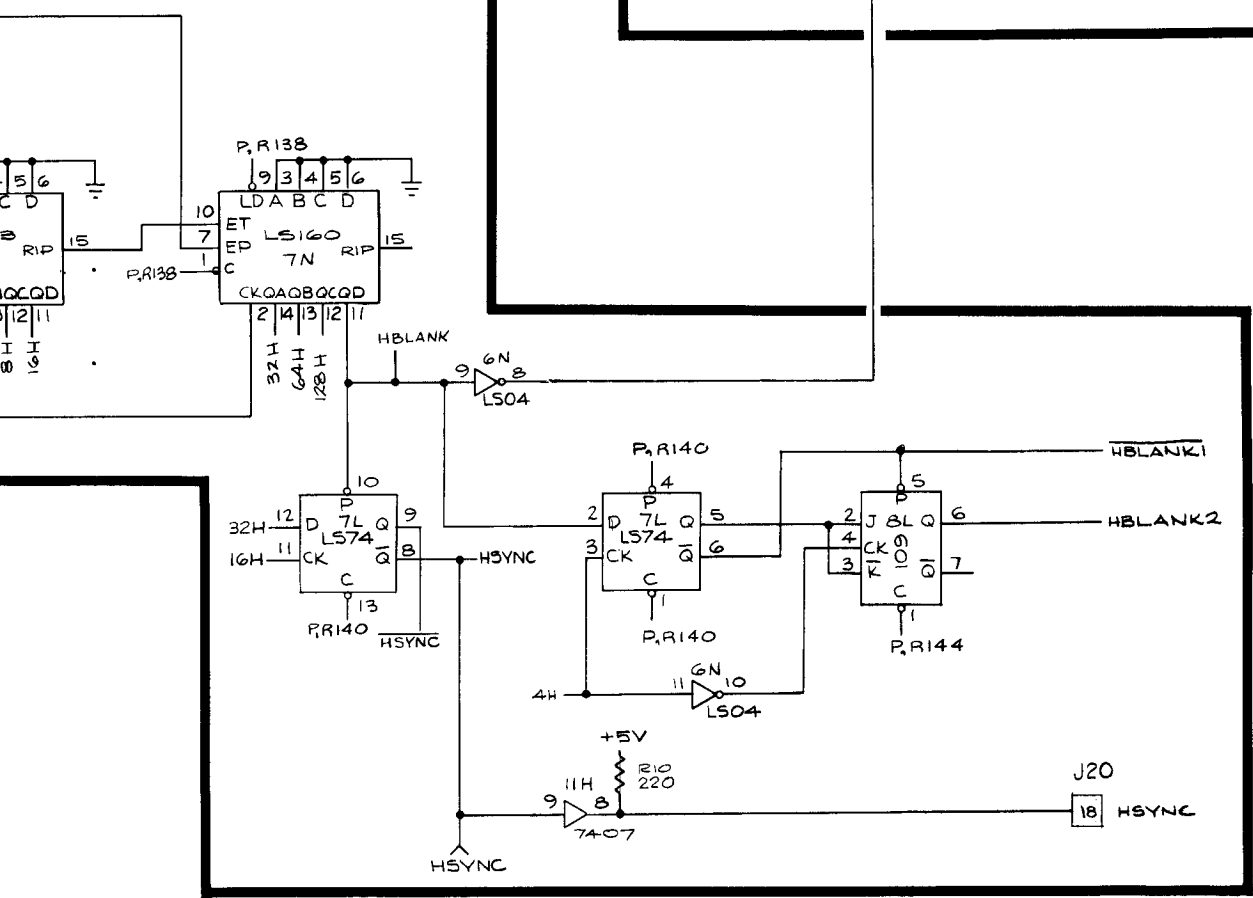
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Vertical Sync Chain



Horizontal Sync Chain



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Crystal Castles PCB Schematic Diagram






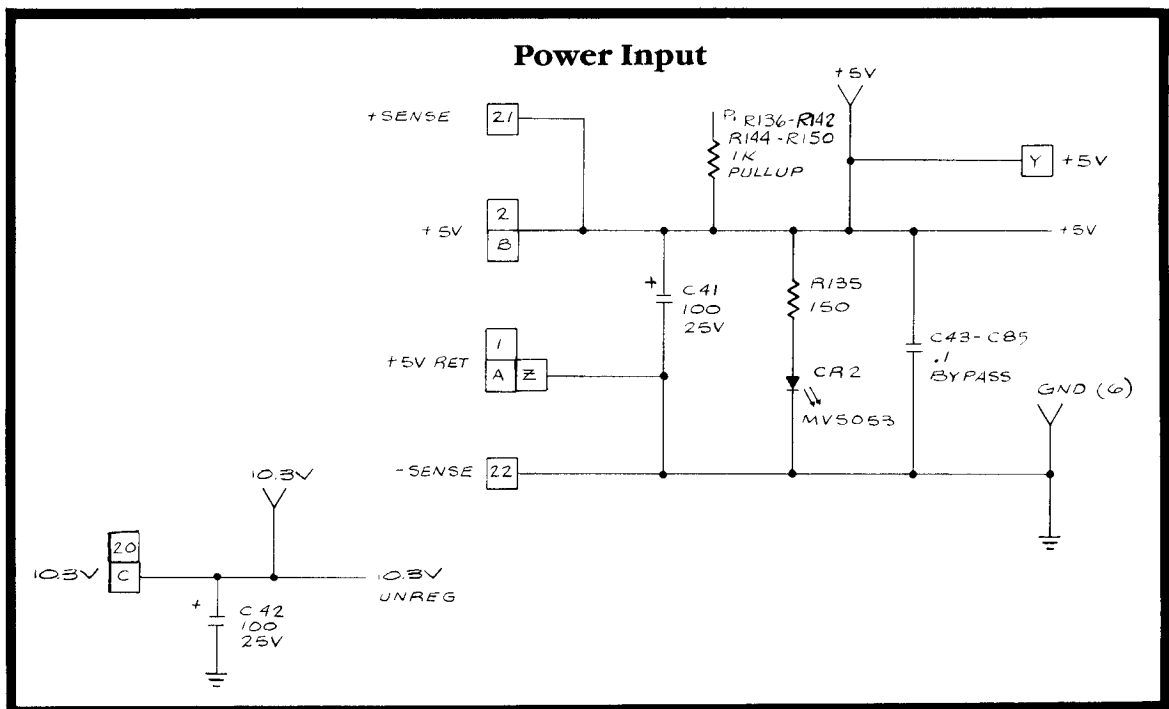
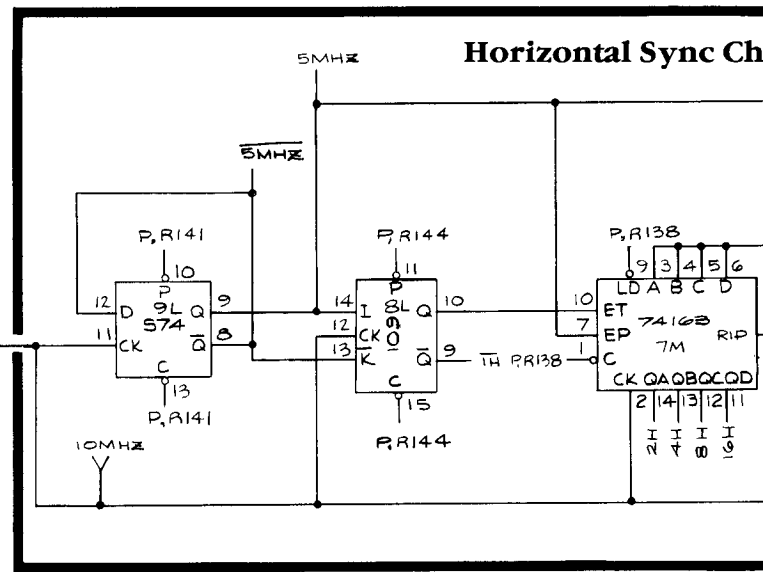
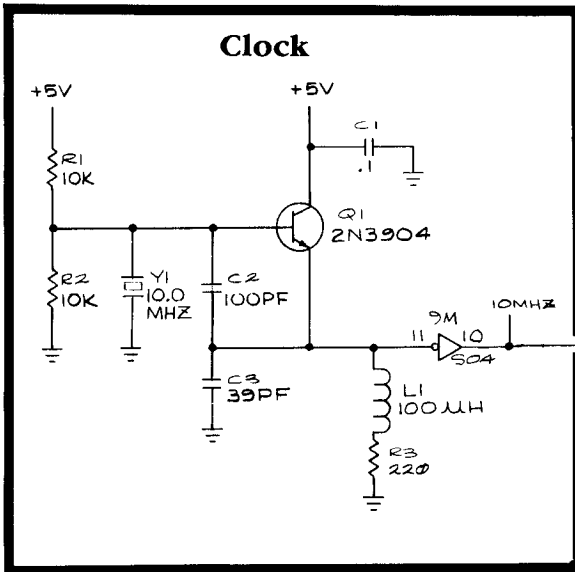
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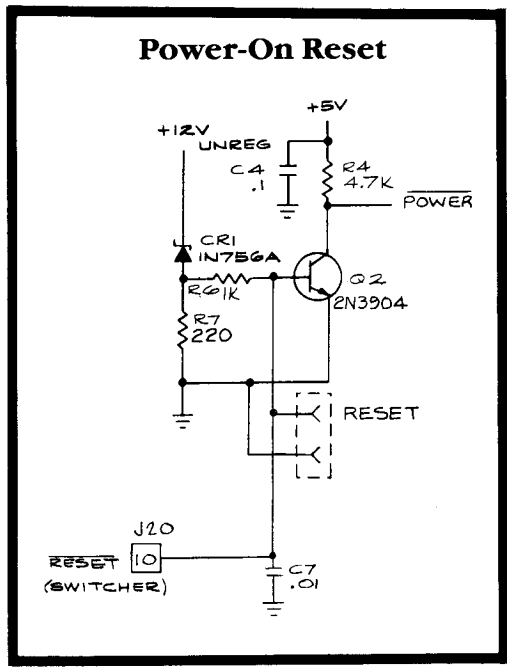
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Connector Symbols

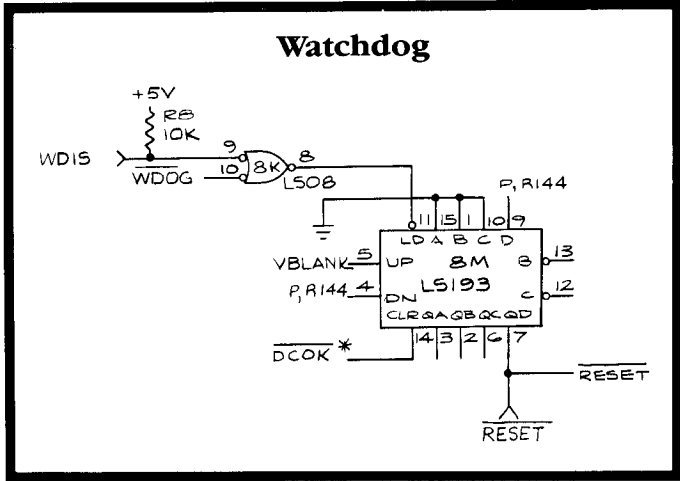
1.  DENOTES J20 CONNECTOR.
2.  DENOTES J19 CONNECTOR.
3.  DENOTES TEST CONNECTOR.



Power-On Reset



Watchdog



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Crystal Castles PCB Schematic Diagram

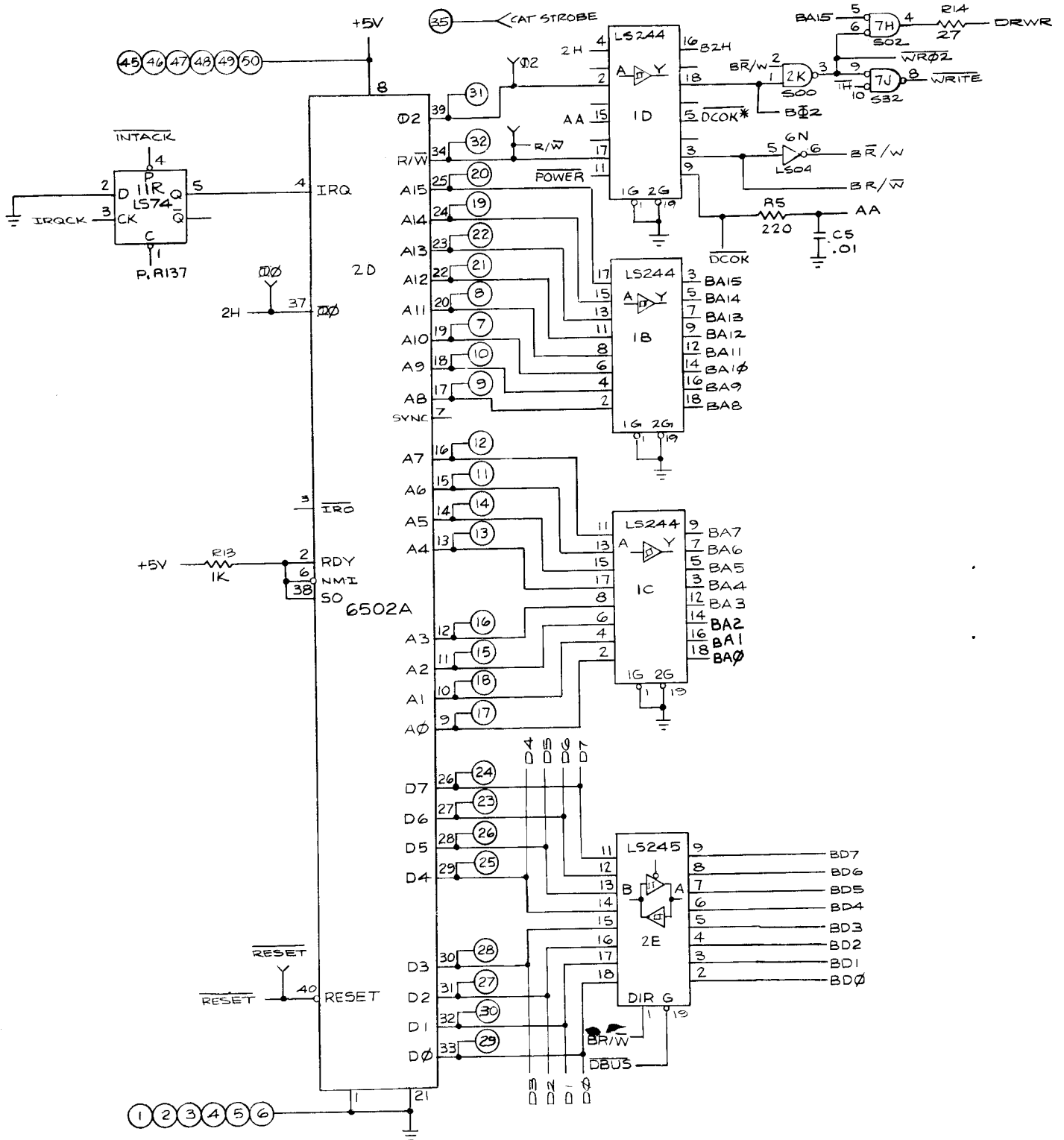


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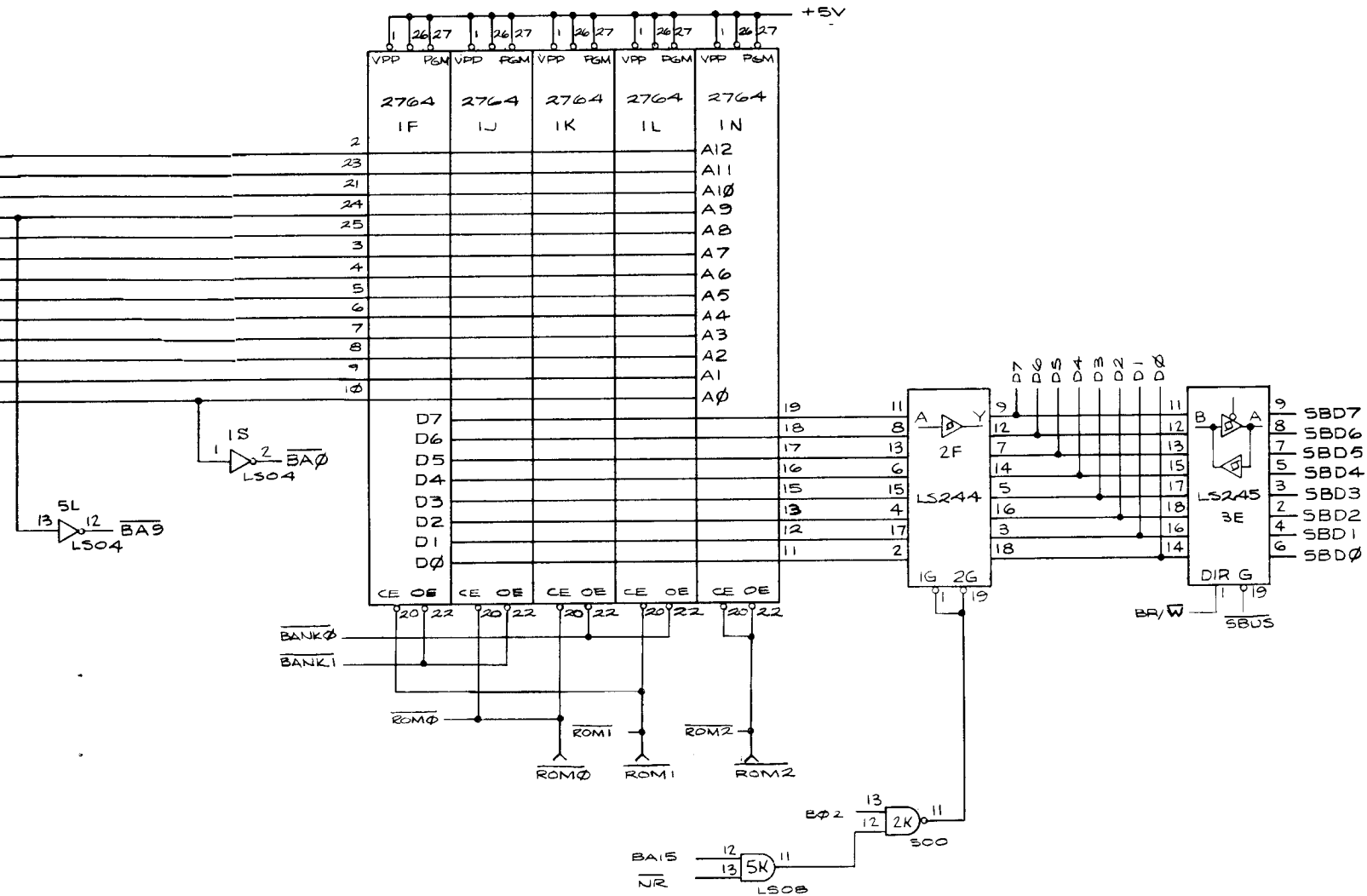
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Microprocessor



Program Memory



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Crystal Castles PCB Schematic Diagram

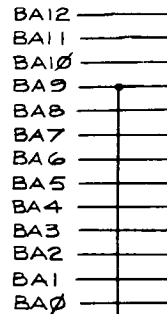
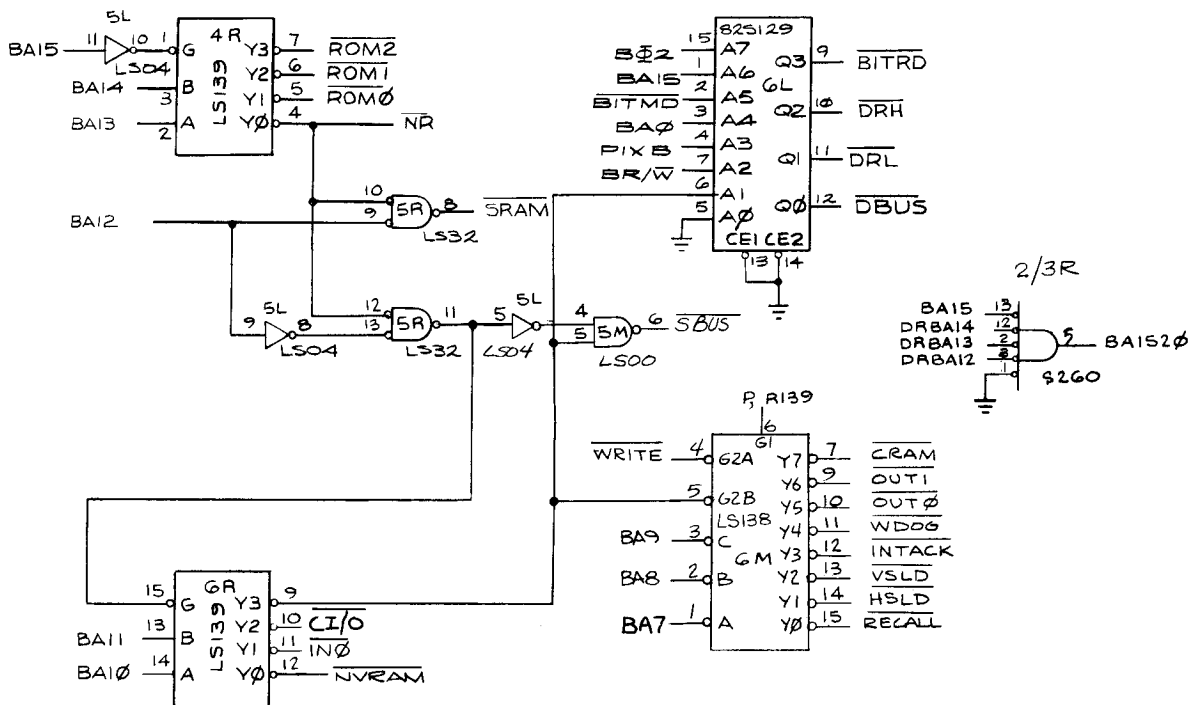
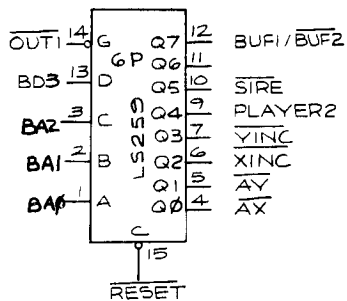
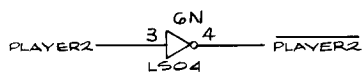


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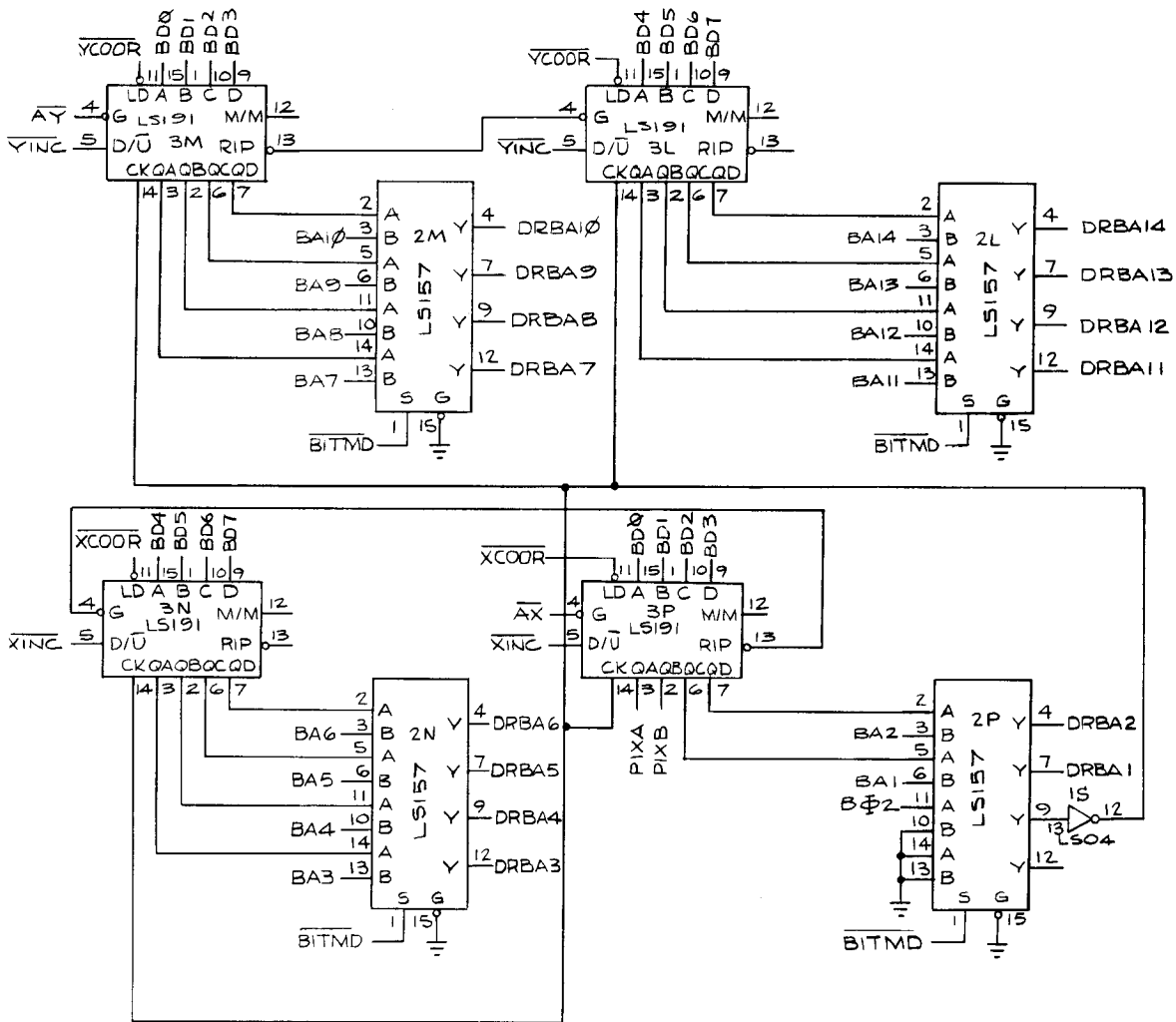
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Address Decoders



13

Auto Increment



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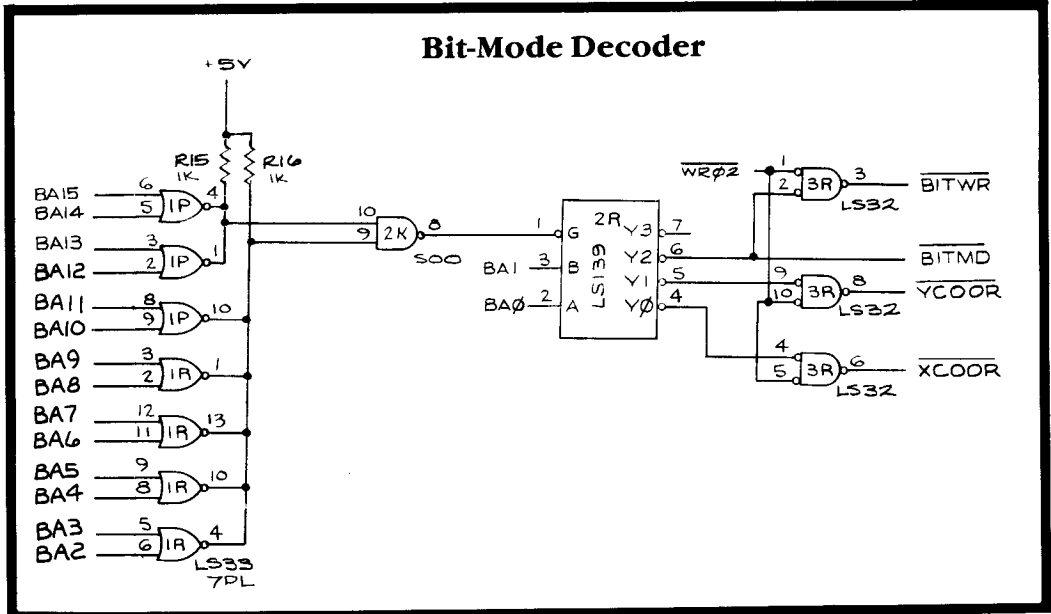


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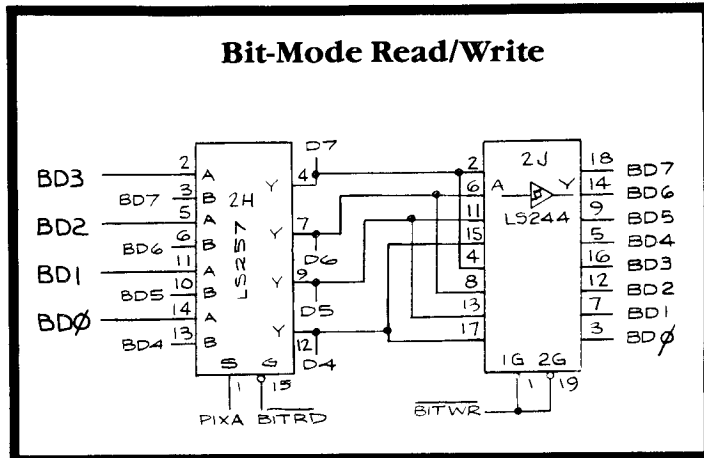
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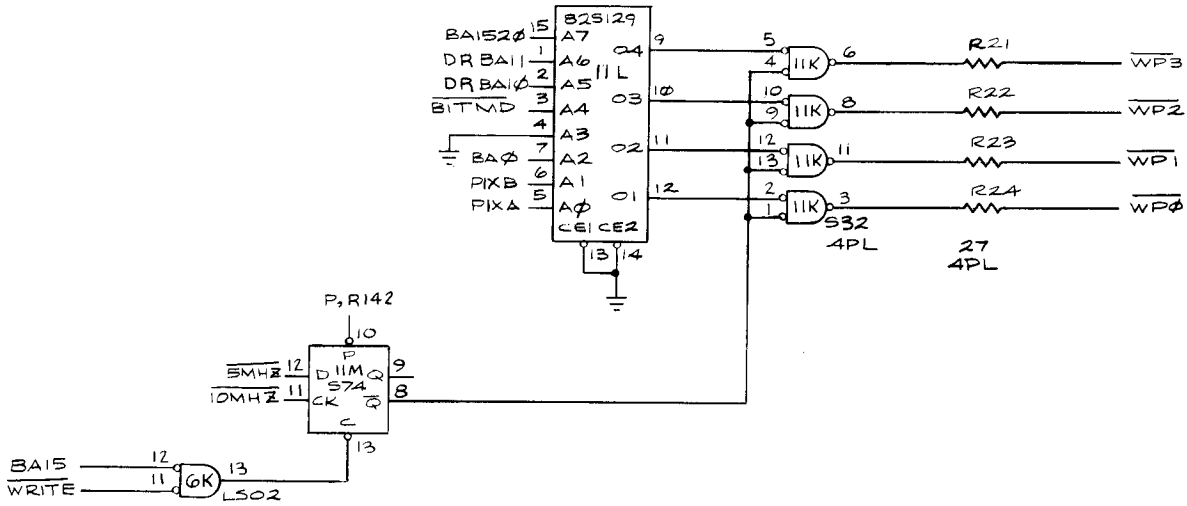
Bit-Mode Decoder



Bit-Mode Read/Write



Dynamic RAM Write Protection



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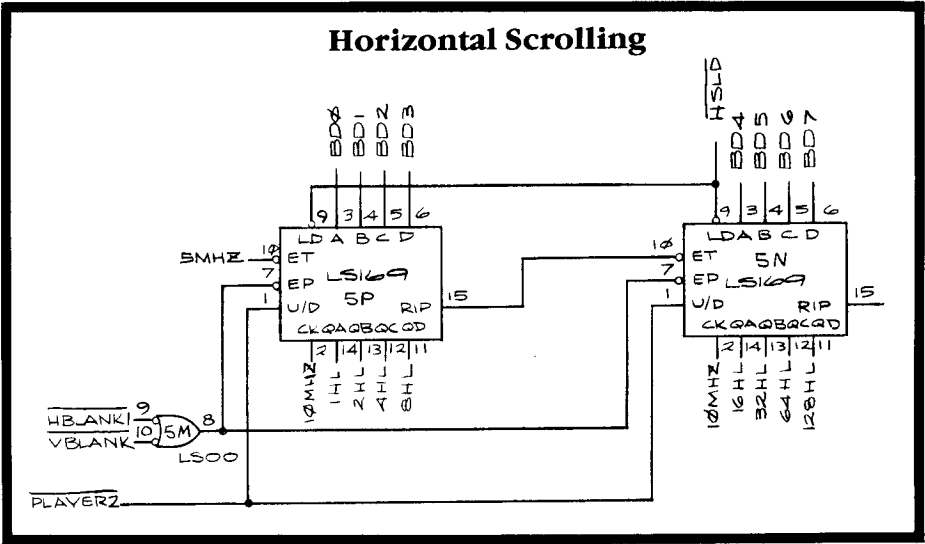


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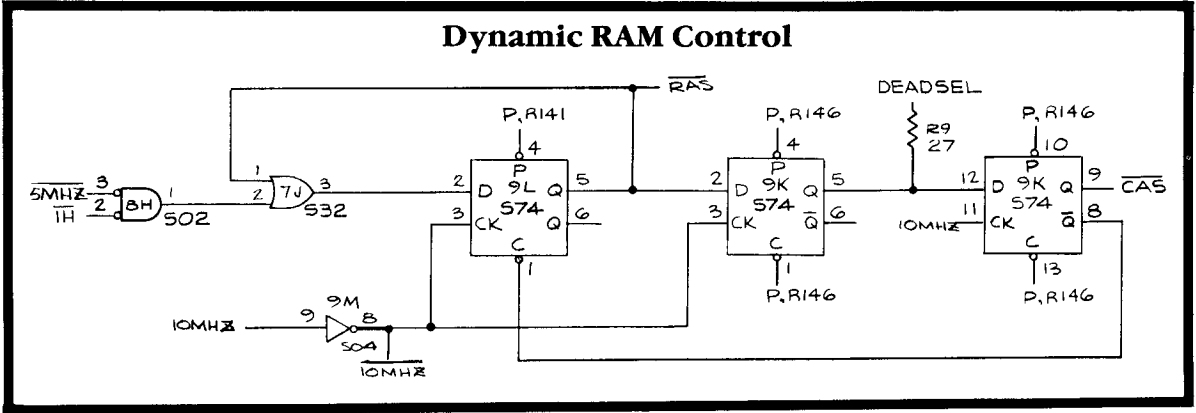
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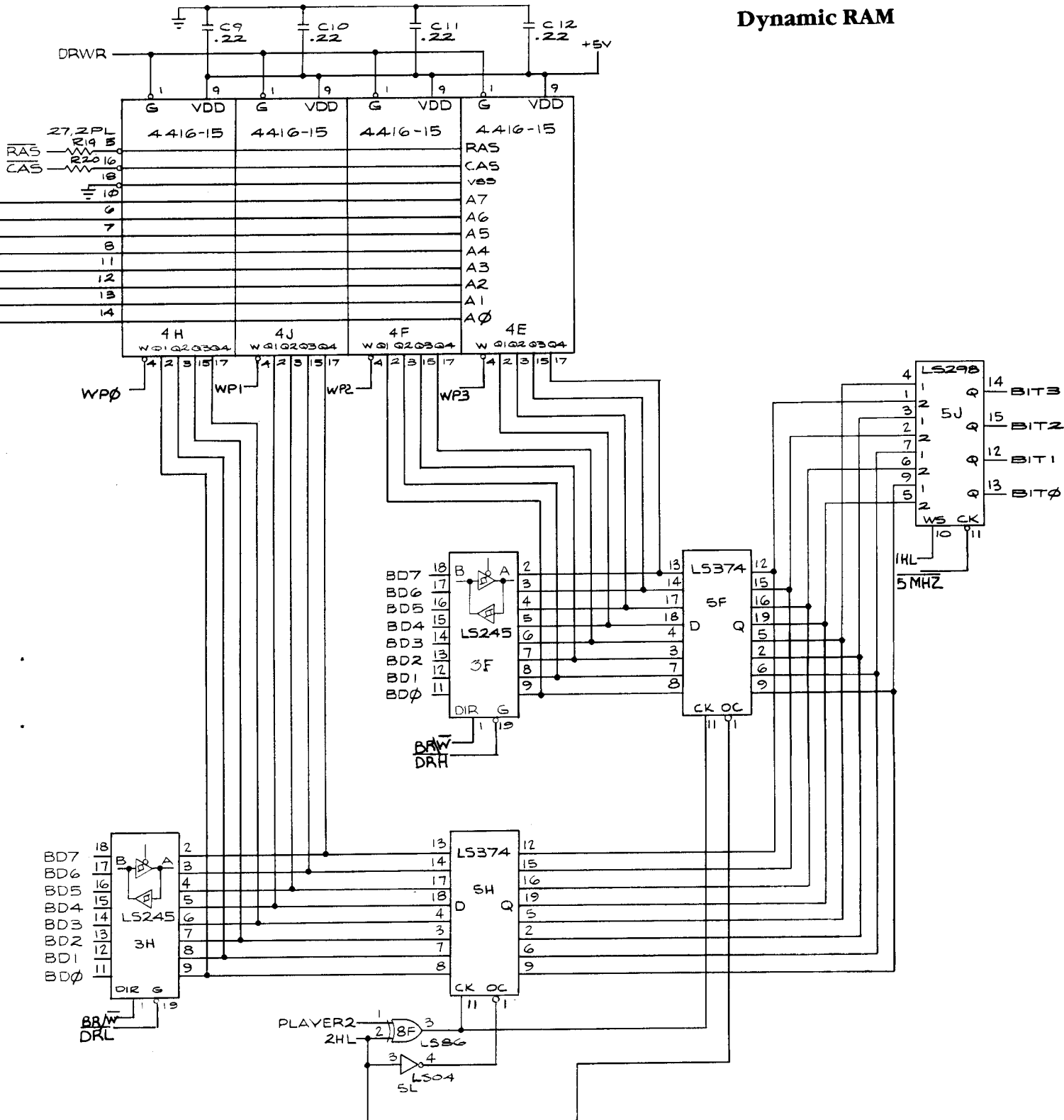
Horizontal Scrolling



Dynamic RAM Control



Dynamic RAM



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Crystal Castles PCB Schematic Diagram

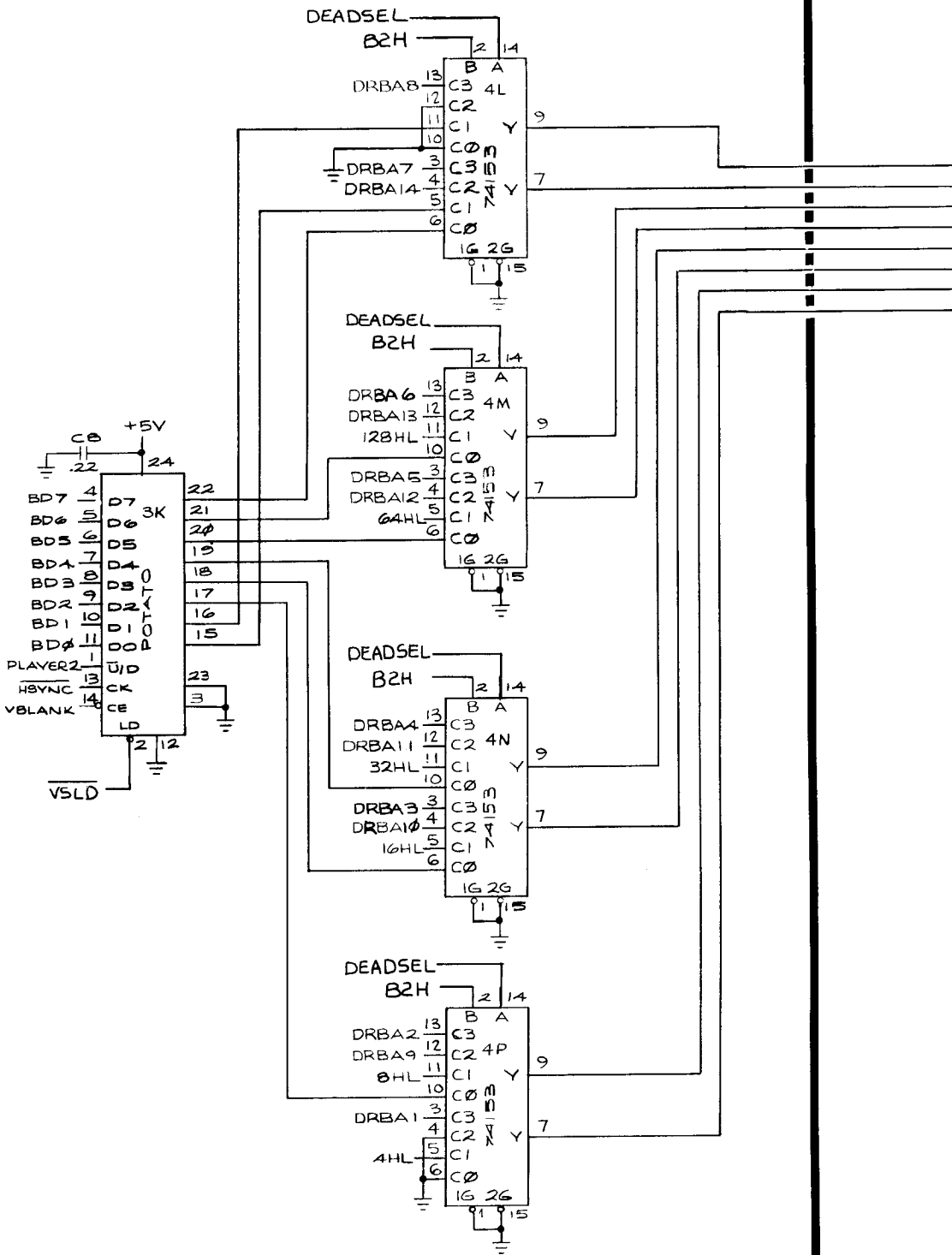


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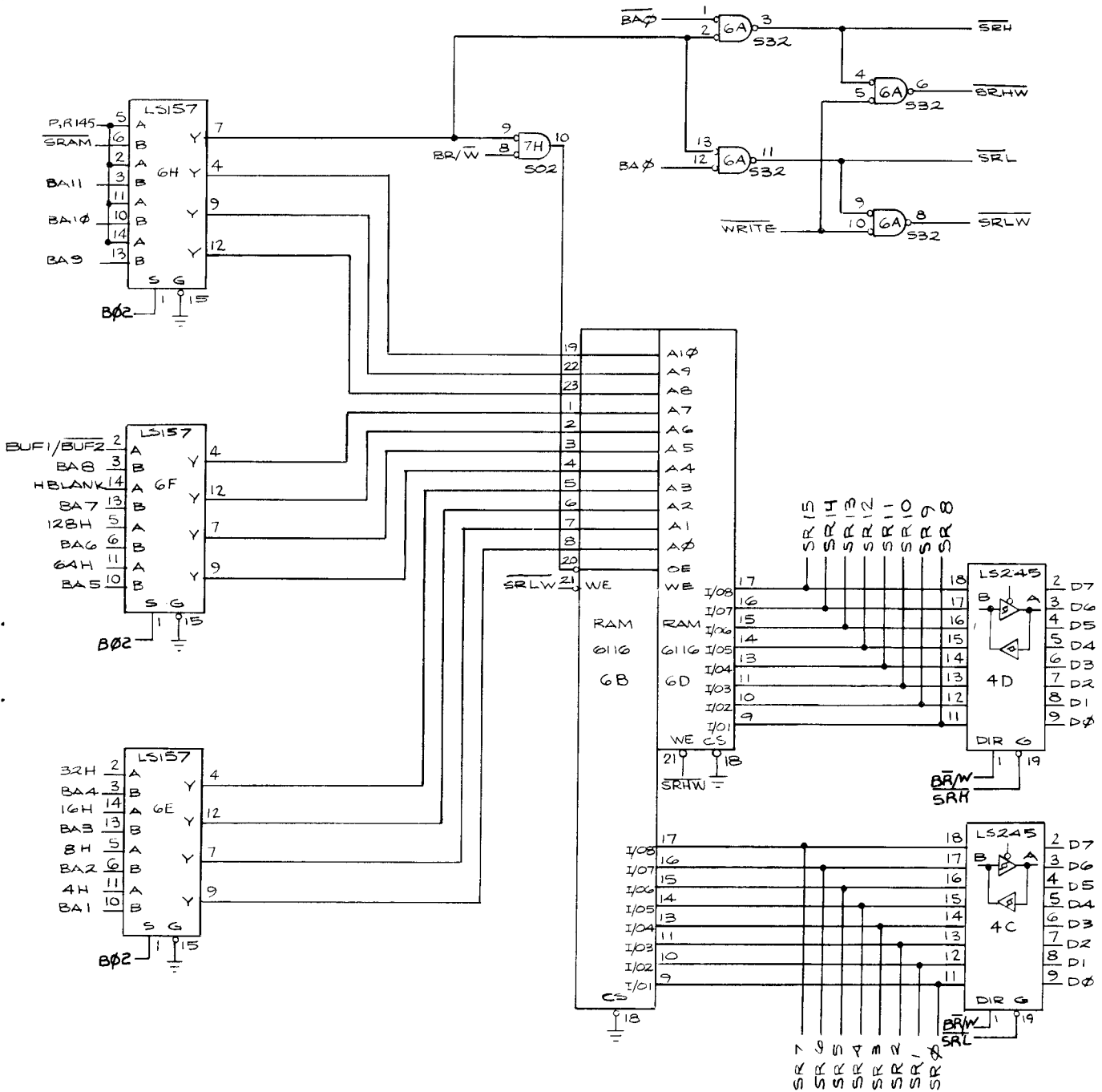
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Address Selectors



Working RAM and Motion-Object RAM



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Crystal Castles PCB Schematic Diagram

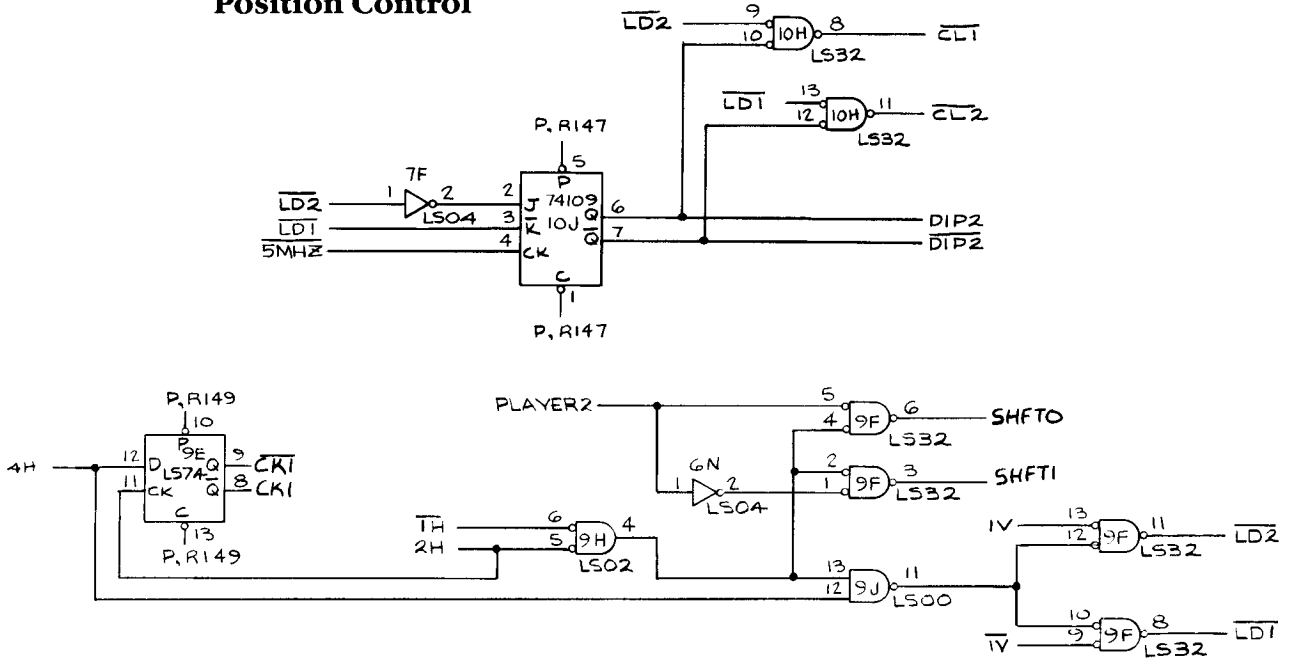


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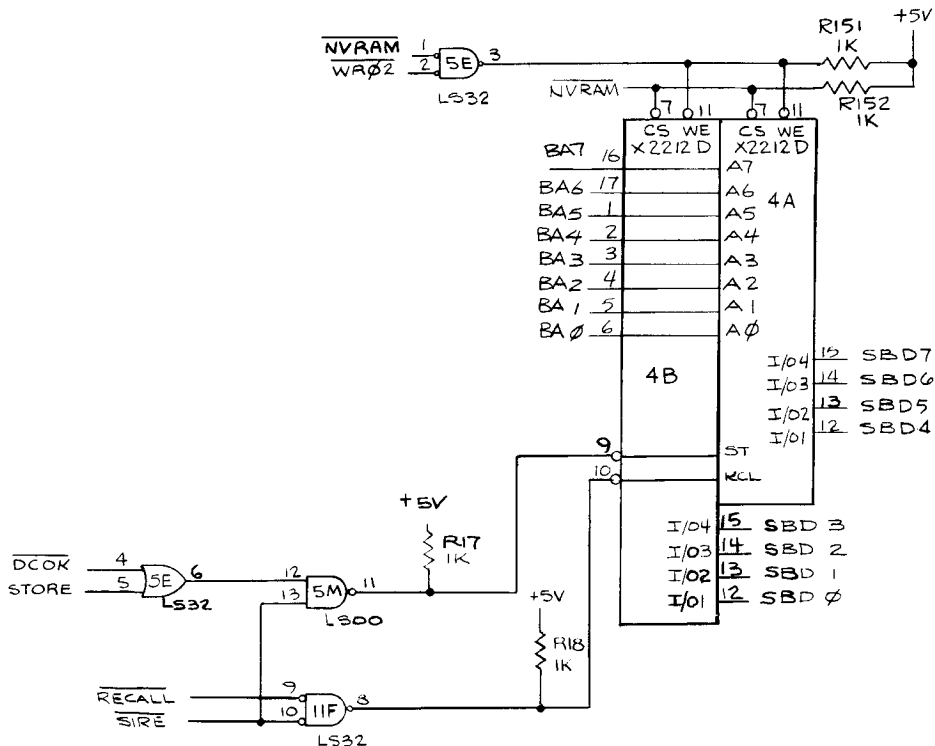
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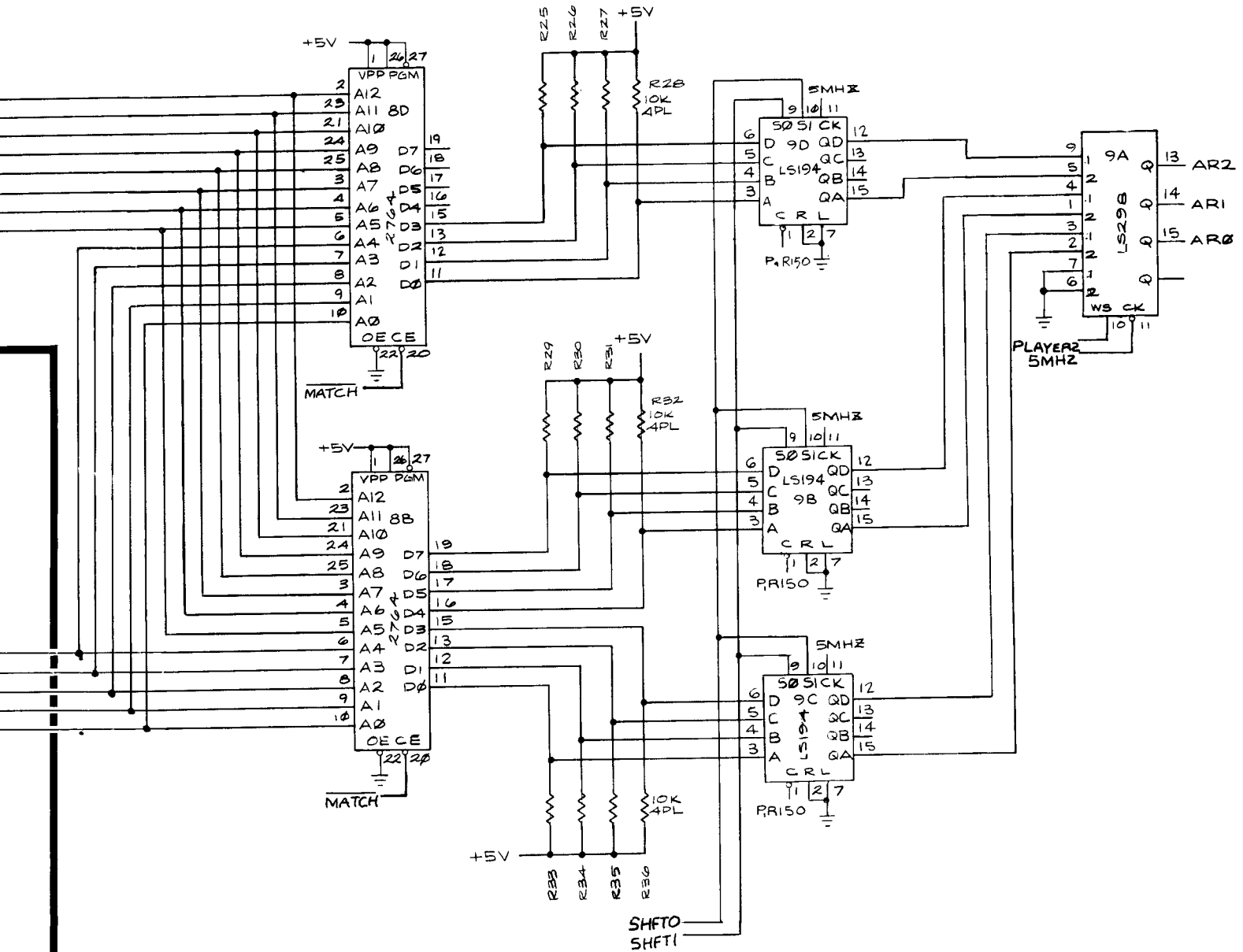
Position Control



Non-Volatile RAM



Motion-Object Picture ROM



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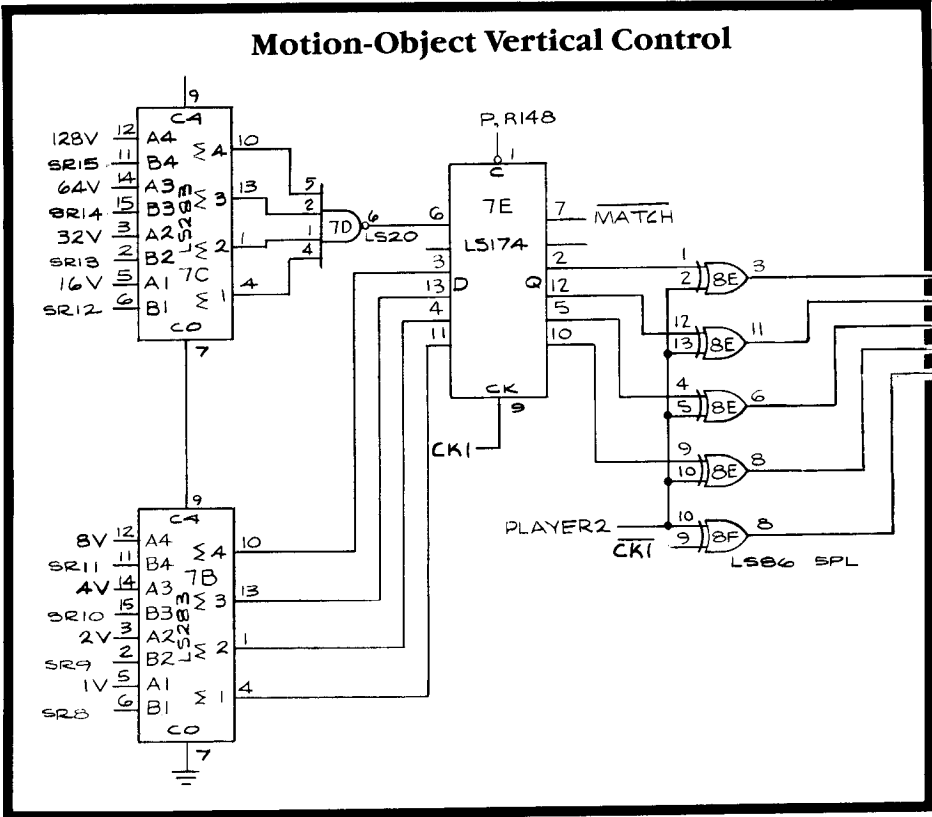
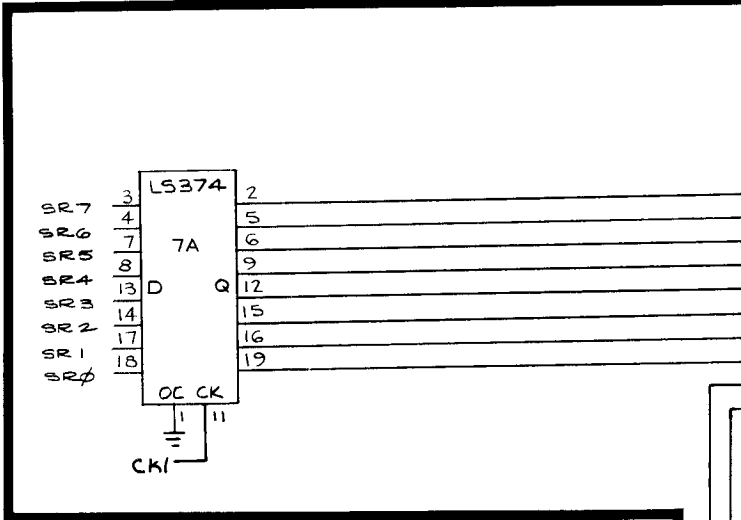
Crystal Castles PCB Schematic Diagram



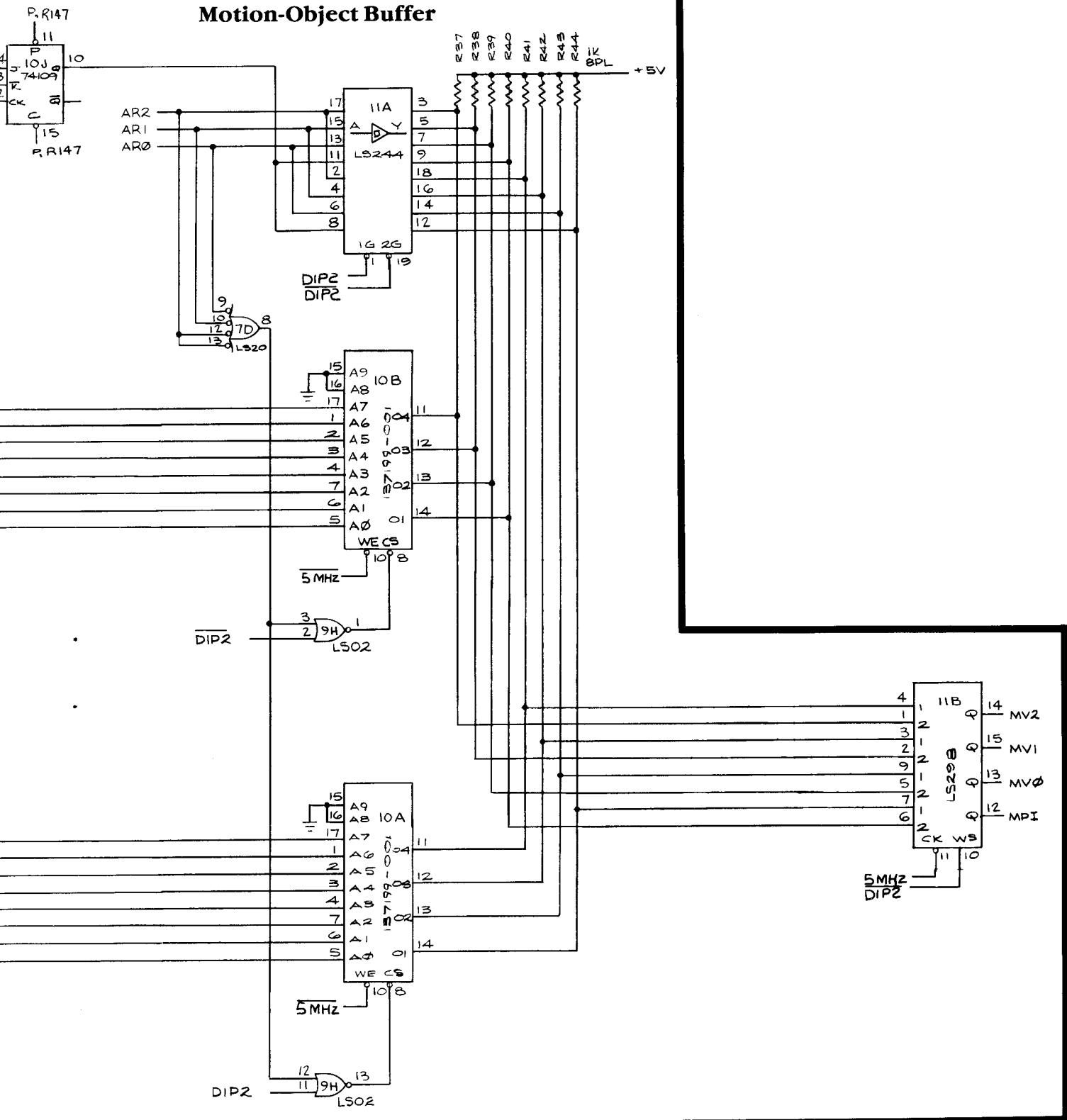
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Motion-Object Buffer



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Crystal Castles PCB Schematic Diagram

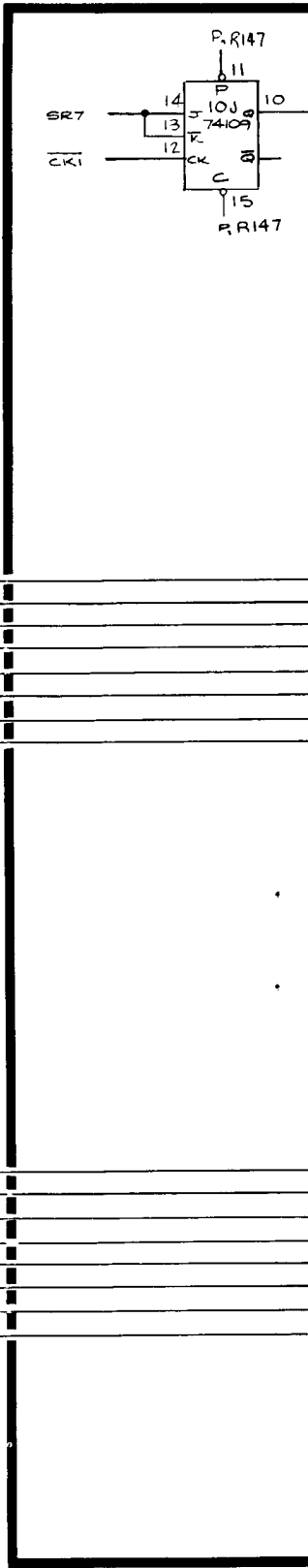
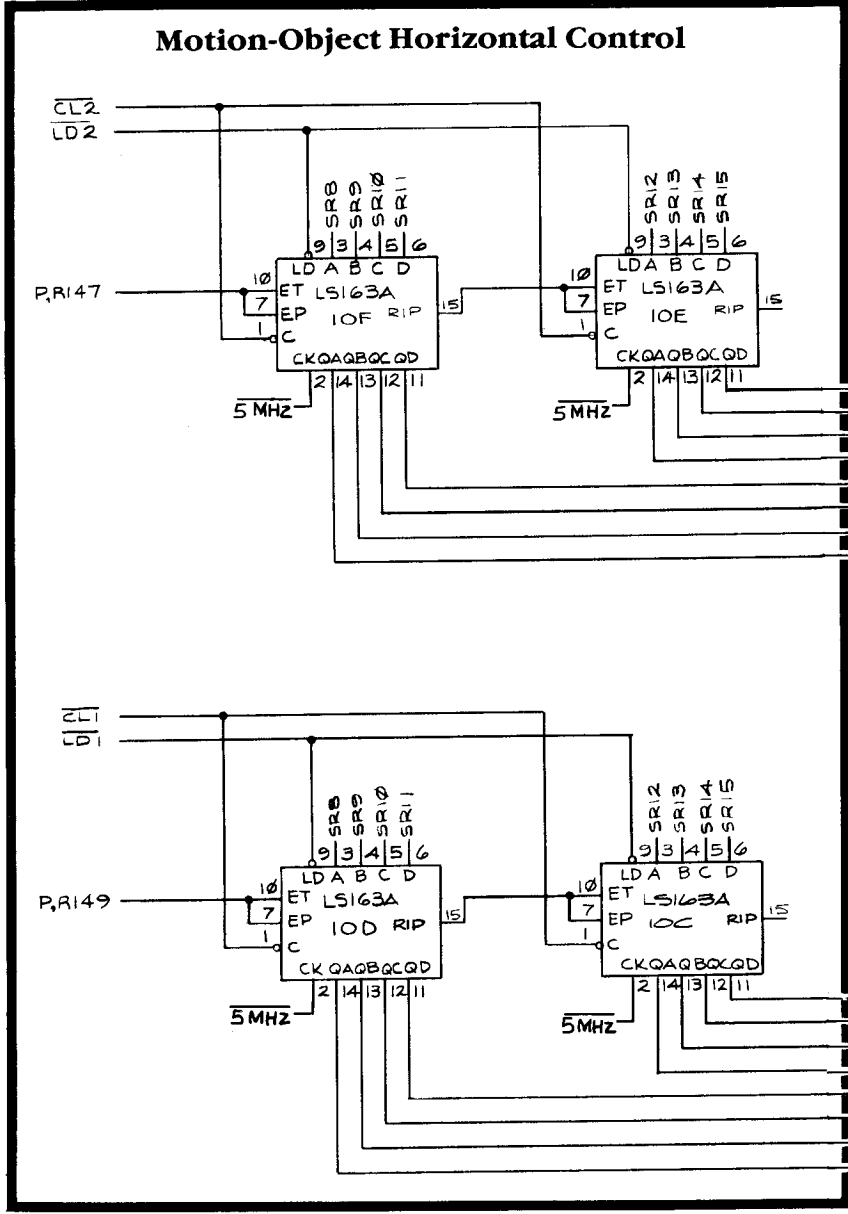


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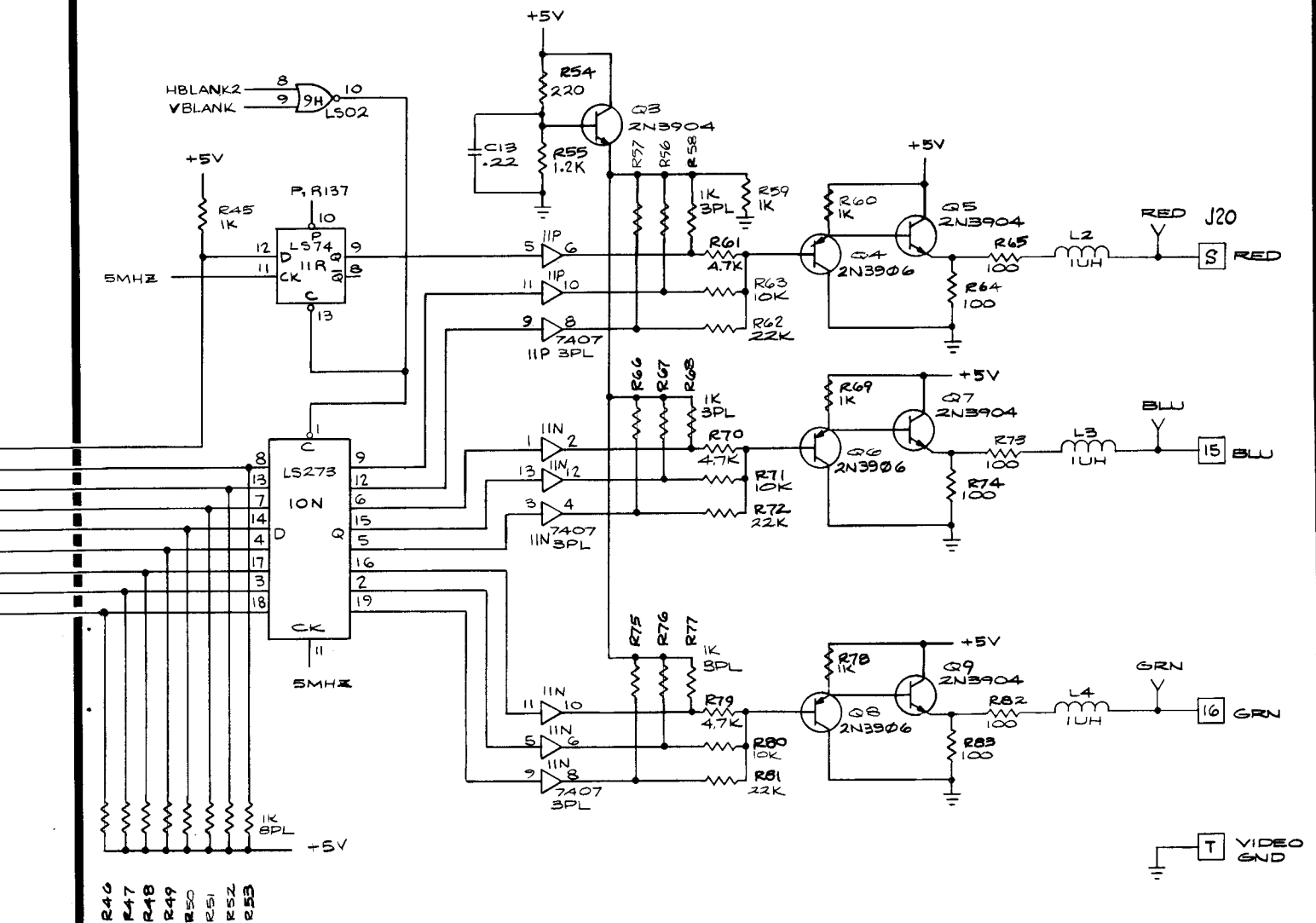
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Motion-Object Horizontal Control



Color Output



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Crystal Castles PCB Schematic Diagram

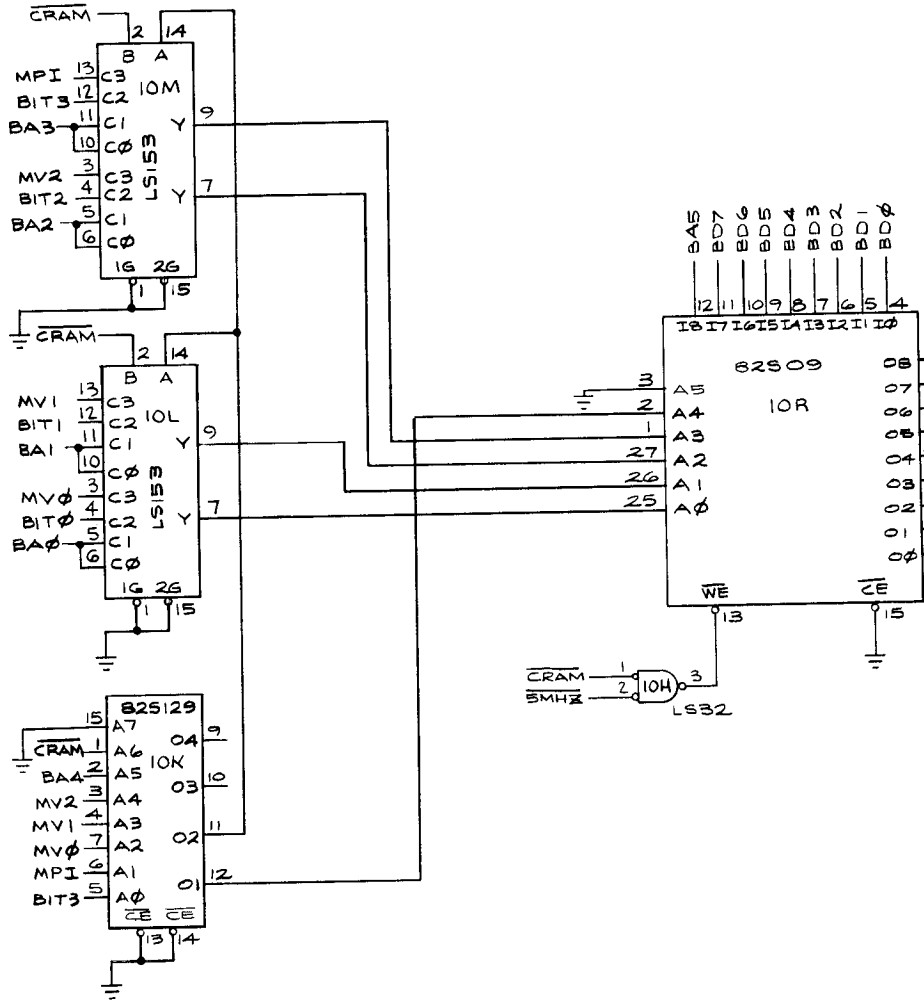


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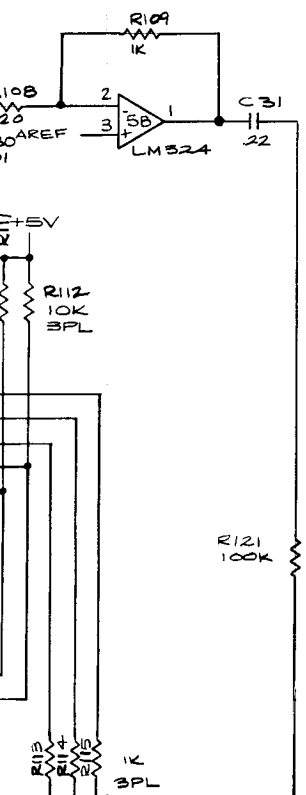
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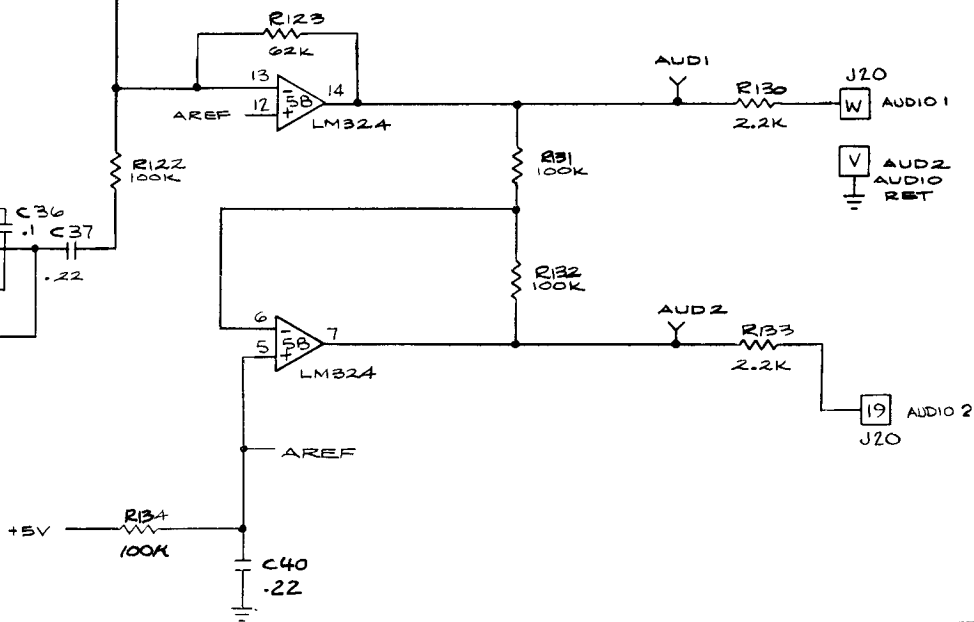
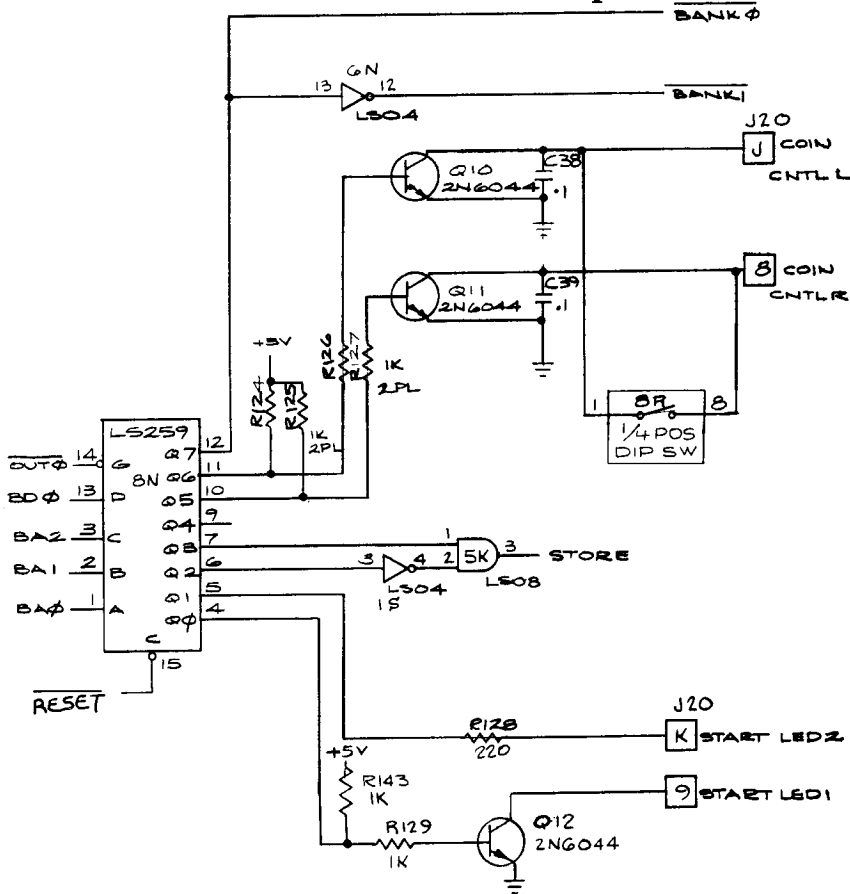
Color Memory



Output



Coin Counter and LED Output



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Crystal Castles PCB Schematic Diagram

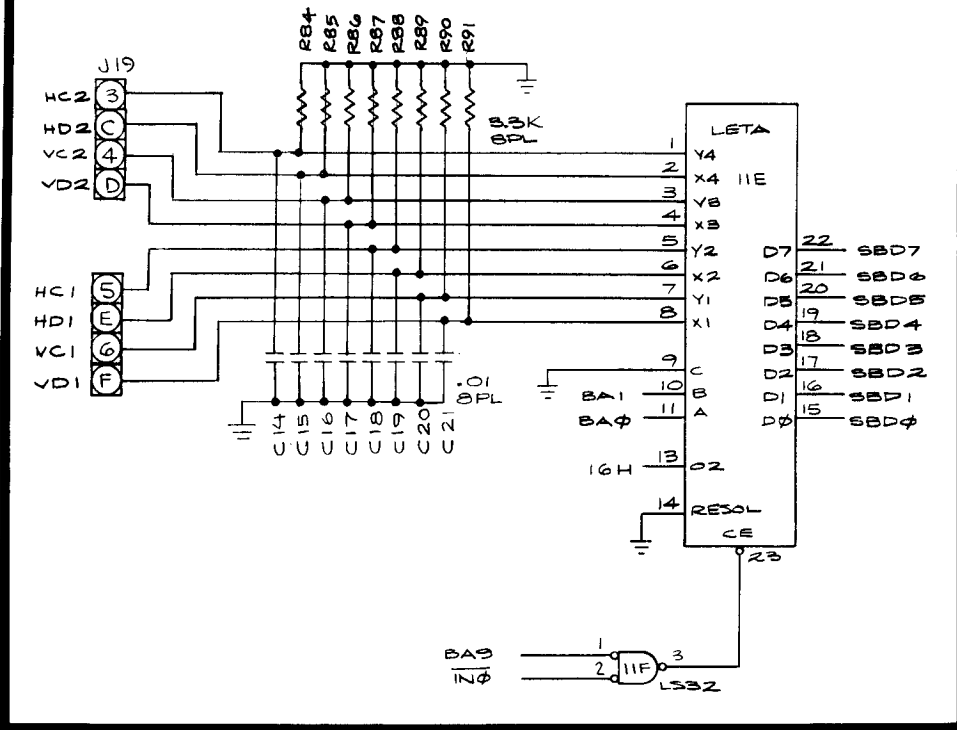


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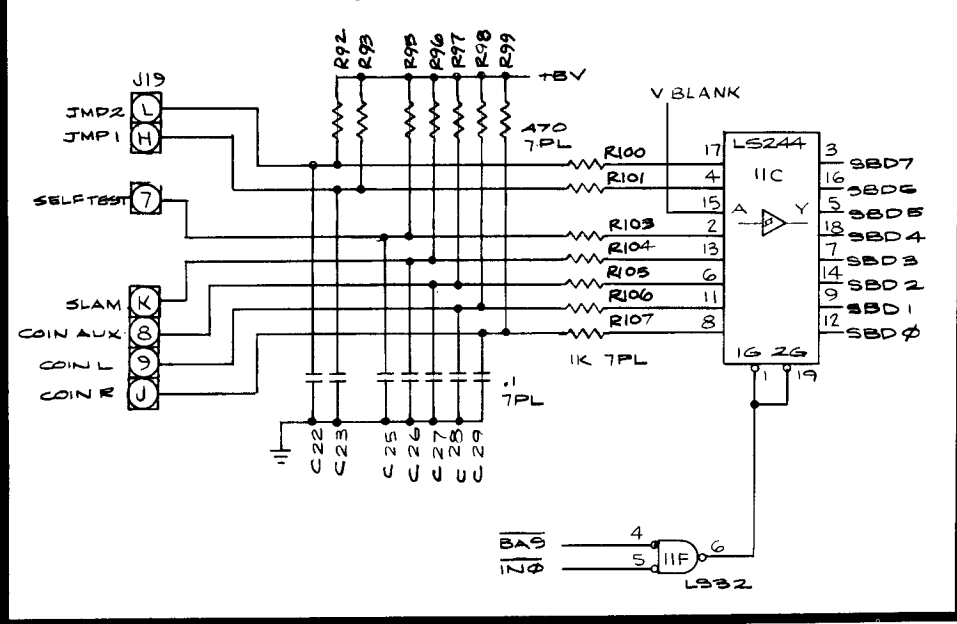
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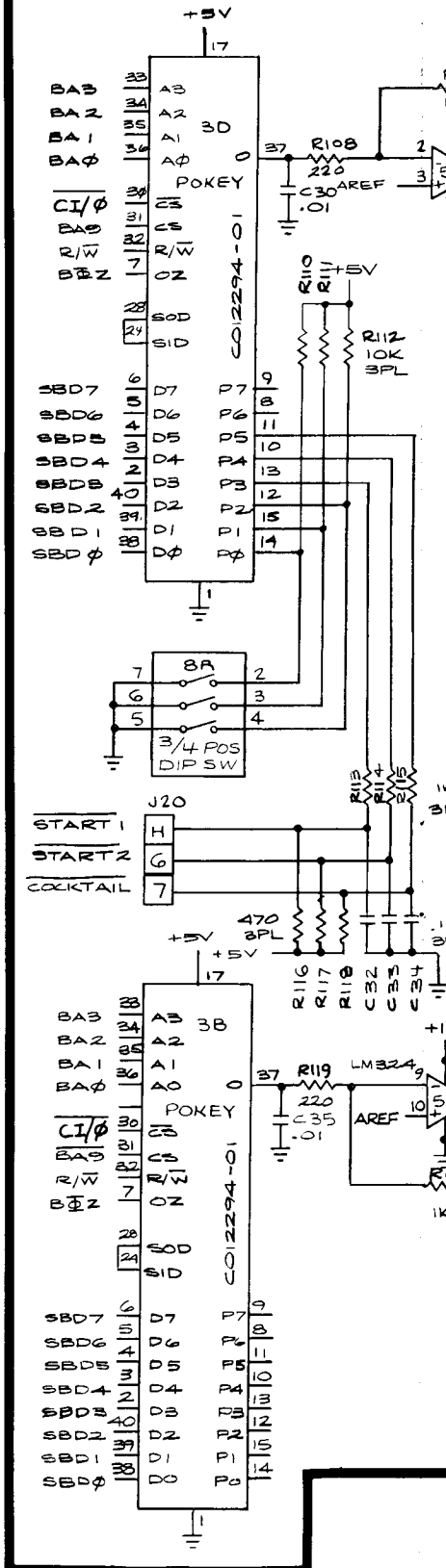
Trak-Ball Input

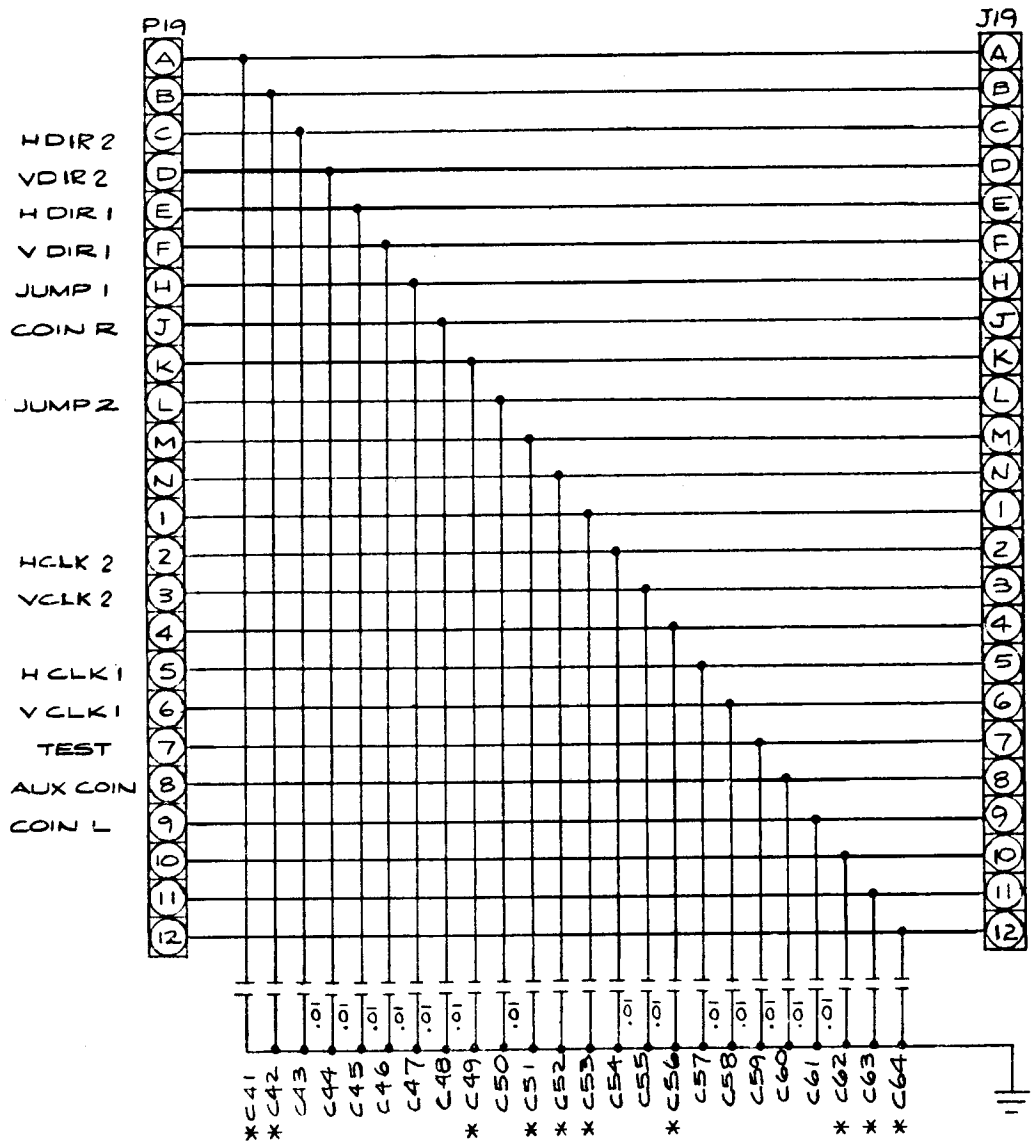


Player Switches Input



Audio Output





NOTES:

1. * DENOTES NOT LOADED CAPACITOR.

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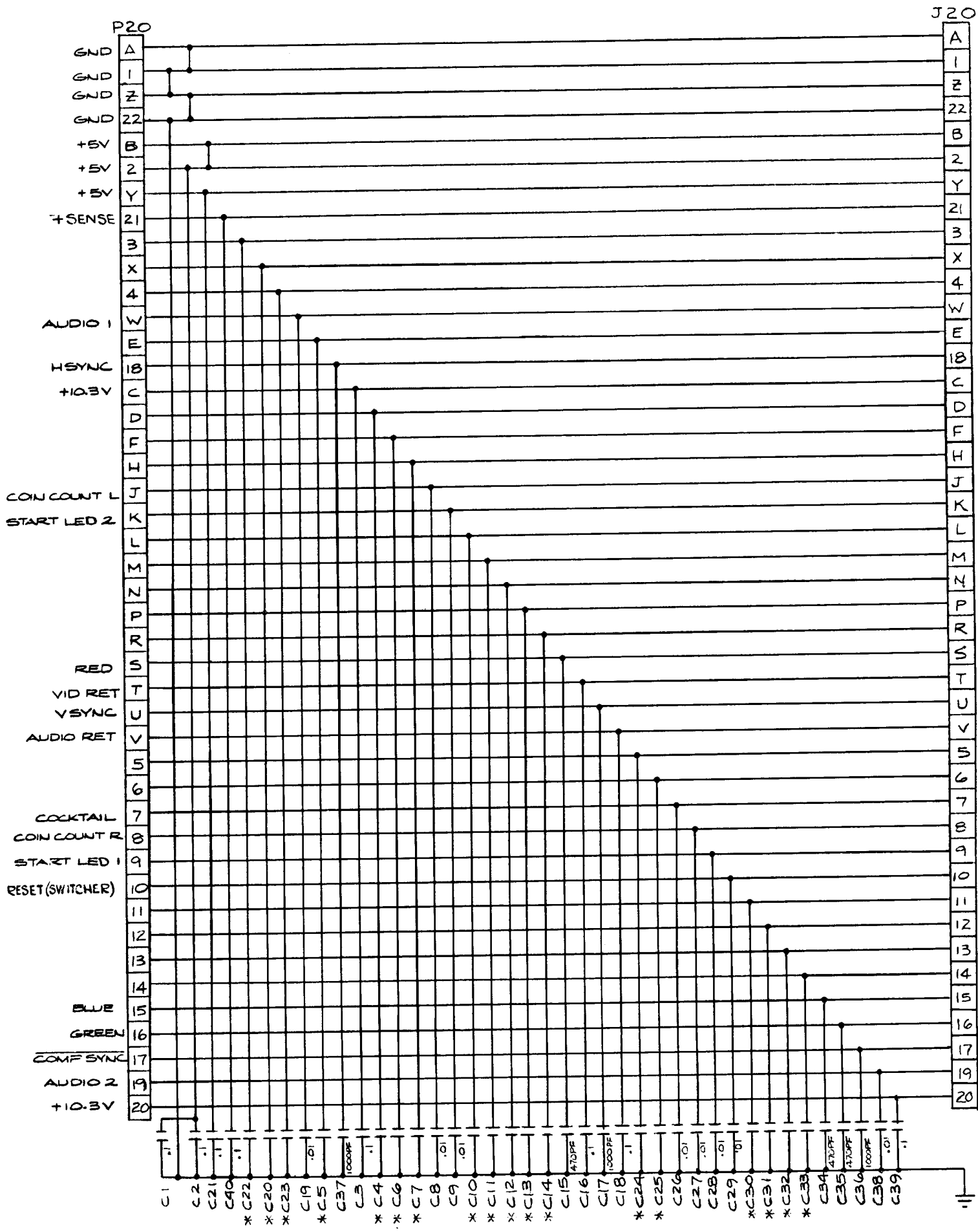
Crystal Castles EMI Shield PCB

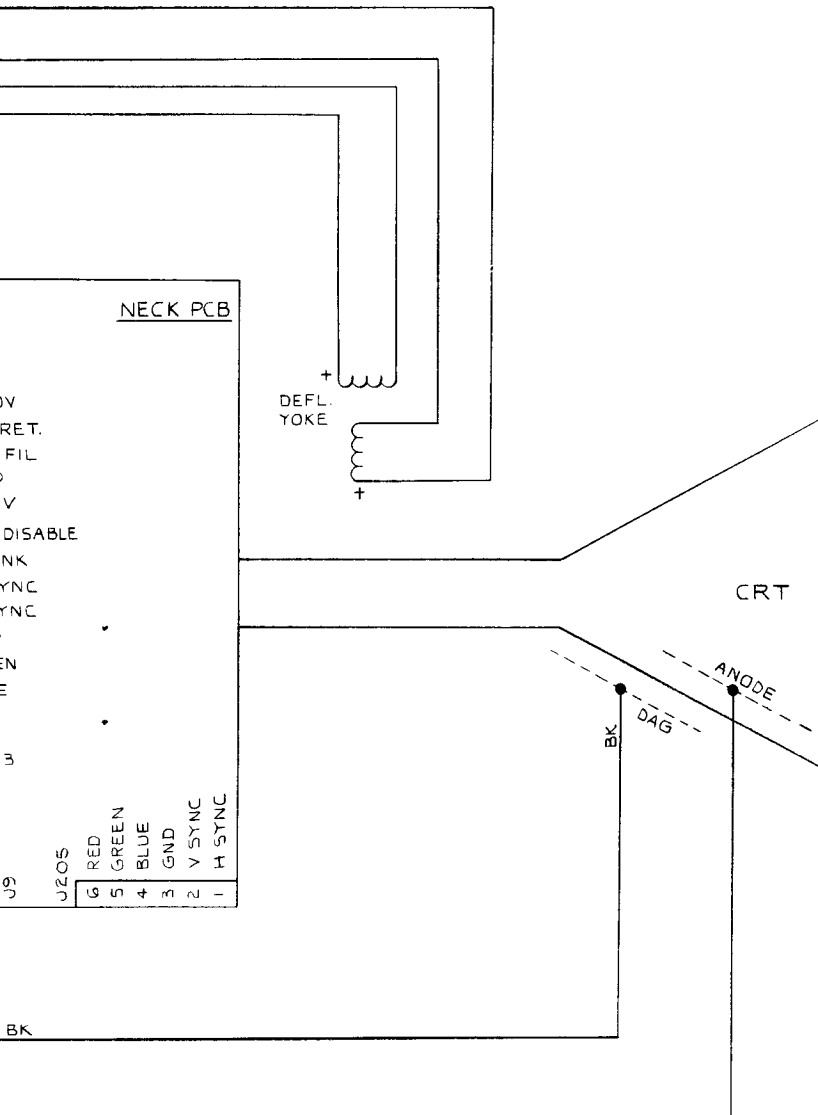


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NOTE:



1. ALTERNATE COLOR IN PARENTHESIS ().

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**Atari Color Raster Display
Wiring Diagram**

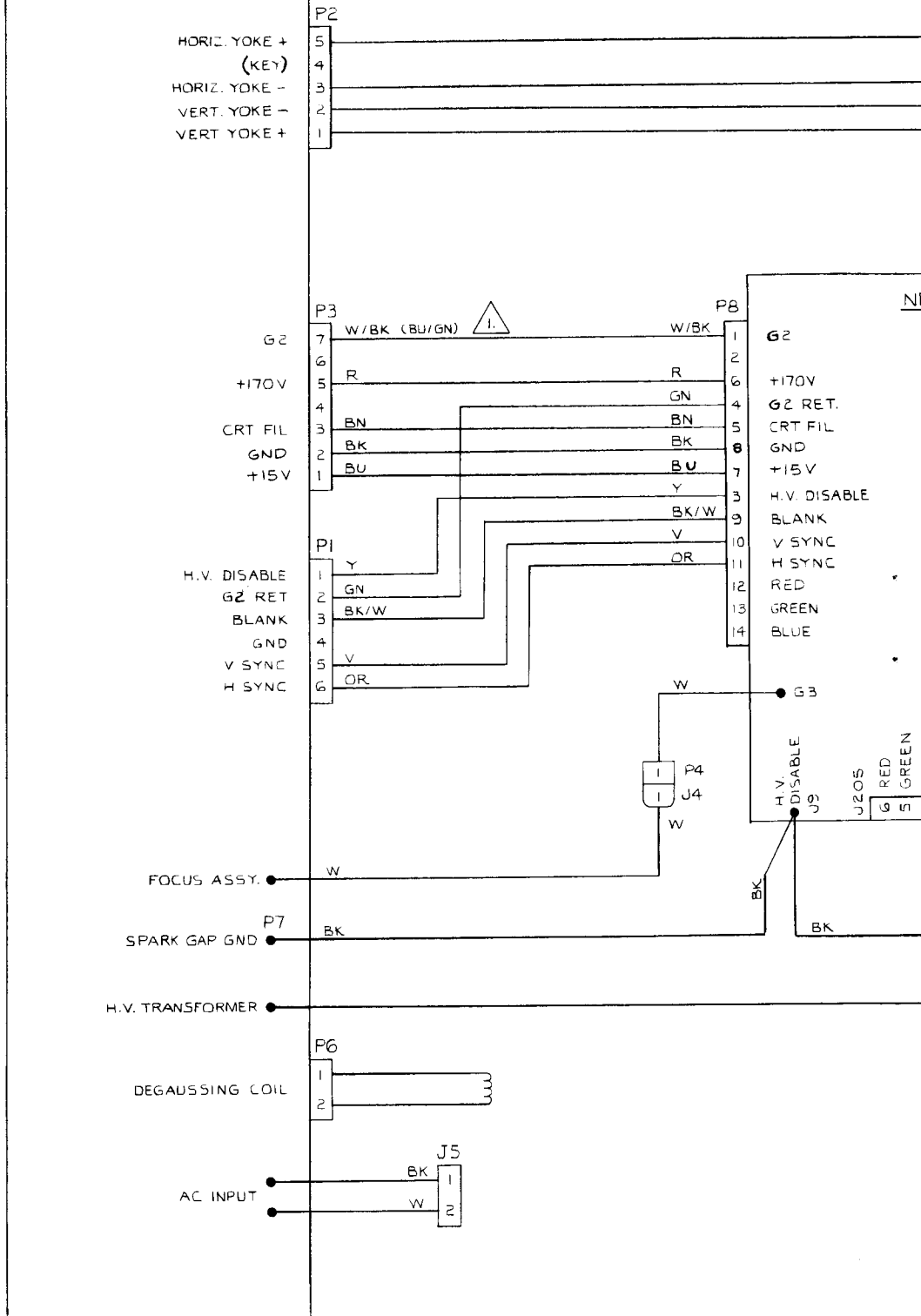


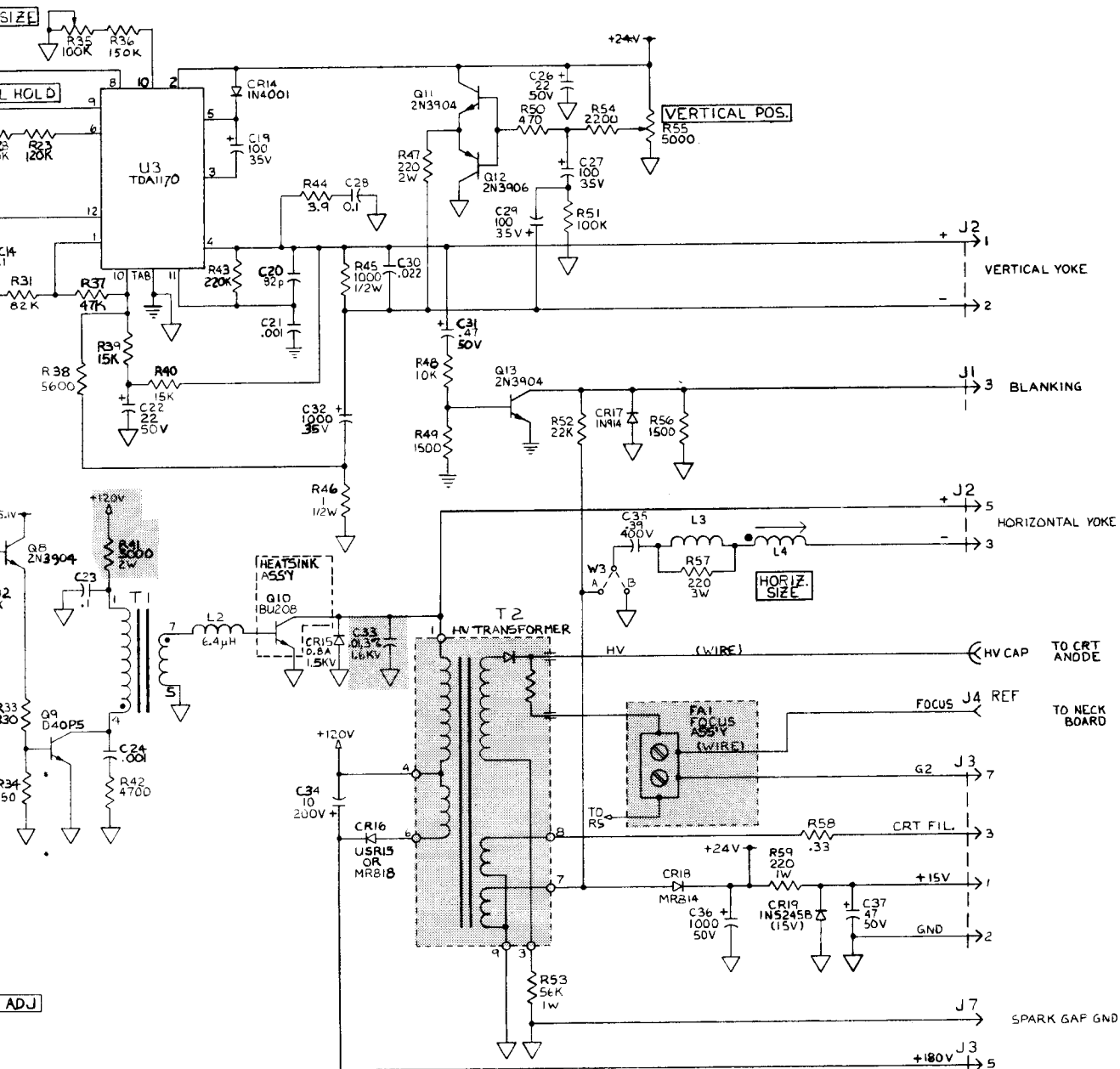
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DEFLECTION PCB






NOTES:
 UNLESS OTHERWISE SPECIFIED,
 1. ALL RESISTORS ARE 5% 1/4 WATT, AND IN OHMS.
 2. ALL CAPS ARE IN MICROFARADS.
 3. \perp INDICATES COM. CON. ∇ INDICATES EARTH GND.

PRODUCT SAFETY NOTICE

The shaded areas of this schematic indicate components whose values are of special significance to product safety. Should any component in the shaded areas need to be replaced, use only the value given in the parts lists. Do not deviate from the resistance, wattage, and voltage values shown.

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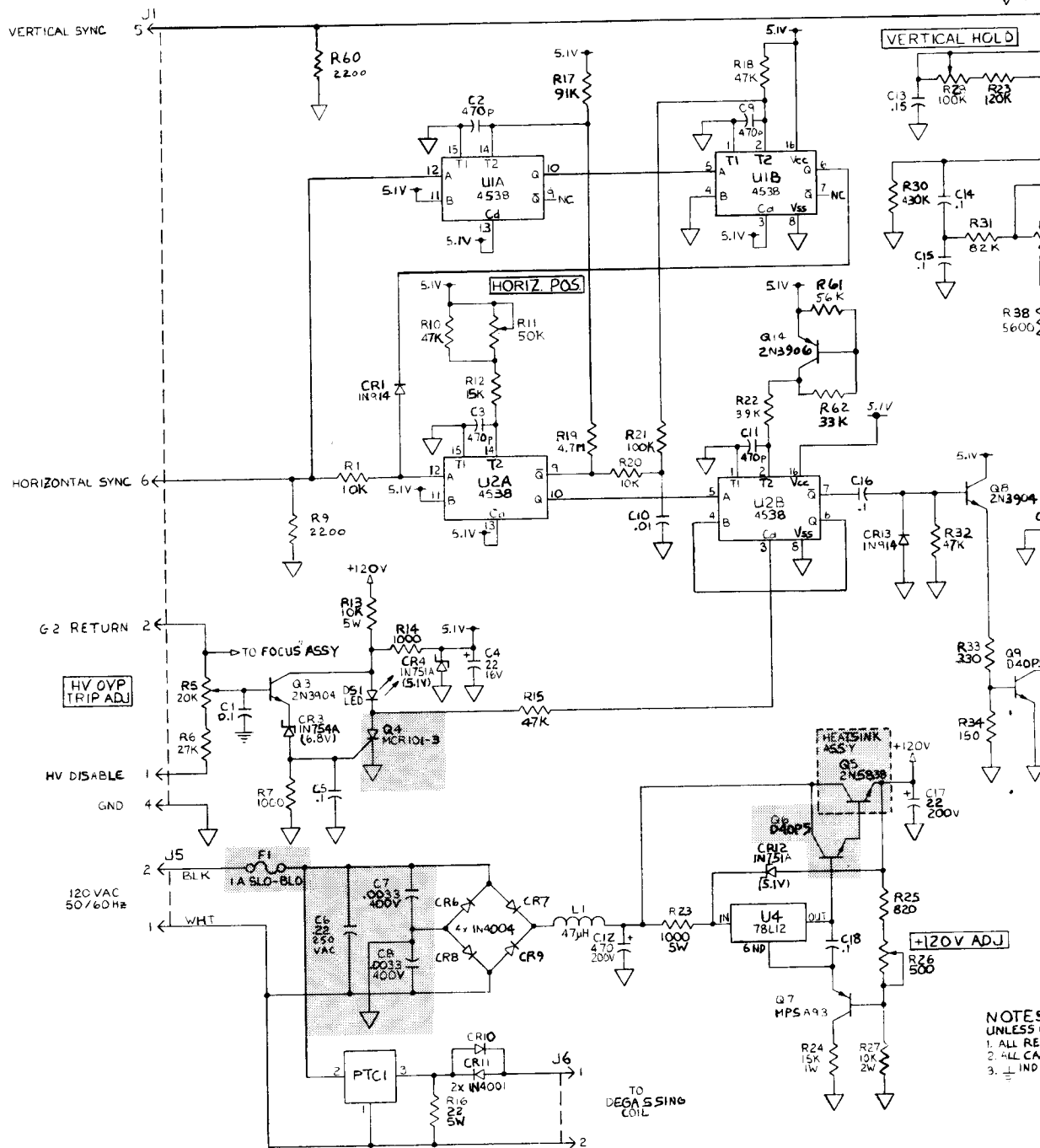
**Atari Color Raster
Display Deflection PCB**

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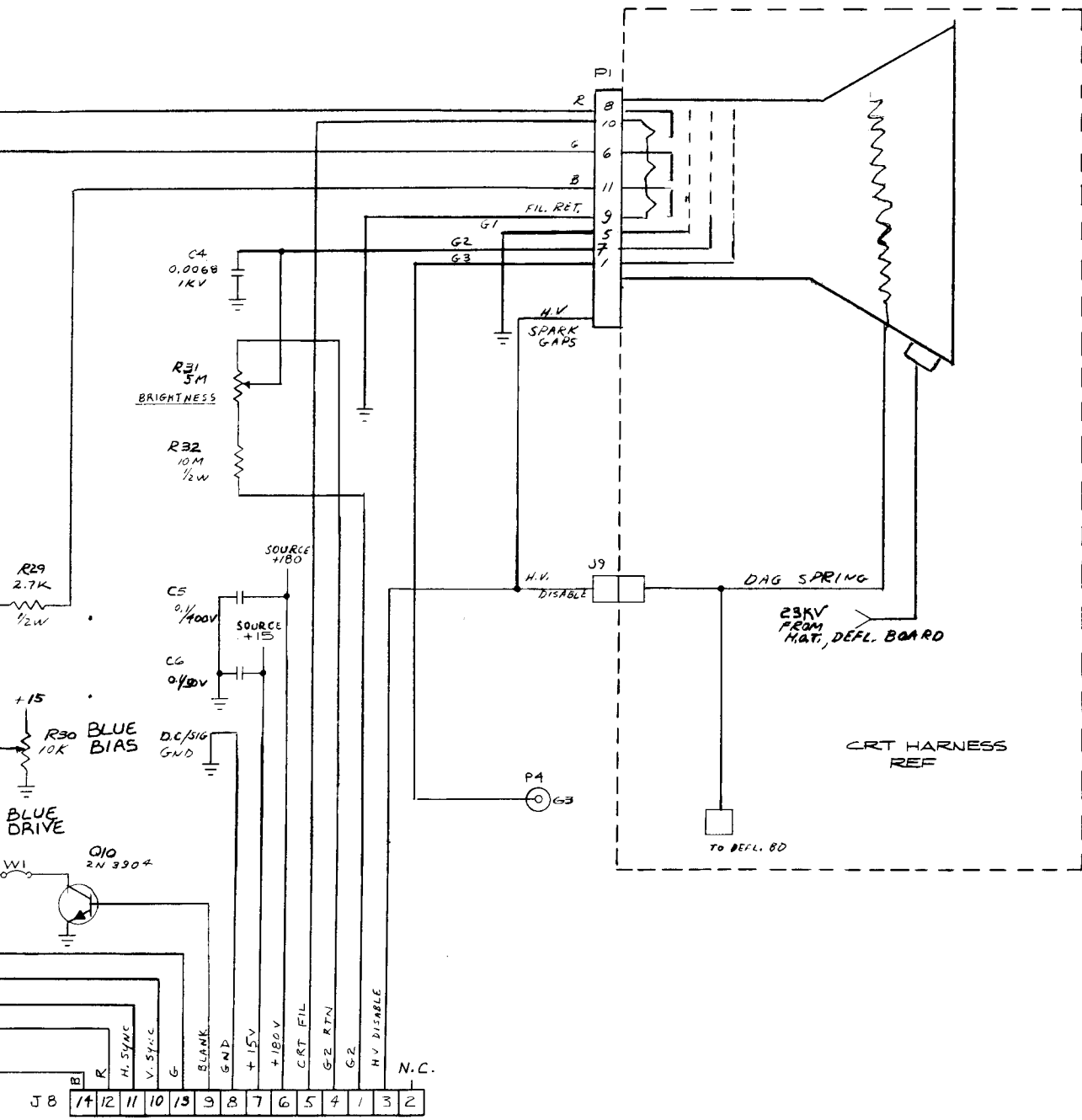
VERTICAL SIZE



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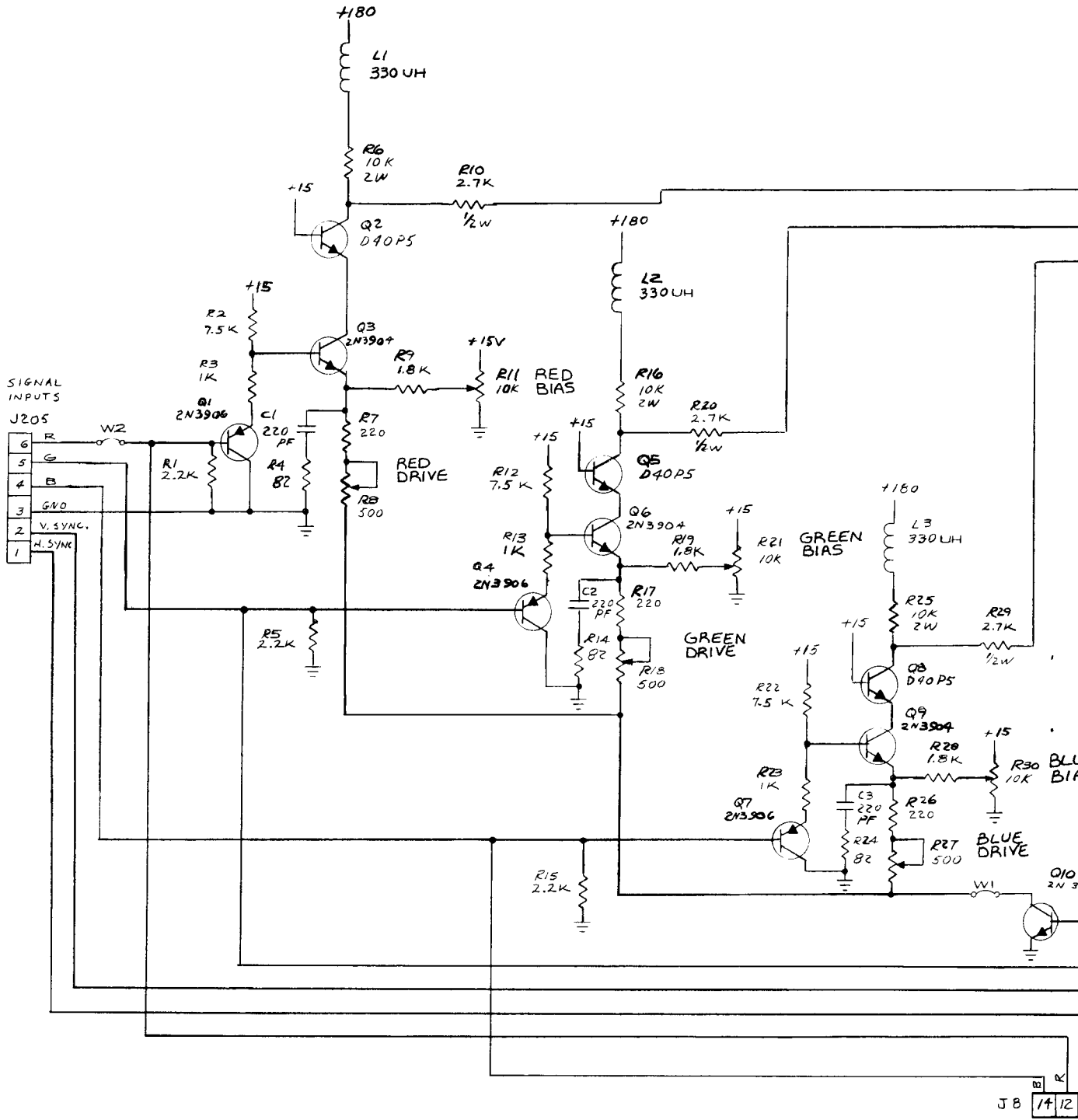
Atari Color Raster Display Neck PCB

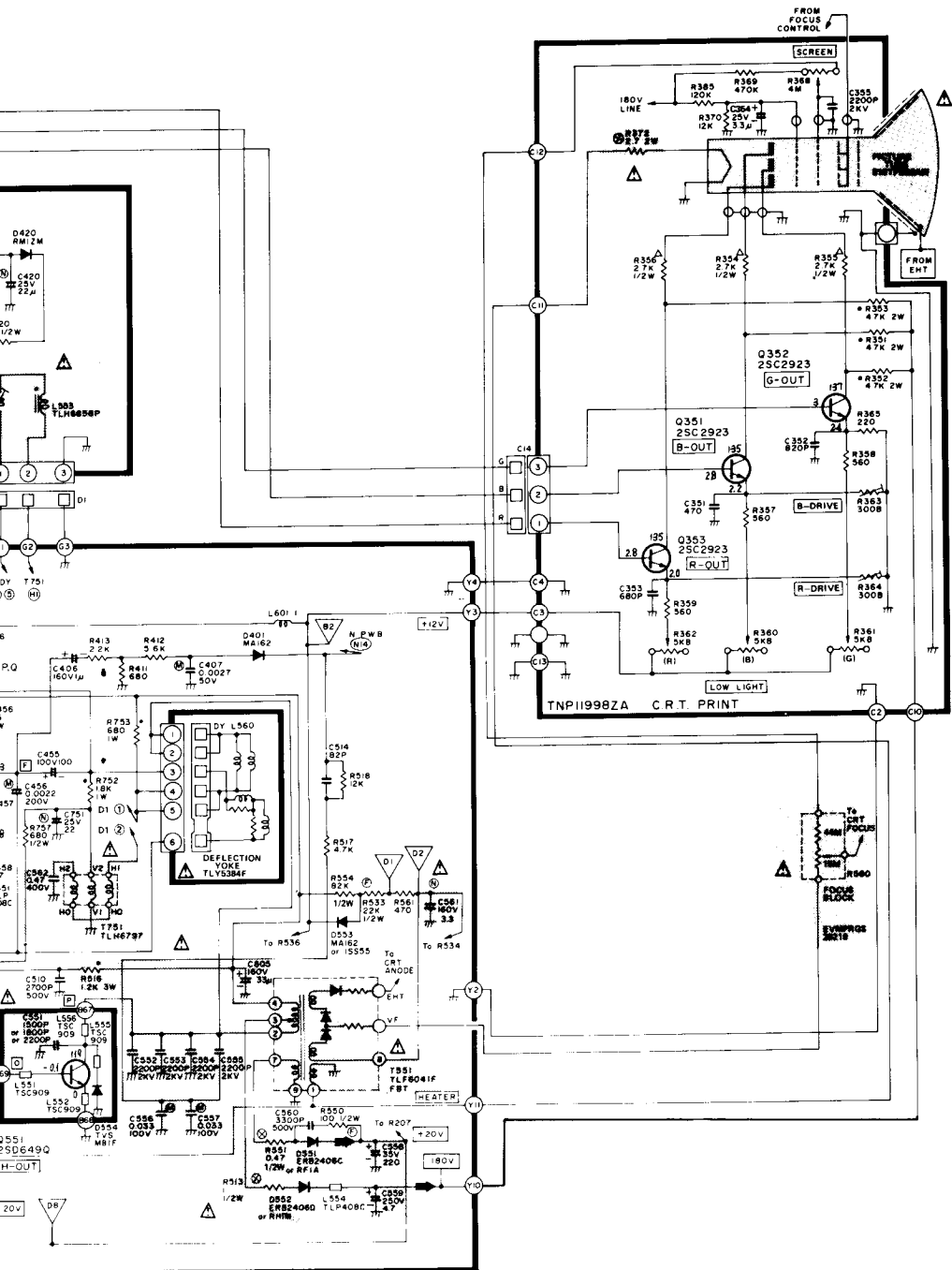


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WARNING

Components identified by shading have special characteristics important to safety and must be replaced only with identical parts.

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Matsushita Color Raster Display

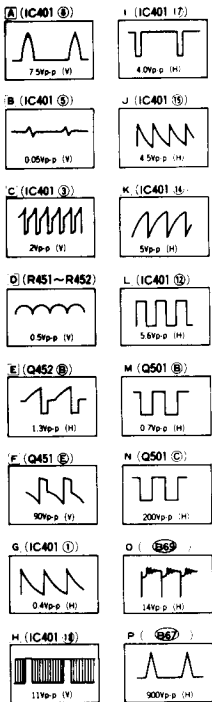


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Waveform



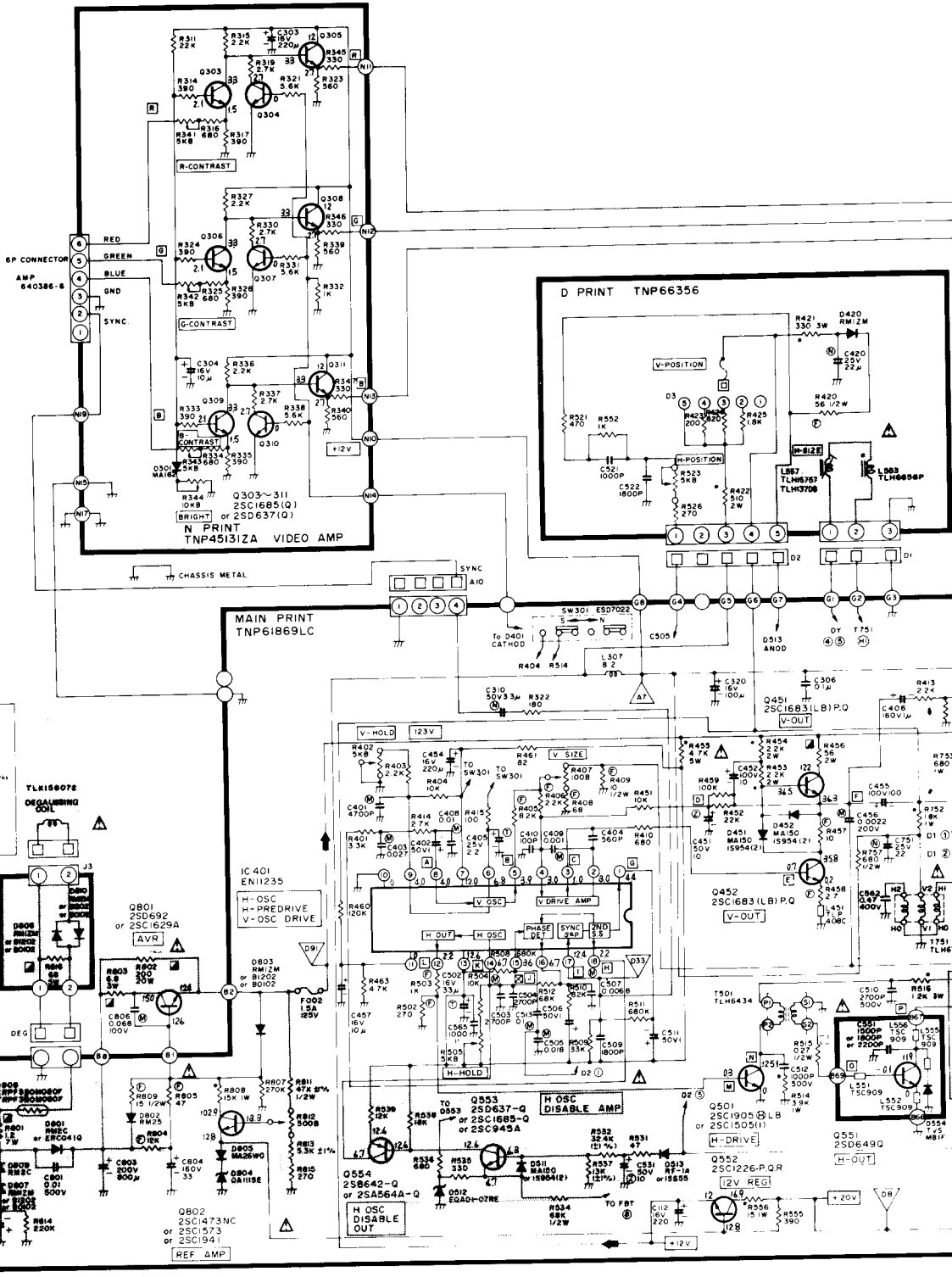
NOTE

1. RESISTOR
 All resistors are carbon 1/4W resistor, unless otherwise noted the following marks:
 Unit of resistance is OHM (Ω) 1K = 1,000, M = 1,000,000
 □ Solid * Metal Drip
 □ Wire Wound * Thermistor
 □ Non-Flammable * Fuse
 □ Cement

2. CAPACITOR
 All capacitors are ceramic 50V capacitor, unless otherwise noted the following marks:
 Unit of capacitance is μF, unless otherwise noted:
 □ Electrolytic * Safety Vent * Polyester
 □ Bore * Titanium Oxide * Polystyrene
 □ Z type * Temp. Compensation
 □ Discoid Tantalum * Polyester

3. COIL
 Unit of inductance is μH

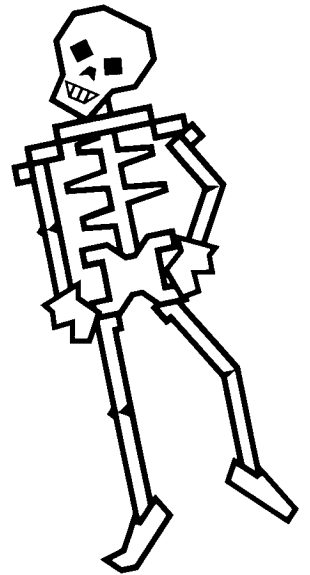
4. TEST POINT
 □ Test point position
 □ Test point position



J PRINT TNP 56507ZA DEGAUSS

IC 401 EN11235

Q551 2SC1226-PQR
[2V REG]



Crystal Castles™ Troubleshooting Guide



 A Warner Communications Company

Crystal Castles™

Troubleshooting with the CAT Box

Troubleshooting with the Read/Write Controller

A. CAT Box Preliminary Set-Up

1. Remove the electrical power from the game and the CAT Box.
2. Remove the wiring harness from the game PCB.
3. Remove the game PCB from the game cabinet.
4. Remove Microprocessor 2C from the game PCB.
5. Connect the harness from the game to the game PCB.
6. Connect together the $\Phi 0$ and $\Phi 2$ test points on the game PCB with the shortest possible jumper.
7. Connect the \overline{WDDIS} test point to ground.
8. Connect the CAT Box flex cable to the game PCB edge test connector.
9. Apply power to the game and to the CAT Box.
10. Set CAT Box switches as indicated:
 - a. TESTER SELF-TEST: OFF
 - b. TESTER MODE: R/ \overline{W}
11. Press TESTER RESET.
12. Connect the DATA PROBE to the CAT Box. Connect the DATA PROBE ground clip to a game PCB ground test point.

B. Checking the Address Lines

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
 - a. BYTES: 1
 - b. PULSE MODE: UNLATCHED
 - c. R/ \overline{W} MODE: (OFF)
 - d. R/ \overline{W} : READ
3. Key in the address pattern given in Table 1 (use AAAA to start) with the CAT Box keyboard.
4. Set R/ \overline{W} MODE to STATIC.
5. Probe each IC-pin listed in Table 1 with the DATA PROBE and check that the CAT Box 1 or 0 LED for the corresponding address line lights up.
6. Repeat parts 2-c through 5 using address 5555 in part 3.

Table 1 Address Lines

Logic State for Address AAAA	IC-Pin	Logic State for Address 5555
BA15 1	1B3	0
BA14 0	1B5	1
BA13 1	1B7	0
BA12 0	1B9	1
BA11 1	1B12	0
BA10 0	1B14	1
BA9 1	1B16	0
BA8 0	1B18	1
BA7 1	1C9	0
BA6 0	1C7	1
BA5 1	1C5	0
BA4 0	1C3	1
BA3 1	1C12	0
BA2 0	1C14	1
BA1 1	1C16	0
BA0 0	1C18	1

C. Checking the Data Lines

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
 - a. BYTES:1
 - b. R/ \overline{W} MODE: (OFF)
 - c. R/ \overline{W} : WRITE
3. Key in address 0000 with the keyboard.
4. Press DATA SET. Key in data AA with the keyboard.
5. Set R/ \overline{W} MODE to STATIC.
6. Probe each IC-pin listed in Table 2 with the DATA PROBE and check that the CAT Box 1 or 0 LED for the corresponding address line lights up.
7. Set R/ \overline{W} MODE to (OFF).
8. Repeat parts 4 through 6 using data 55 in part 4.

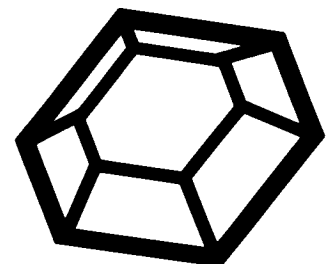
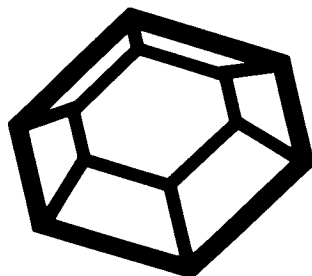


Table 2 Data Lines

Logic State for Data AA	IC-Pin	Logic State for Data 55
D7 1	2E-11	0
D6 0	2E-12	1
D5 1	2E-13	0
D4 0	2E-14	1
D3 1	2E-15	0
D2 0	2E-16	1
D1 1	2E-17	0
D0 0	2E-18	1
BD7 1	2E-9	0
BD6 0	2E-8	1
BD5 1	2E-7	0
BD4 0	2E-6	1
BD3 1	2E-5	0
BD2 0	2E-4	1
BD1 1	2E-3	0
BD0 0	2E-2	1

D. Checking the RAM

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
 - a. DBUS SOURCE: ADDR
 - b. BYTES:1024
 - c. R/W MODE: (OFF)
 - d. R/W: WRITE
3. Enter address 0003 with the keyboard.
4. Set the CAT Box switches as indicated:
 - a. R/W MODE to PULSE and back to (OFF)
 - b. R/W to READ
 - c. R/W MODE to PULSE and back to (OFF)
5. If the CAT Box reads an address that doesn't compare with that written, the COMPARE ERROR LED will light up. The ADDRESS/SIGNATURE display of the CAT Box will show the failing address location and the ERROR DATA DISPLAY switch is enabled. Using this switch, determine if the error is in the high-order or low-order RAM.
6. Repeat this test with DBUS SOURCE set to ADDR.
7. Set the CAT Box switches as indicated:
 - a. BYTES: 256
 - b. DBUS SOURCE: ADDR
 - c. R/W: (OFF)
 - d. R/W: WRITE
8. Repeat parts 5 through 6 to check addresses from 1000 through 8FFF.

NOTE

The two custom audio I/O chips must be tested separately by performing the self-test, substituting a known good part, or performing the following procedure.

E. Checking the Custom Audio I/O Chips

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
 - a. BYTES: 1
 - b. R/W: WRITE
 - c. R/W MODE: (OFF)
3. Enter the address from Table 3 with the keyboard.
4. Press DATA SET and enter the data from Table 3 with the keyboard.
5. Set R/W to PULSE and back to (OFF).
6. Repeat parts 3 through 5 for each address and data listed in Table 3. Check for the response indicated.

Table 3 Custom Audio I/O Chips

Address	Data	Test Results
98	00	Custom Audio I/O Chip 4D channel 1 produces pure tone.
98	03	
98	55	
98	AF	
98	00	Custom Audio I/O Chip 4D channel 1 turns off.
98	55	
98	AF	Custom Audio I/O Chip 4D channel 2 produces pure tone.
98	00	Custom Audio I/O Chip 4D channel 2 turns off.
9A	00	Custom Audio I/O Chip 4B channel 1 produces pure tone.
9A	03	
9A	55	
9A	AF	
9A	00	Custom Audio I/O Chip 4B channel 1 turns off.
9A	55	
9A	AF	Custom Audio I/O Chip 4B channel 2 produces pure tone.
9A	00	Custom Audio I/O Chip 4B channel 2 turns off.

F. Checking the Player Switch, Option Switch, and Trak-Ball™ Inputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
 - a. BYTES: 1
 - b. R/W: WRITE
 - c. R/W MODE: (OFF)
3. Enter address 9600 with the keyboard.
4. Press DATA SET and enter data FF with the keyboard.
5. Set R/W to PULSE and back to (OFF).
6. For each entry listed in Table 4, do the following:
 - a. Set R/W MODE to (OFF).
 - b. Set R/W WRITE.
 - c. Enter the first address with the keyboard.
 - d. Press DATA SET and enter the data for that address with the keyboard.
 - e. Set R/W MODE to PULSE and back to (OFF).
 - f. Set R/W to READ.
 - g. Enter the next address.
 - h. Set R/W MODE to STATIC.
 - i. Activate the input switch or signal indicated in Table 4 and check the test result.
 - j. Set R/W MODE to (OFF).
 - k. Repeat parts g through j for each subsequent address given for the entry.

Table 4 Player Switches, Option Switches, and Trak-Ball™ Inputs

Address	Input Switches/Signals	Test Results
9400	Trak-Ball™ VERT	
9401	Trak-Ball™ HORIZ	
9402	Trak-Ball™ VERT (Player 2)	
9403	Trak-Ball™ HORIZ (Player 2)	
9600	D0 COIN R D1 COIN L D2 COIN AUX D3 SLAM D4 SELF TEST D5 SPARE D6 JMP1 D7 JMP2	
00-9A0B	SW2 D0 SW3 D1 SW4 D2	Read switches at address 9A08. DATA display changes when any of these switches or signals are activated.

G. Checking the Coin Counter and Trak-Ball Light

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
 - a. DBUS SOURCE: DATA
 - b. BYTES: 1
 - c. R/W: WRITE
 - d. R/W MODE: (OFF)
3. Enter the address in Table 5 with the keyboard.

CAUTION

If you write ON data to activate a solenoid, *deactivate the solenoid immediately* by writing the OFF data. If you leave a solenoid activated for more than 10 seconds, you may have to replace the solenoid and/or its driver, due to overheating.

4. For each address listed in Table 5, do the following:
 - a. To activate the output:
 - Press DATA SET.
 - Enter the ON data with the keyboard.
 - Set R/W MODE to STATIC and back to (OFF).
 - b. To deactivate the output:
 - Press DATA SET.
 - Enter the OFF data with the keyboard.
 - Set R/W MODE to STATIC and back to (OFF).

Table 5 LED and Coin Counter Outputs

Address	On Data	Off Data	Output Device
9E86	FF	00	Left Coin Counter
9E85	FF	00	Right Coin Counter
9E80	FF	00	Trak-Ball™ Light



Troubleshooting the Watchdog Circuit

The Watchdog circuit will send continuous reset pulses to the microprocessor if a problem exists within the microprocessor circuit. If the self-test fails to run, it is a good practice to check the $\overline{\text{RESET}}$ line.

$\overline{\text{RESET}}$ is a microprocessor input (pin 40). In a properly operating game, reset should occur during power-up or when the $\overline{\text{RESET}}$ test point is grounded. A pulsing $\overline{\text{RESET}}$ line indicates that something is causing the microprocessor to lose its place within the program. Typical causes are:

1. Open or shorted address or data bus lines.

2. Bad microprocessor chip.
3. Bad bus buffers.
4. Bad ROM.
5. Bad RAM.
6. Any bad input or output that causes an address or data line to be held in a constant high or low state.

A pulsing $\overline{\text{RESET}}$ signal indicates a problem exists somewhere within the microprocessor circuitry. To aid in troubleshooting, the $\overline{\text{WDDIS}}$ test point can be connected to a ground test point to prevent resets. This will sometimes allow the Self-Test to be used to diagnose the failure during a RESET condition.

