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# STUN. RUNNER™

## Schematic Package

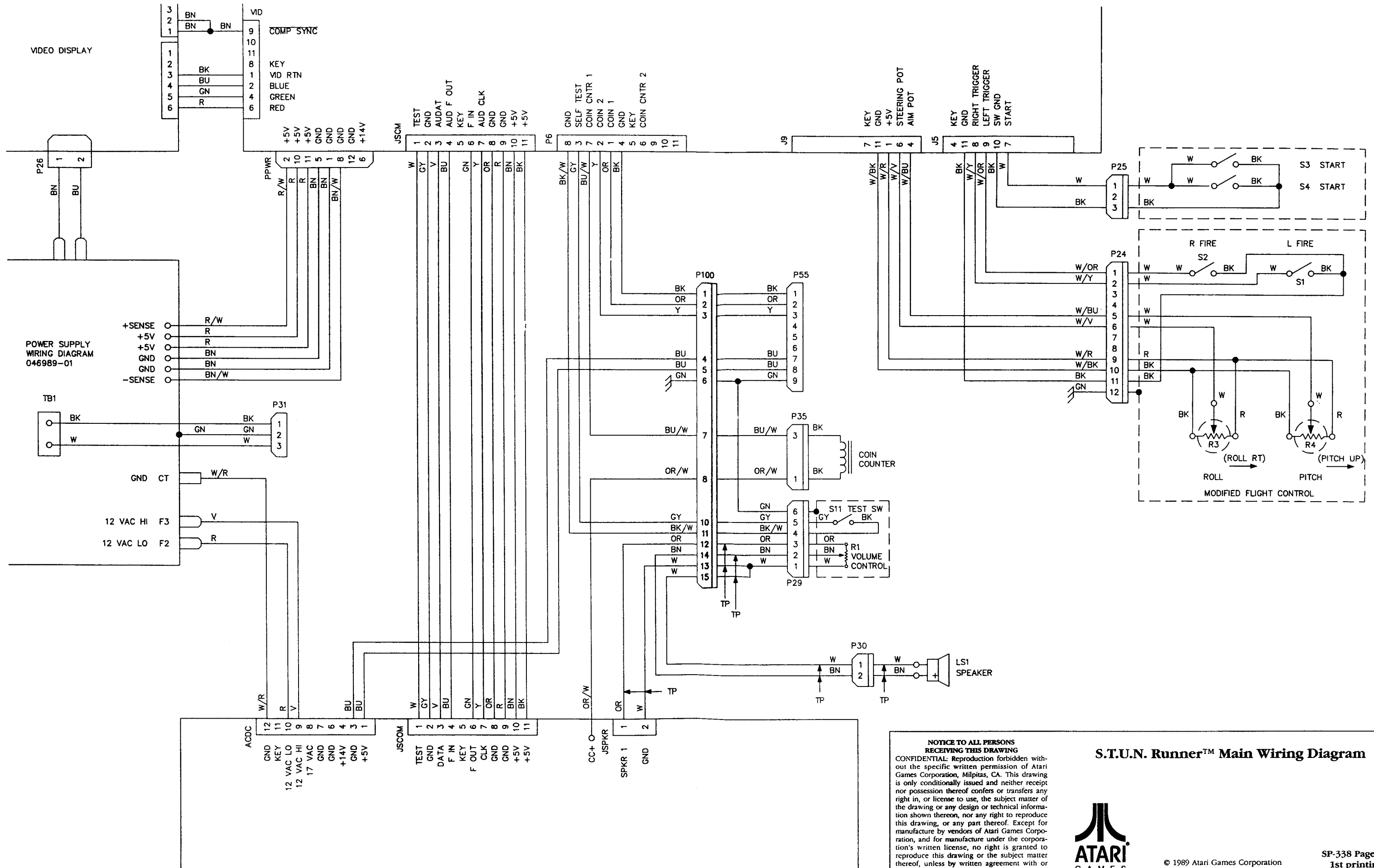
Supplement to Operator's Manual

### NOTE

This staple temporarily holds the schematic package together. Remove the staple before using these schematics.

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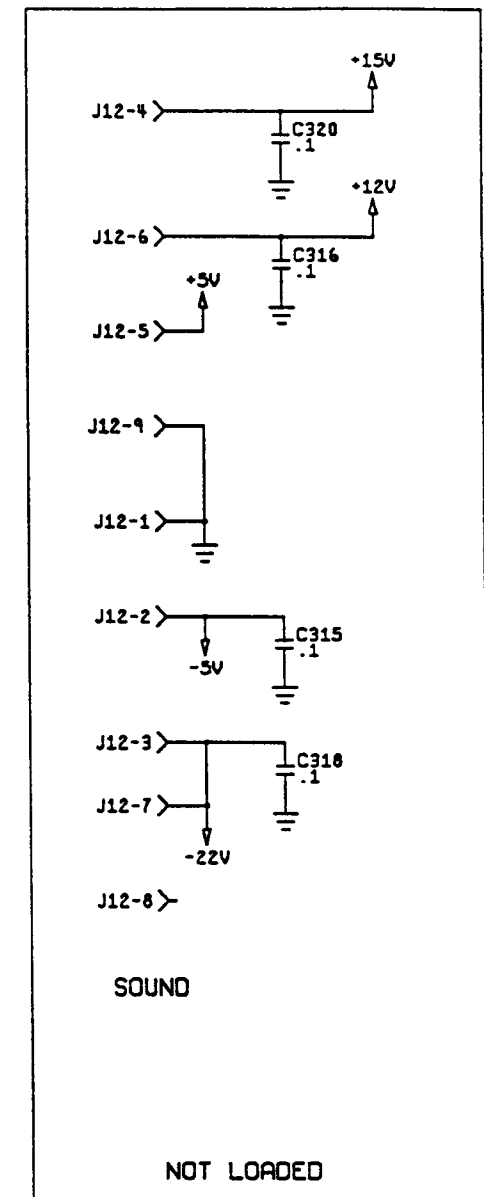
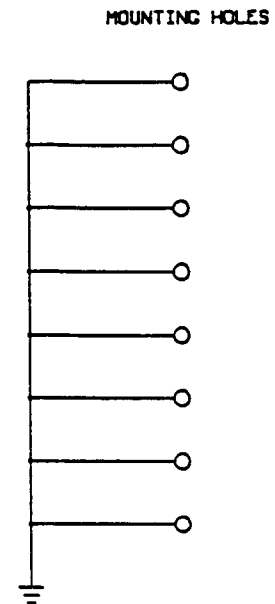
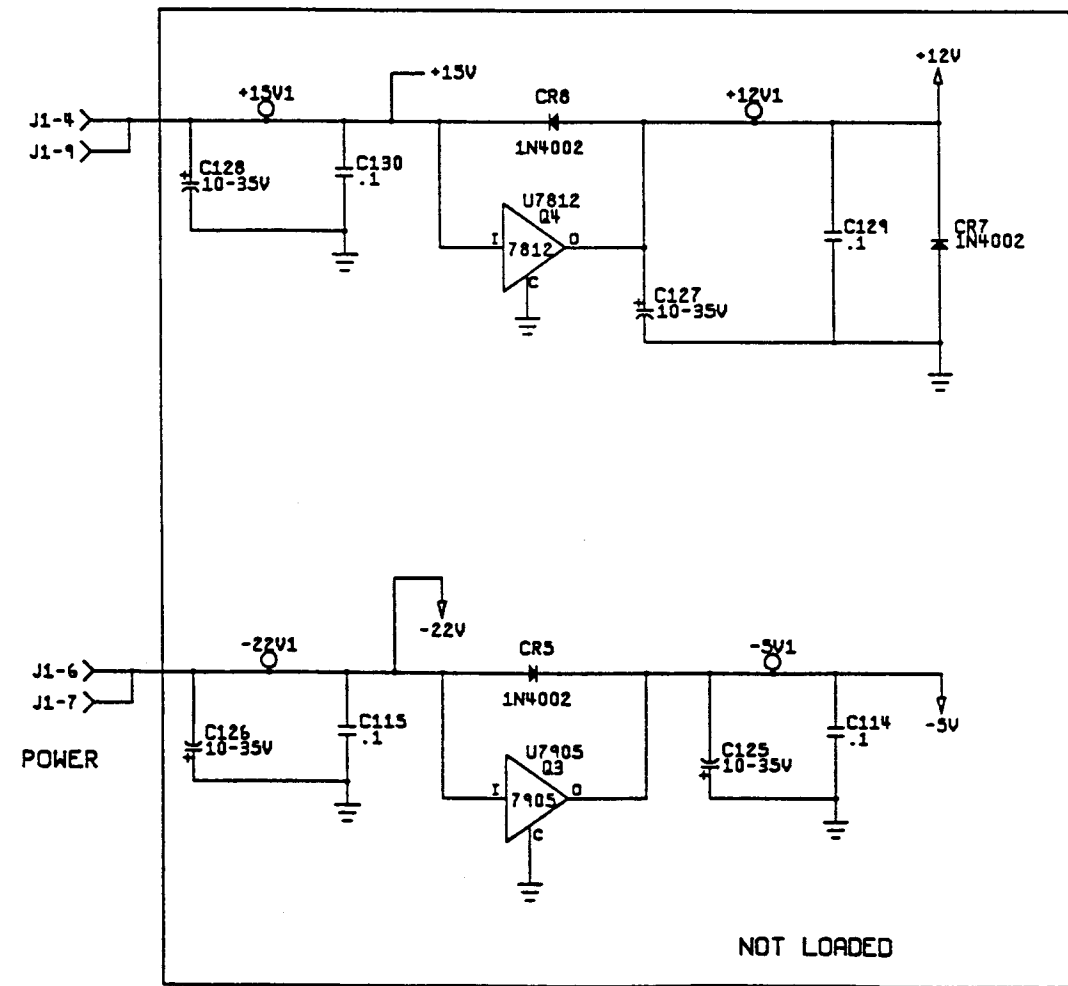
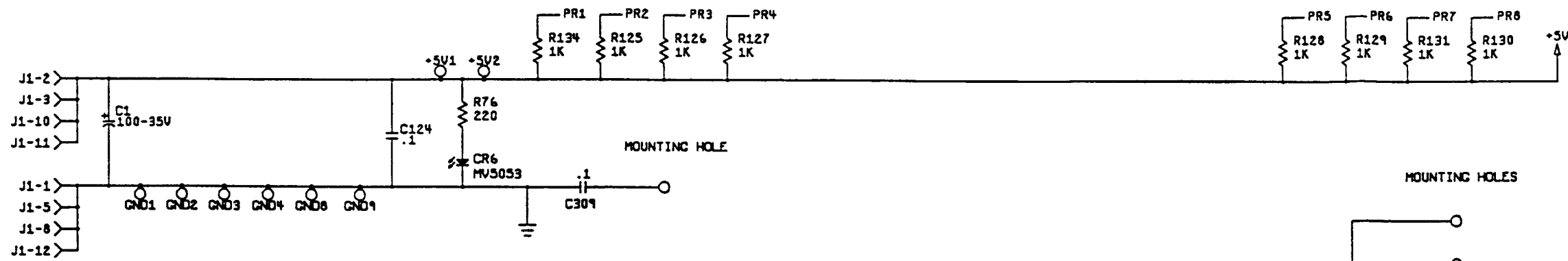
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**S.T.U.N. Runner™ Main Wiring Diagram**

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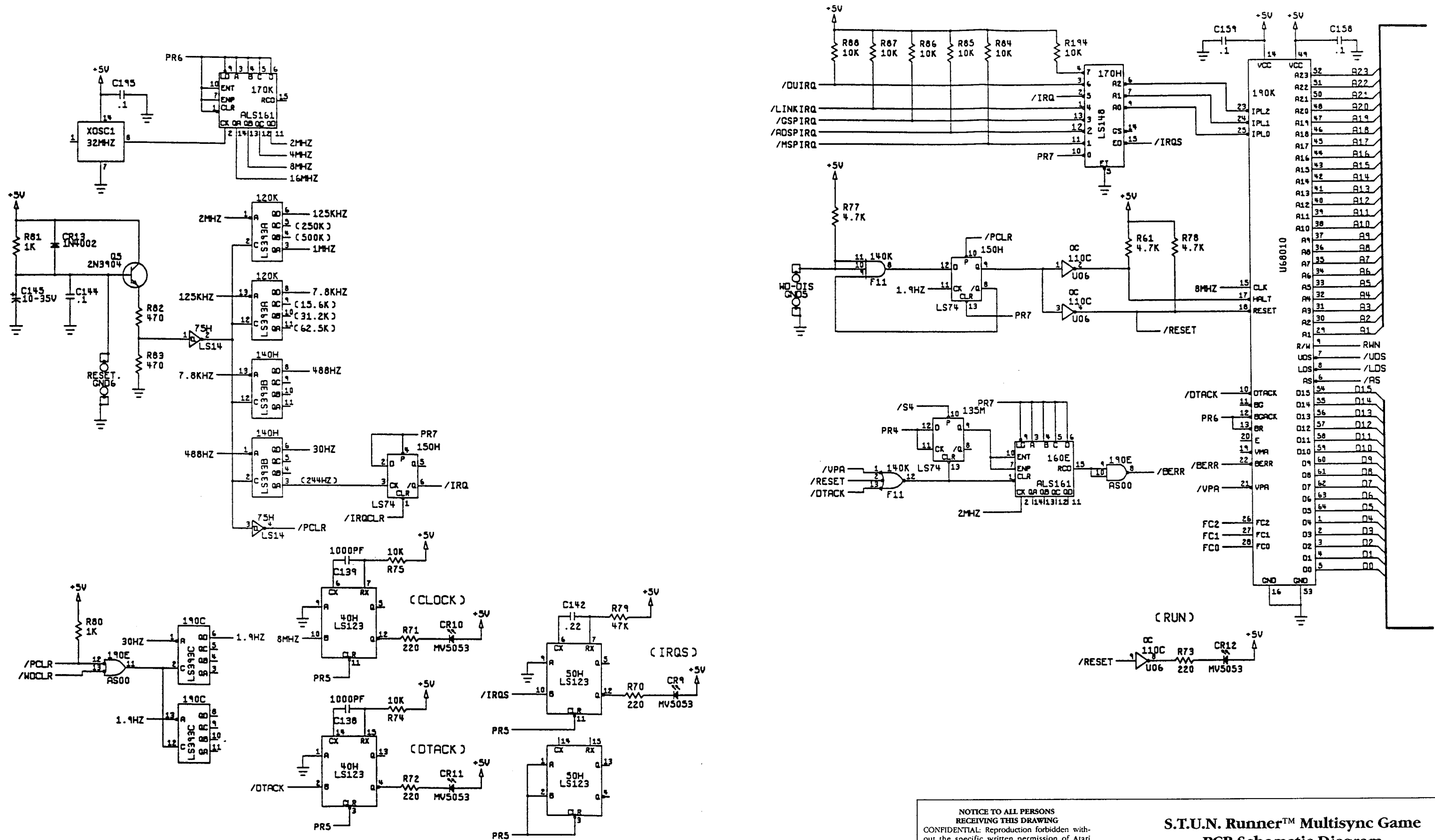
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**S.T.U.N. Runner™ Multisync Game  
 PCB Schematic Diagram**



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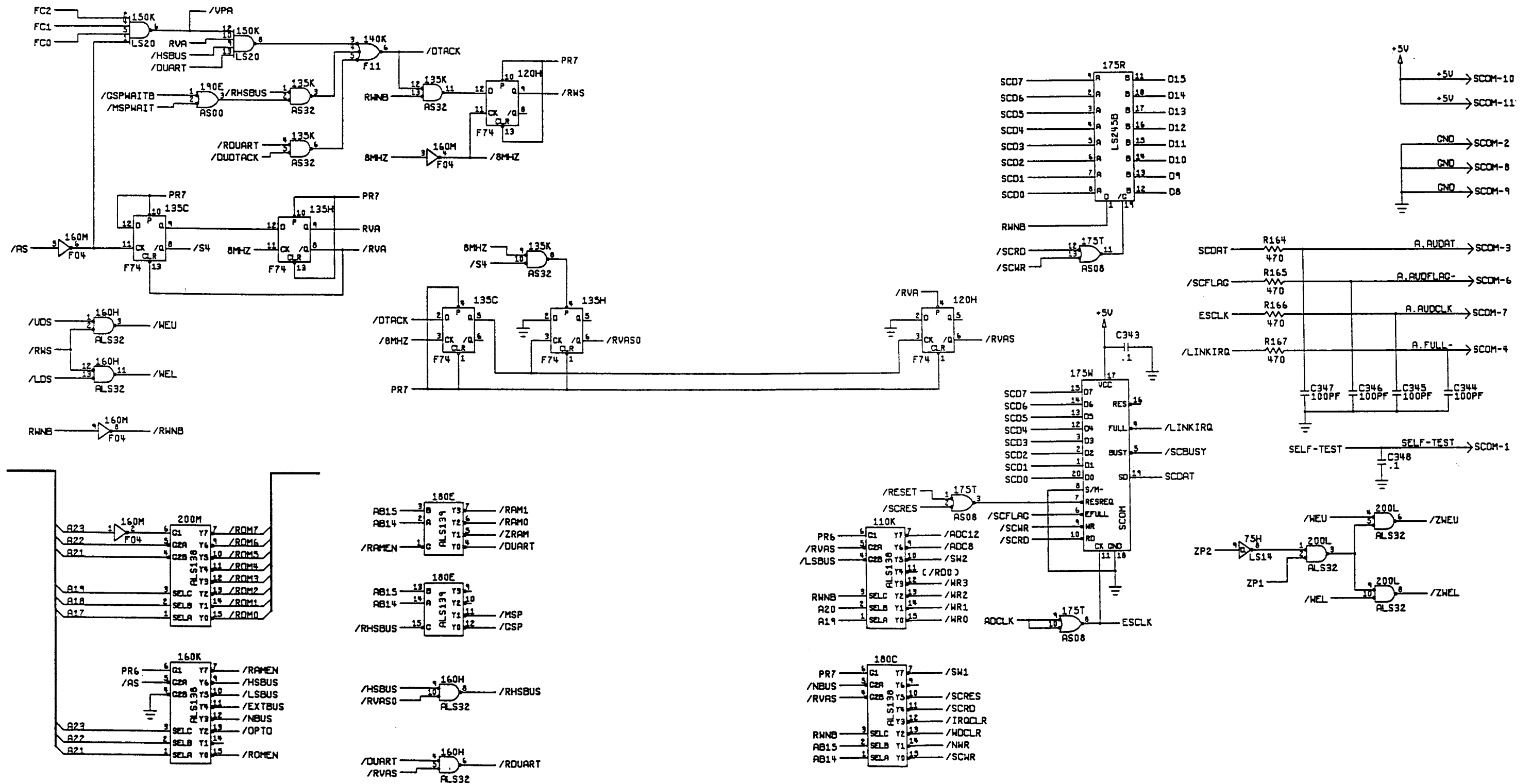
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**S.T.U.N. Runner™ Multisync Game  
PCB Schematic Diagram**



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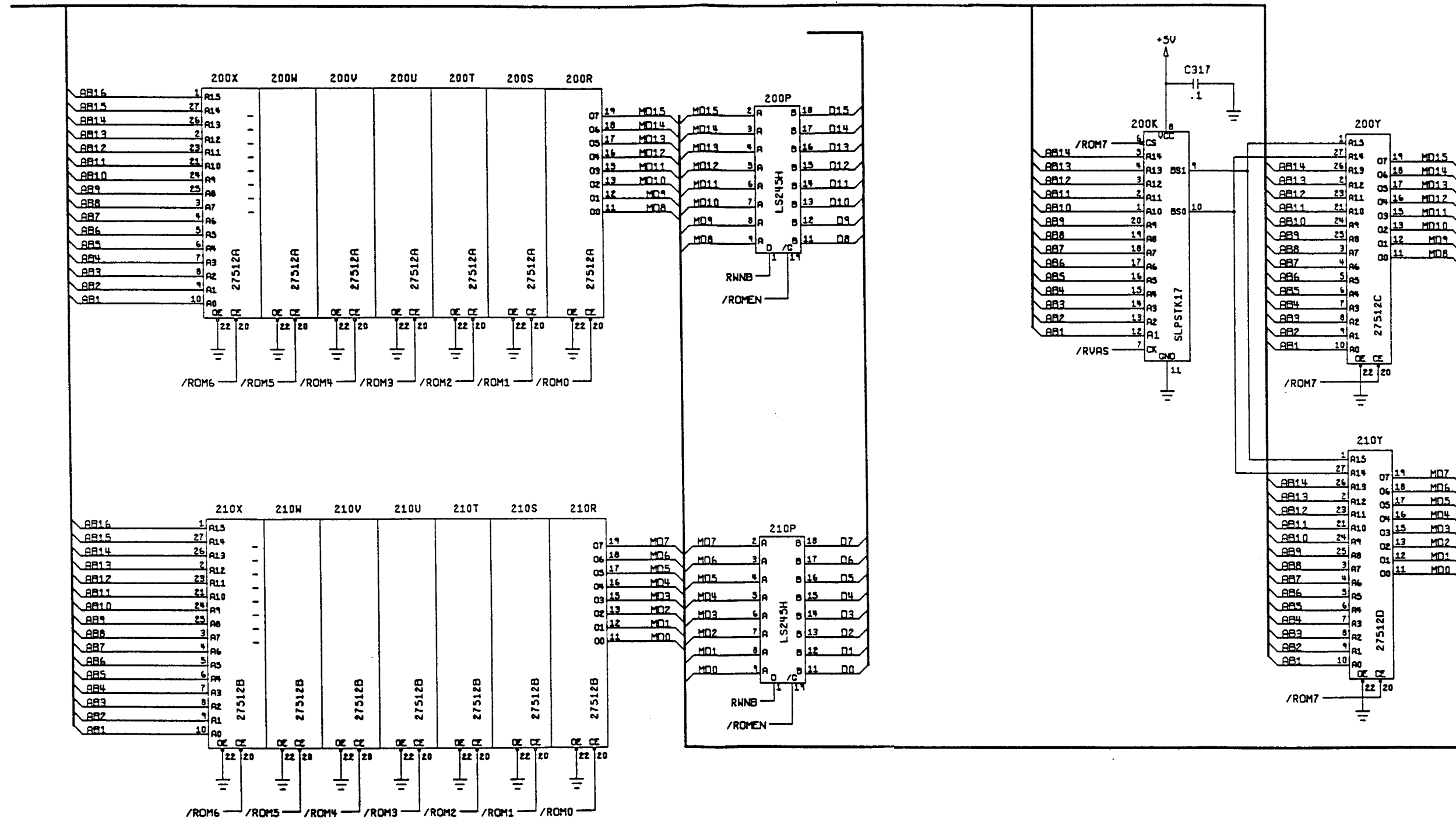
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PCB Schematic Diagram**

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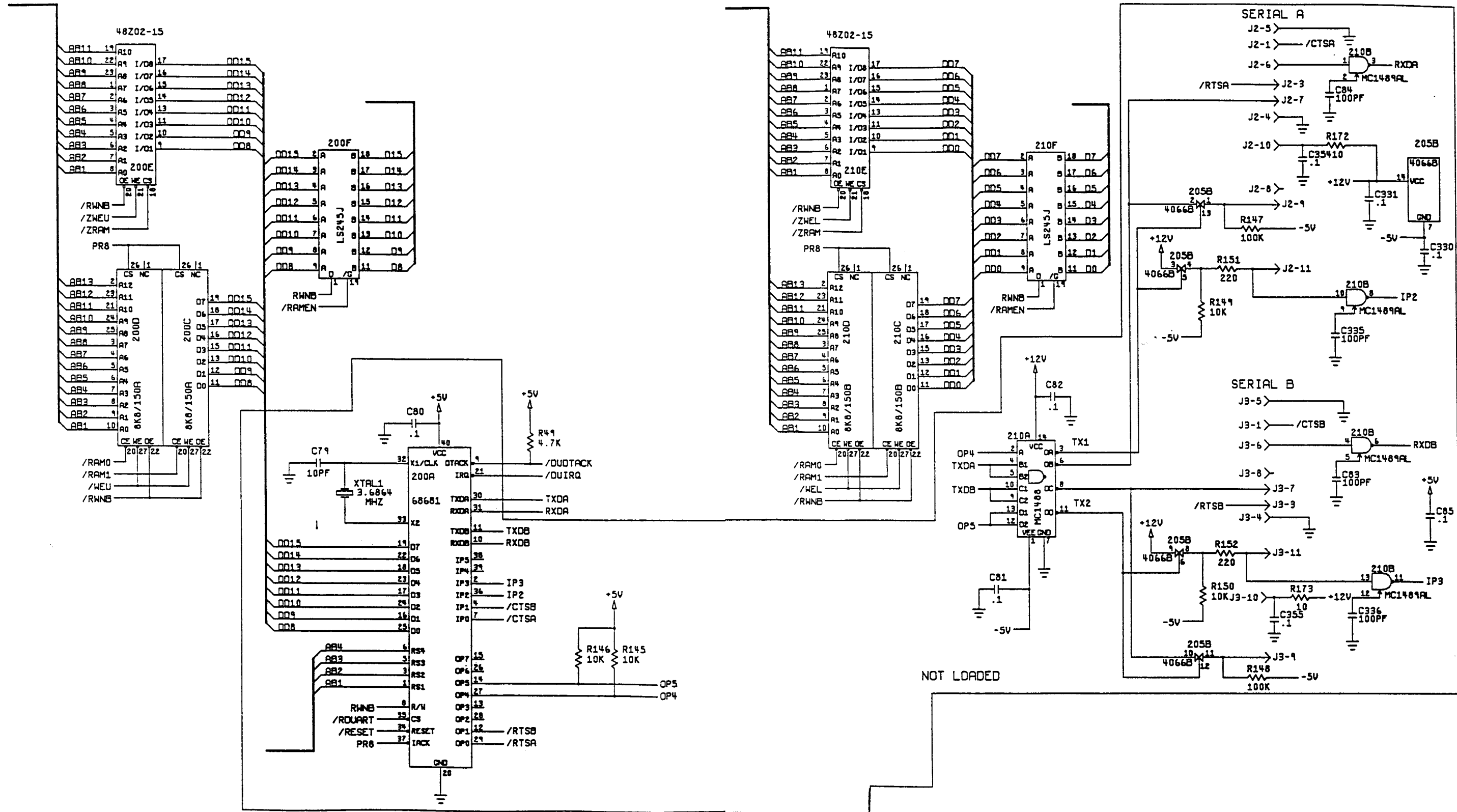
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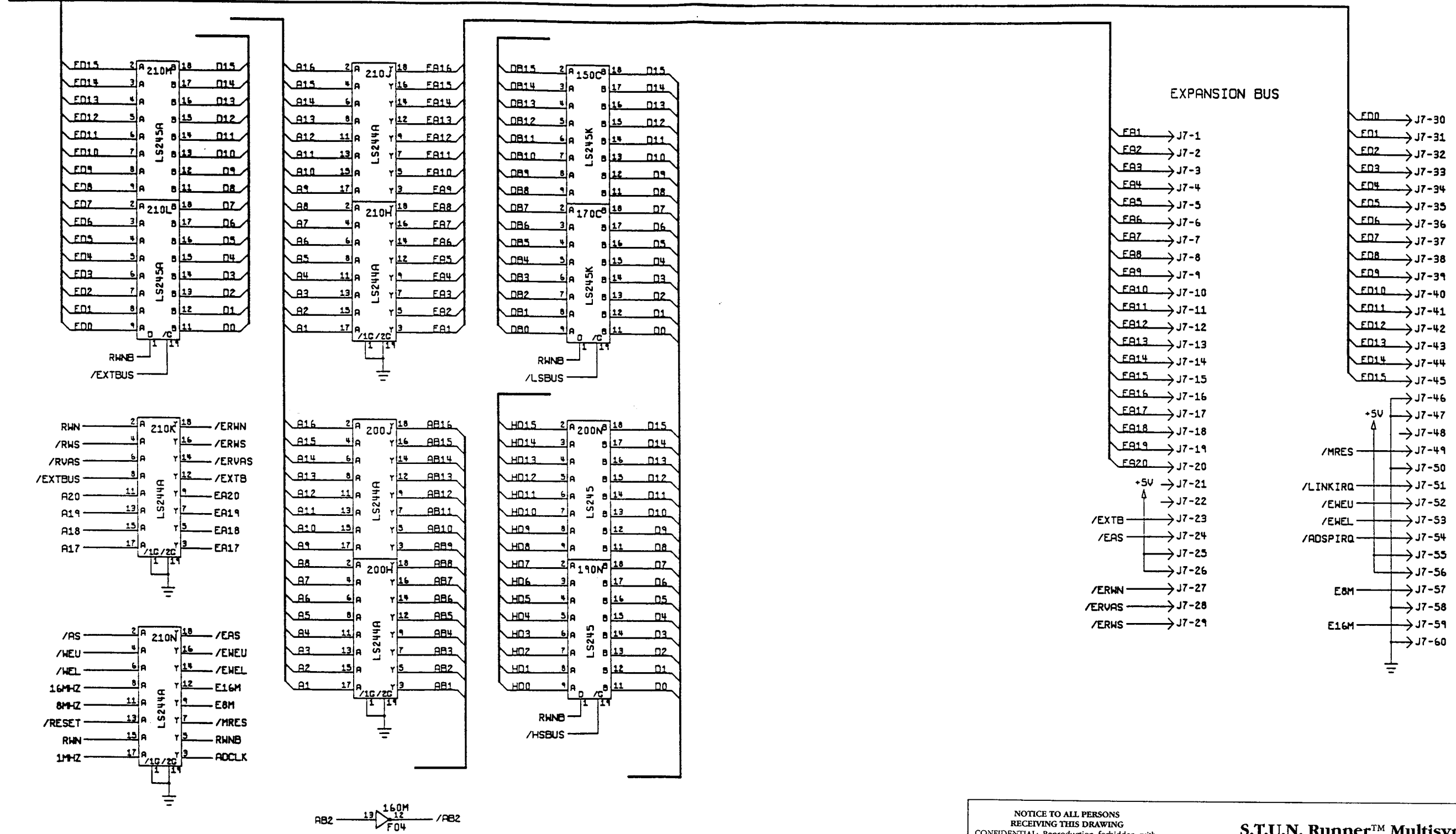
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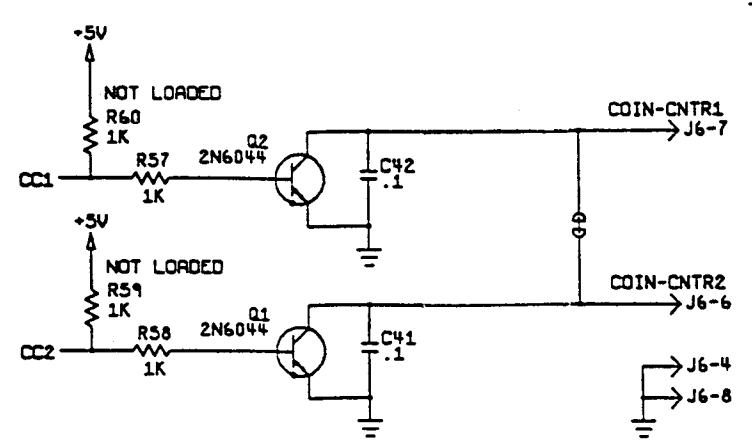
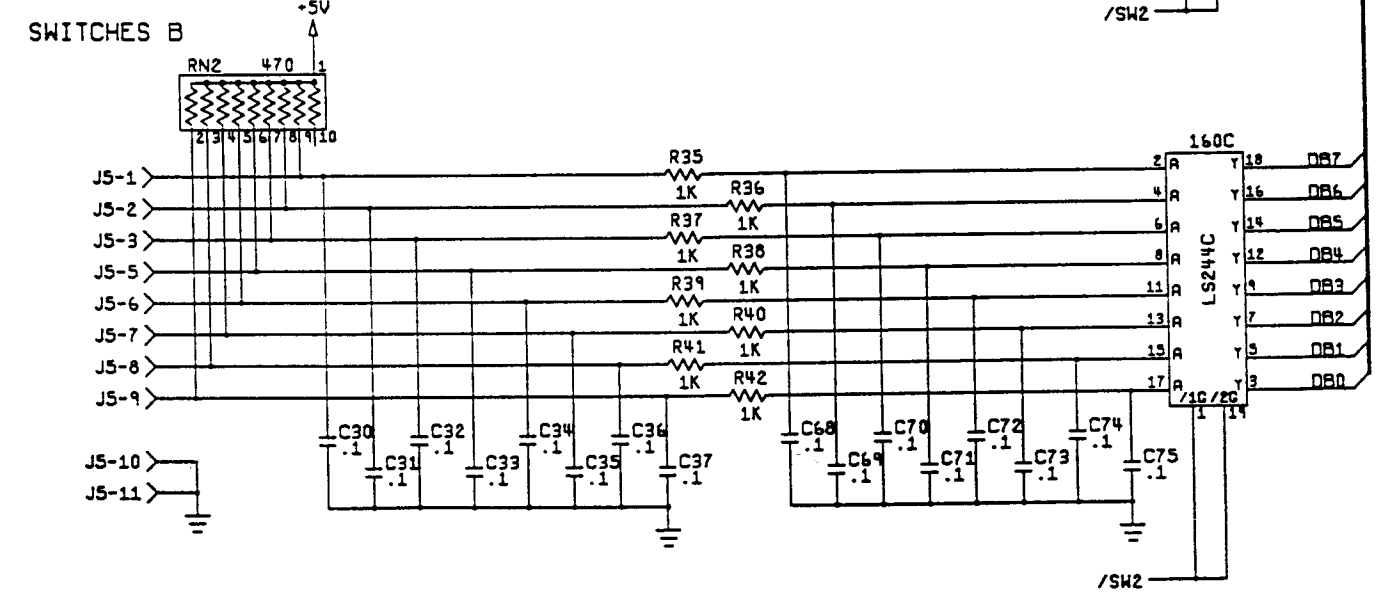
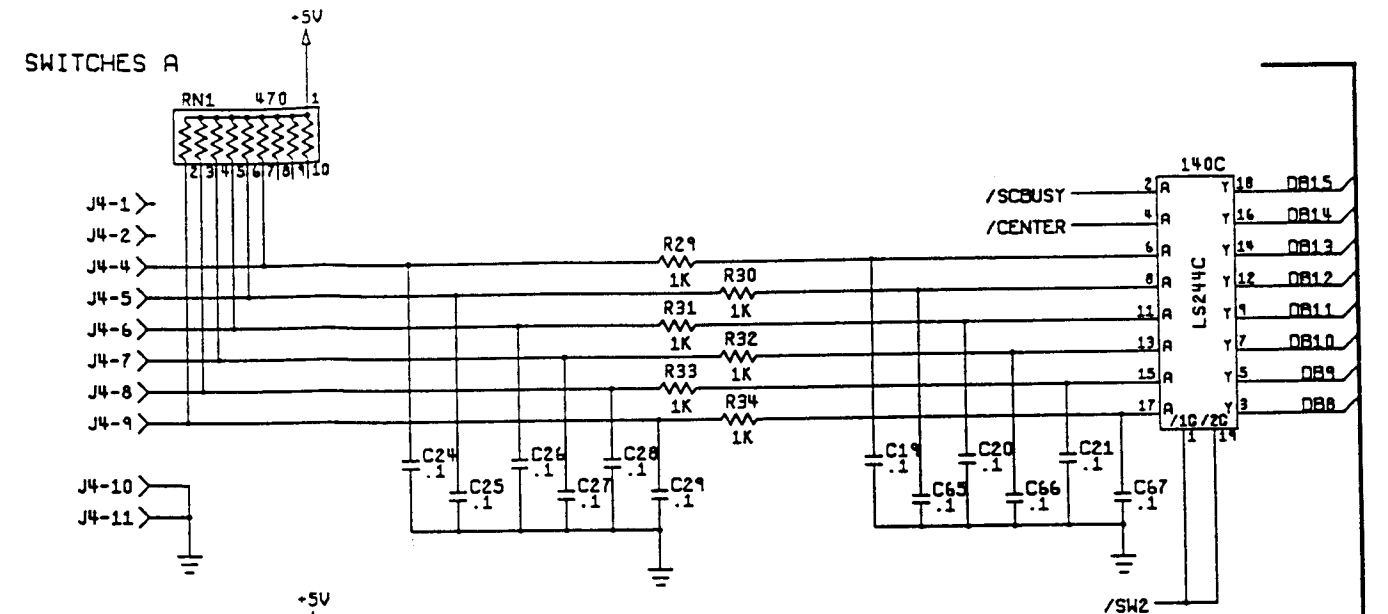
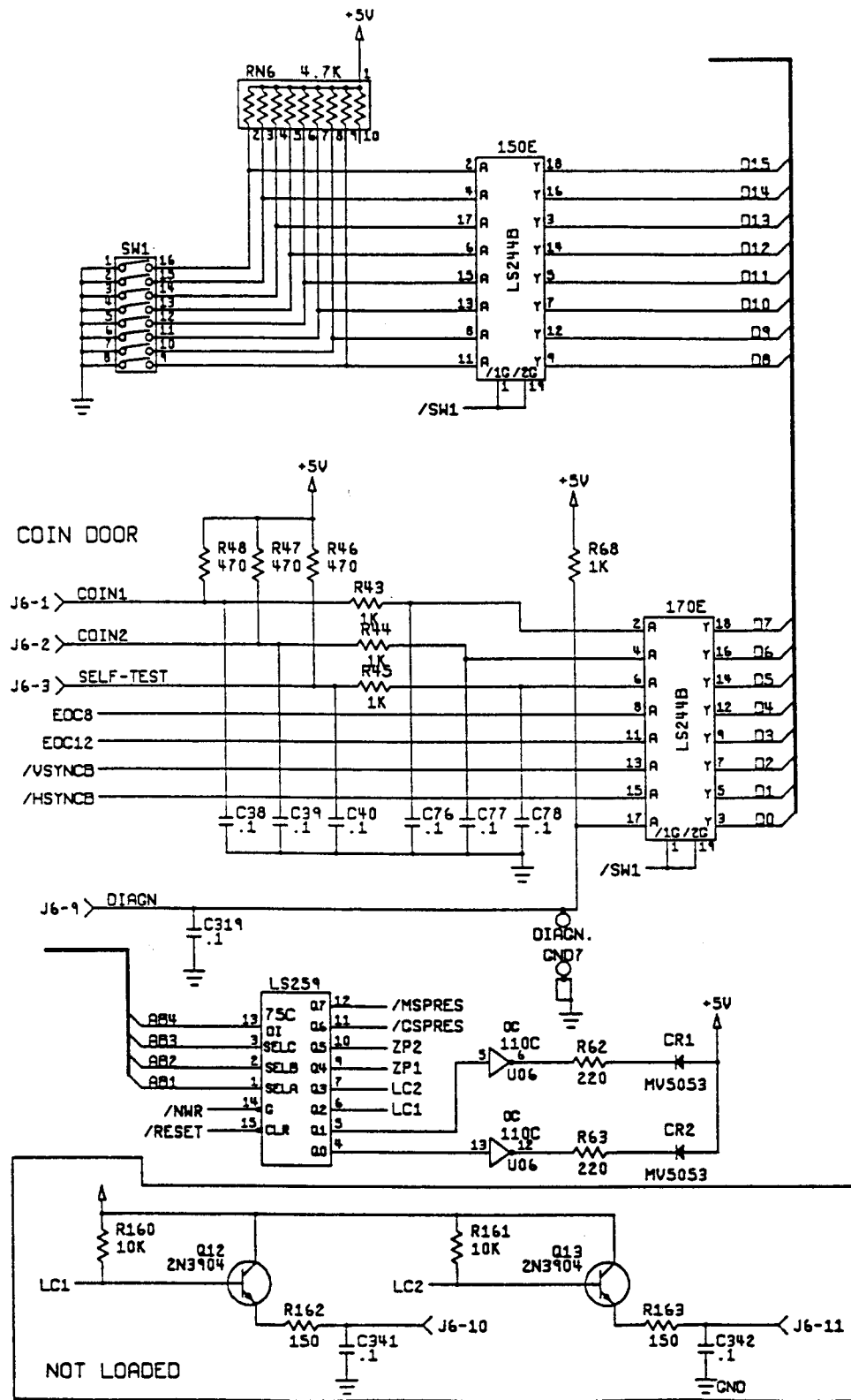
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 PCB Schematic Diagram**

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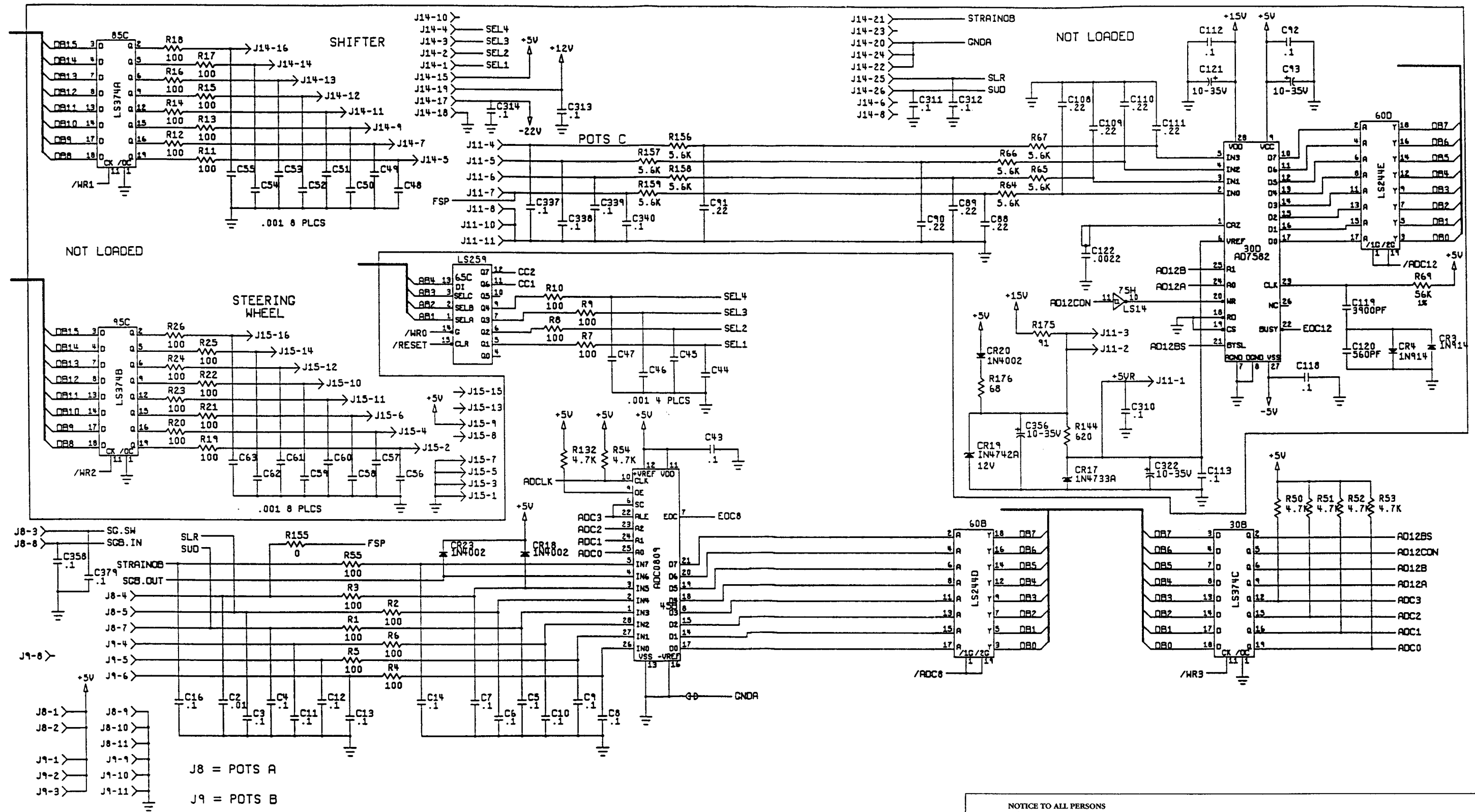
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**S.T.U.N. Runner™ Multisync Game  
 PCB Schematic Diagram**

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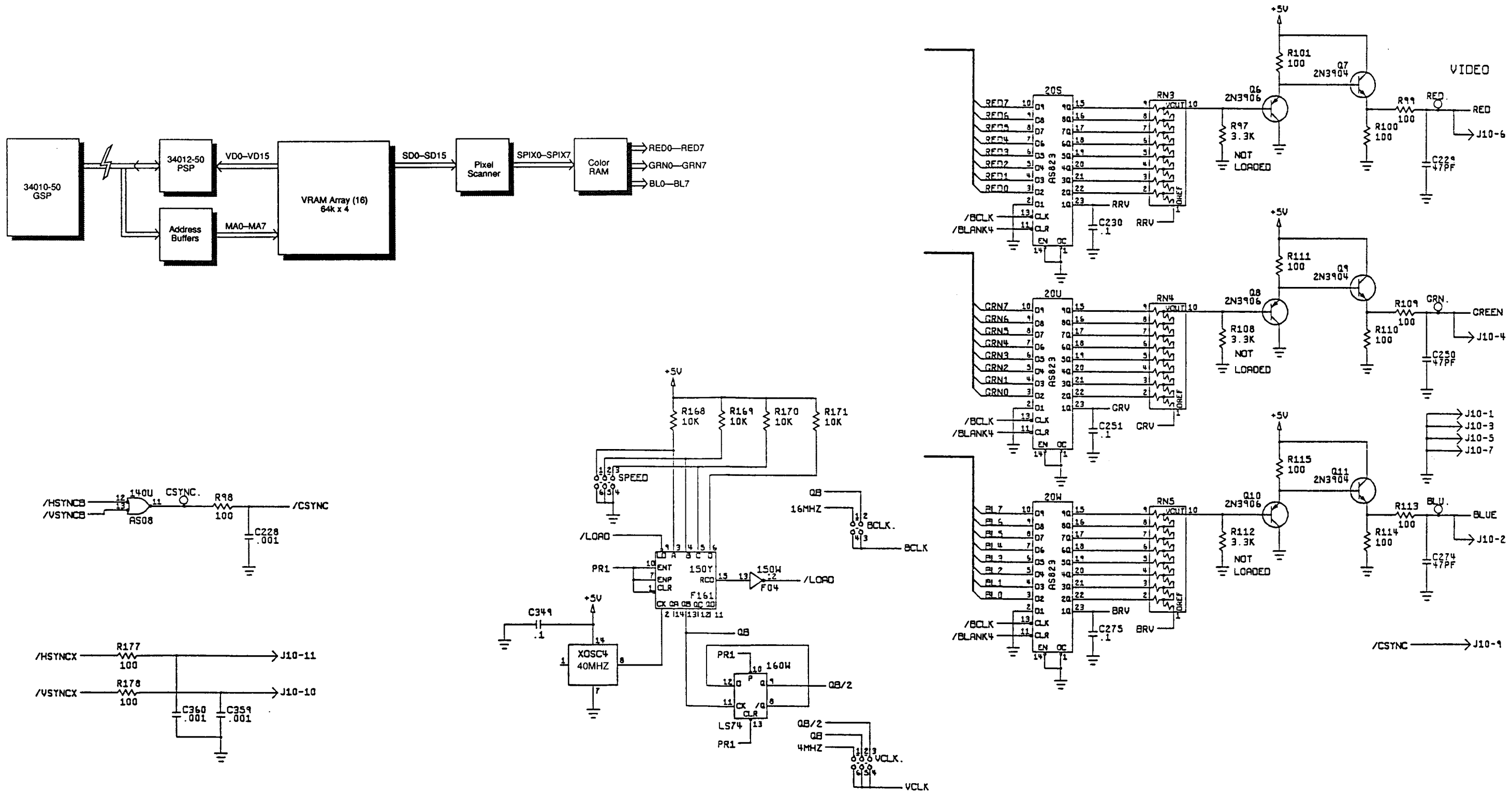
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**S.T.U.N. Runner™ Multisync Game  
 PCB Schematic Diagram**

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**Correct Jumper Settings for S.T.U.N. RUNNER**

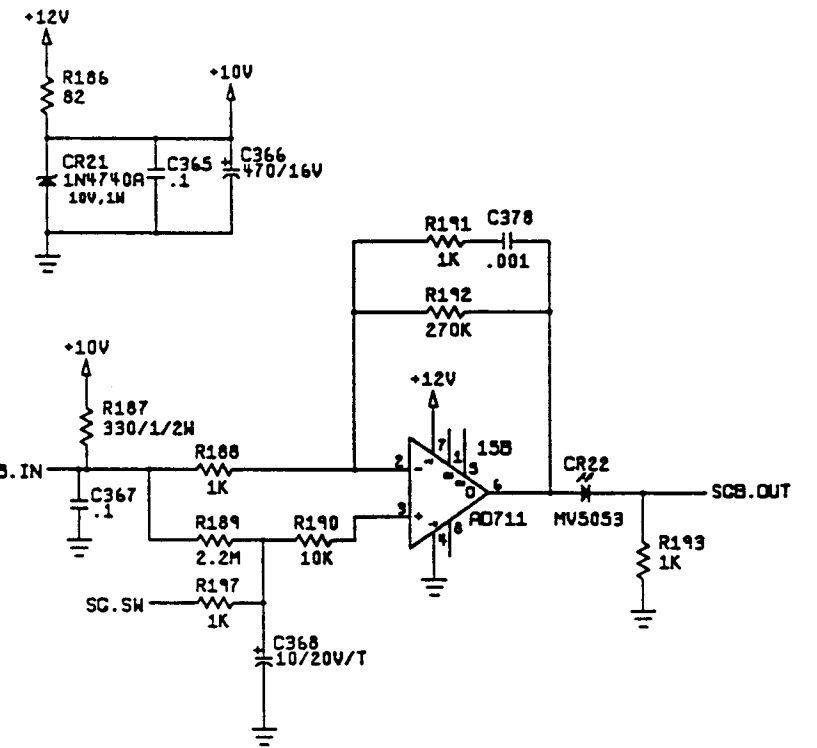
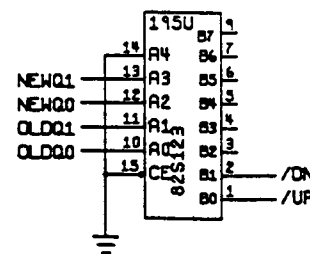
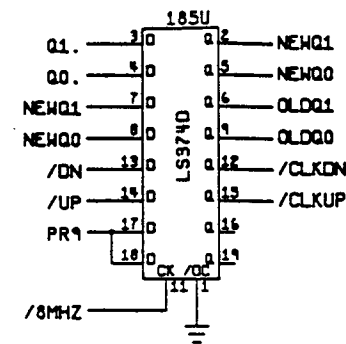
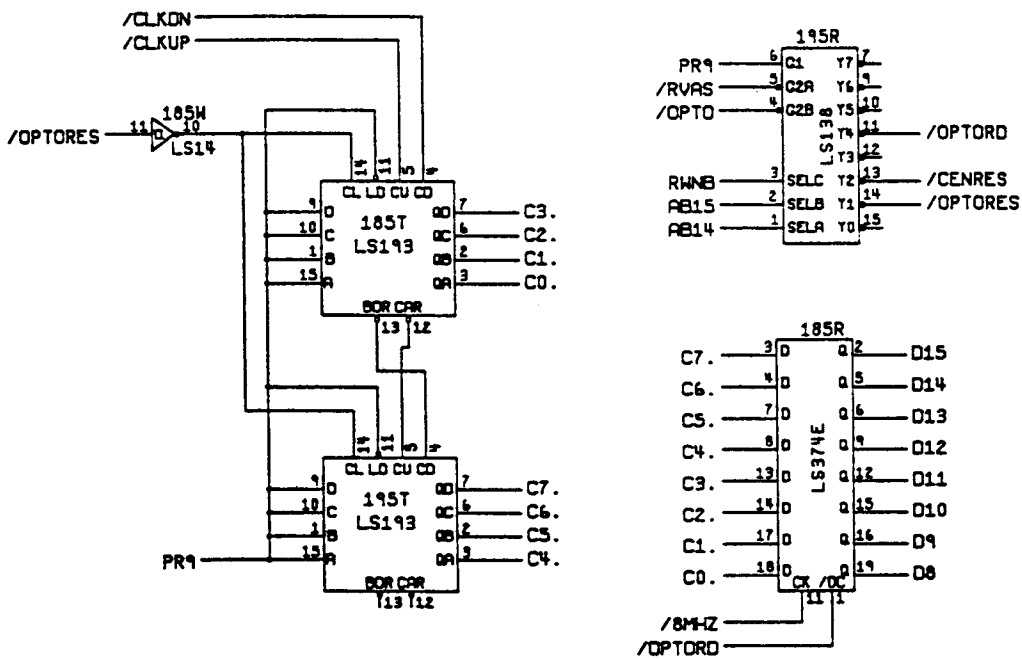
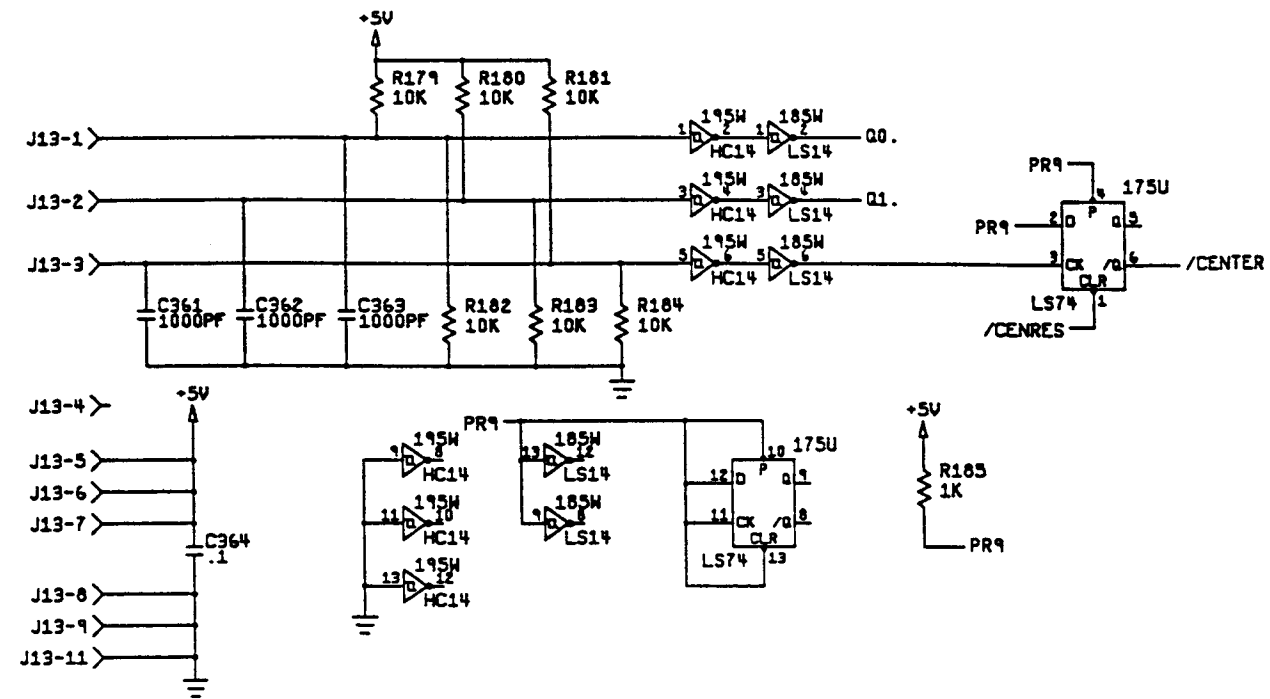
Jumper	Setting
Speed	A, B
BCLK	QB
VCLK	QB/2

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 PCB Schematic Diagram**

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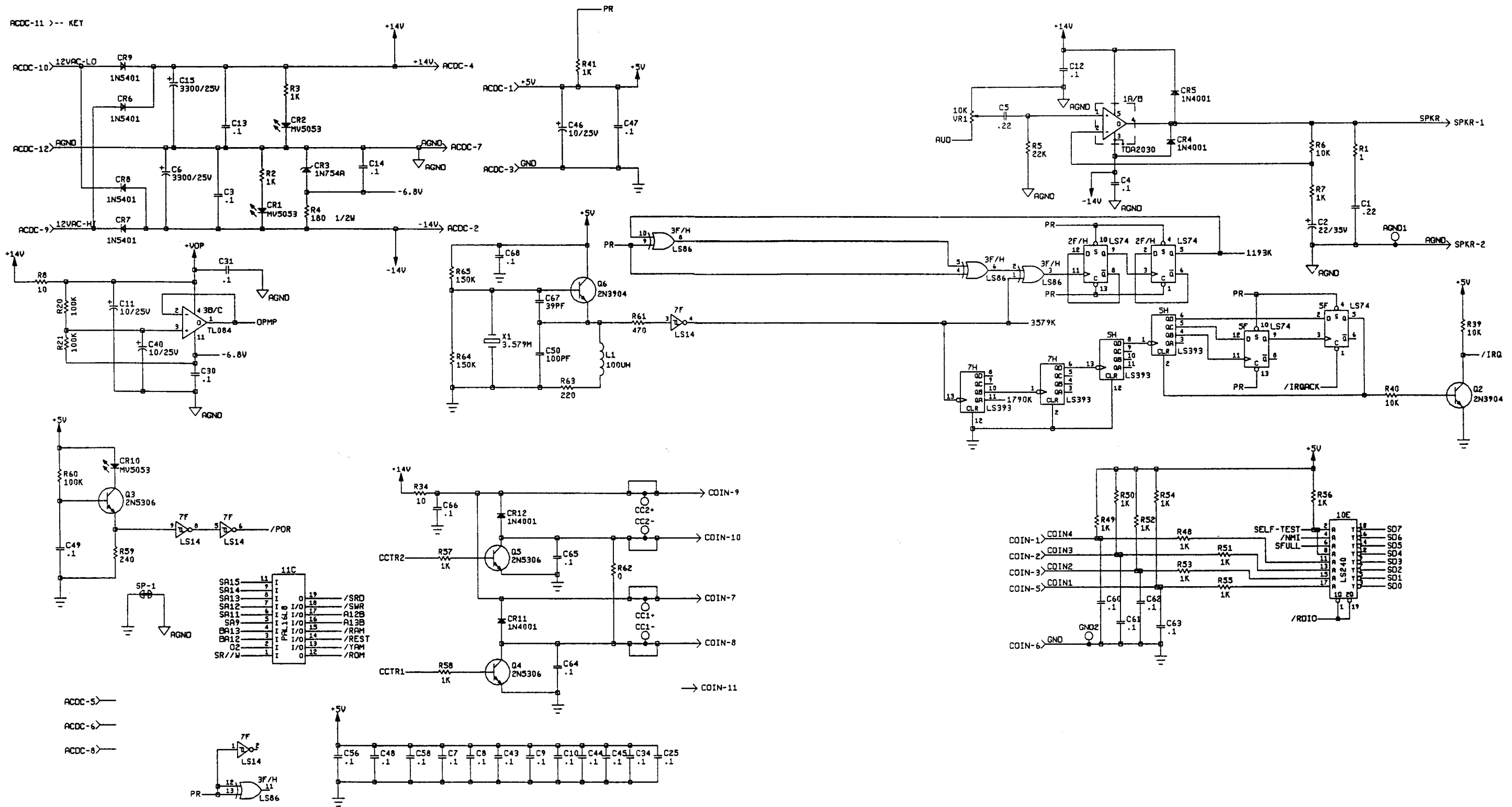
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**S.T.U.N. Runner™ Multisync Game  
PCB Schematic Diagram**



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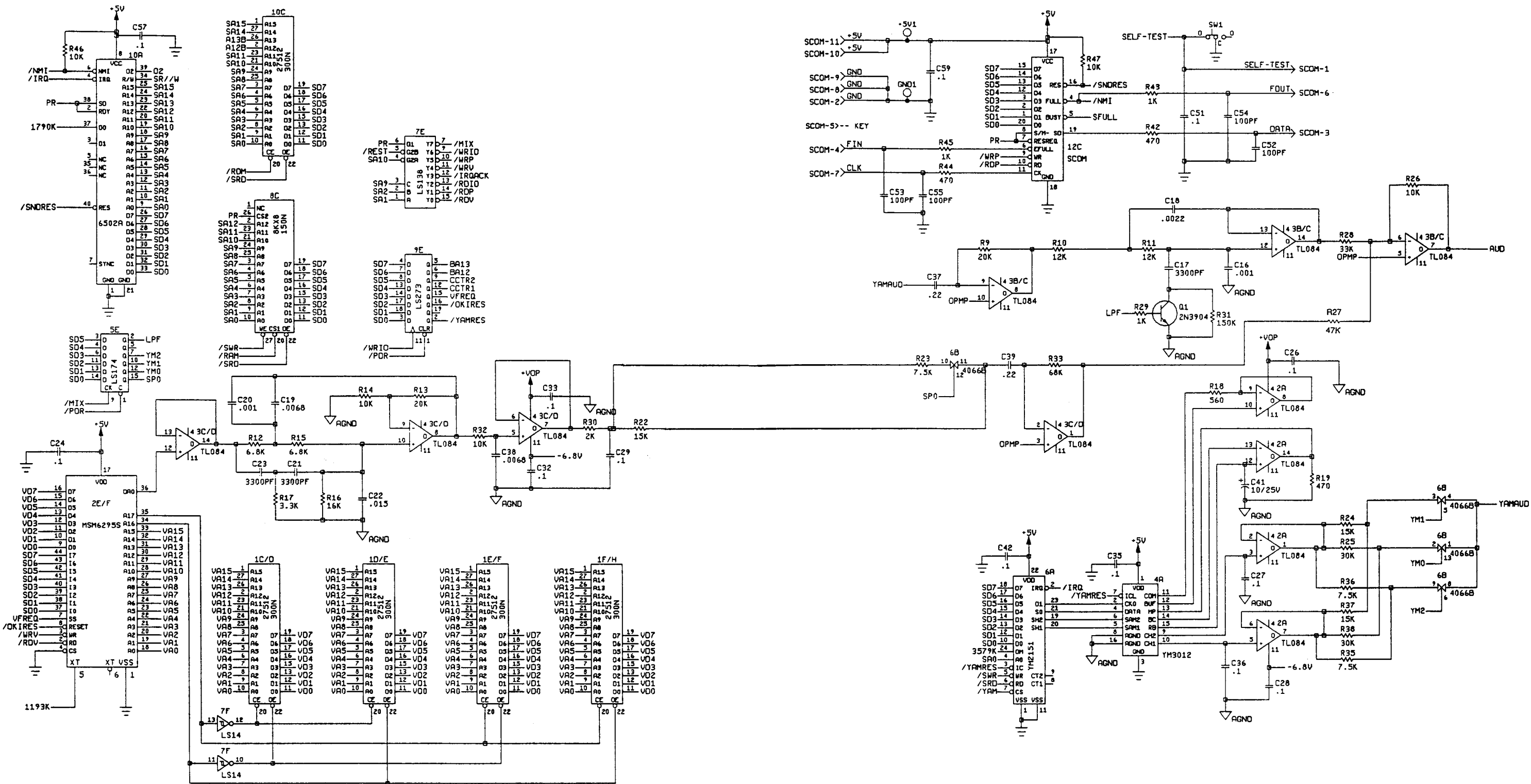
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**S.T.U.N. Runner™ SA Audio II  
PCB Schematic Diagram**



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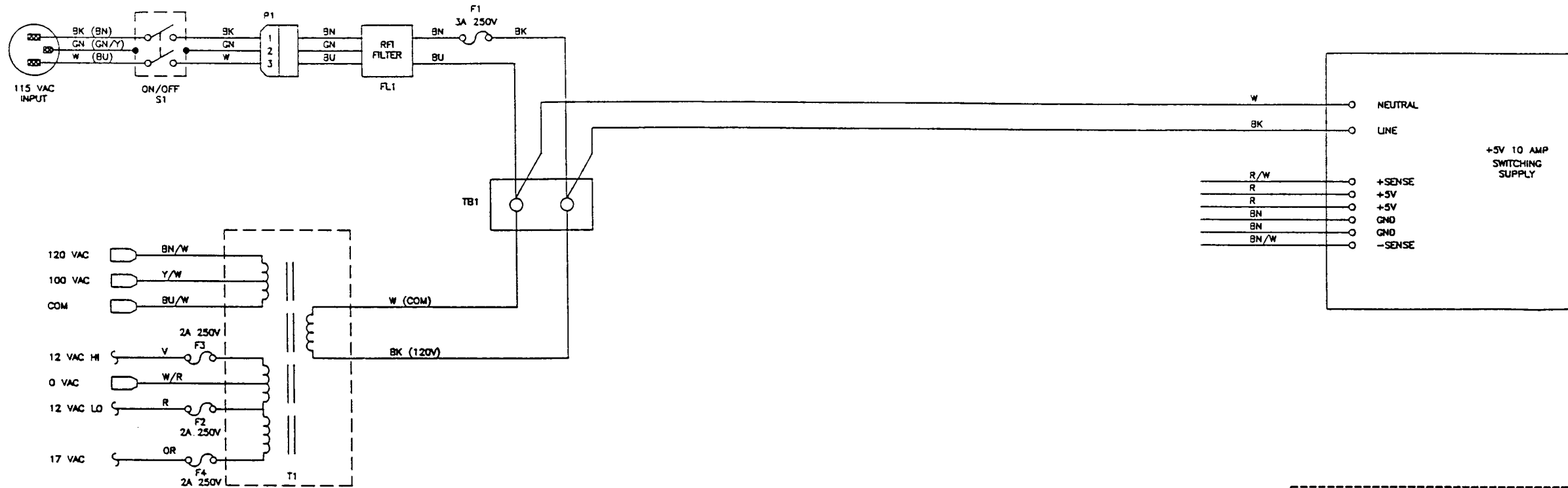
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PCB Schematic Diagram**

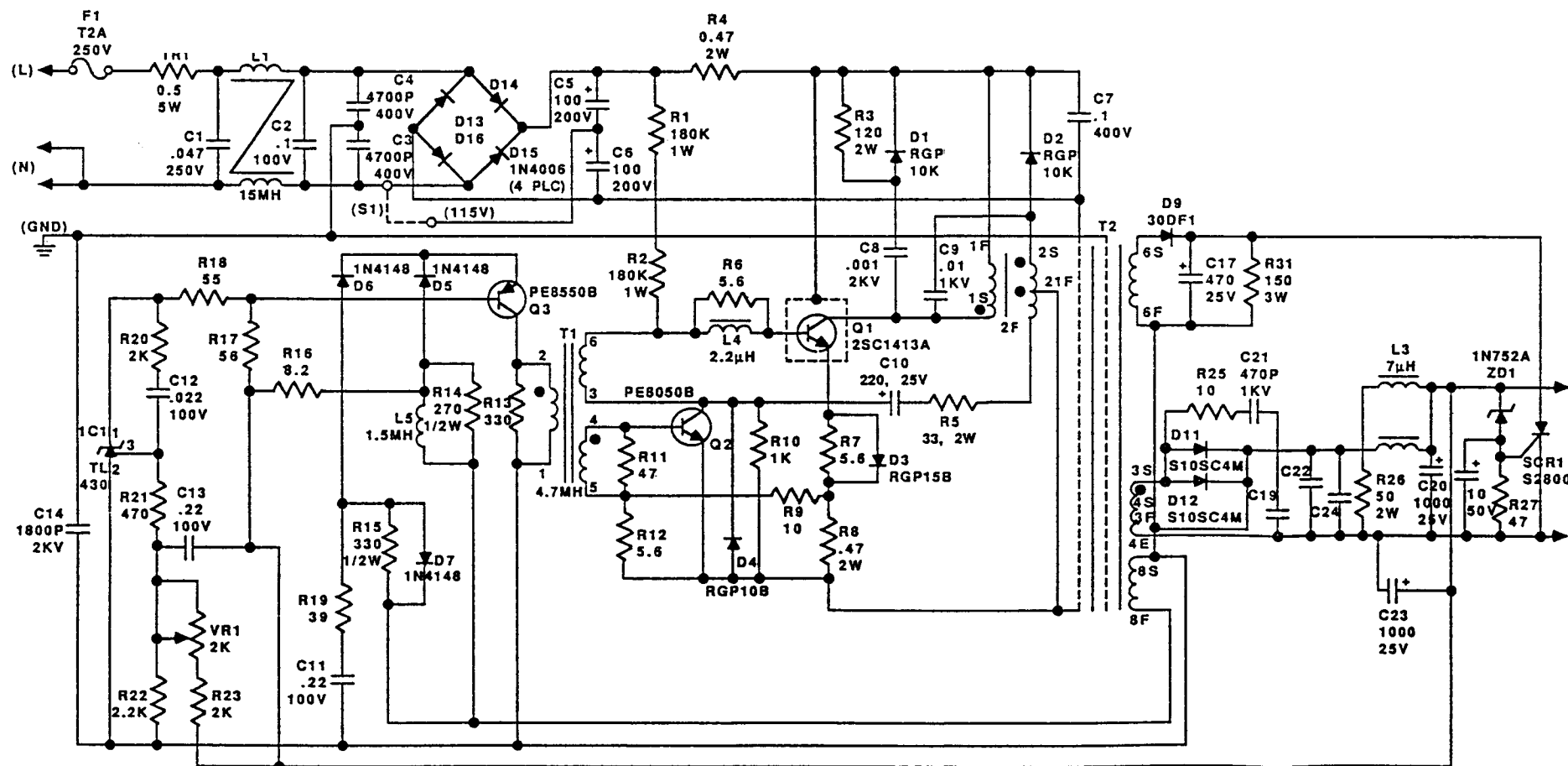


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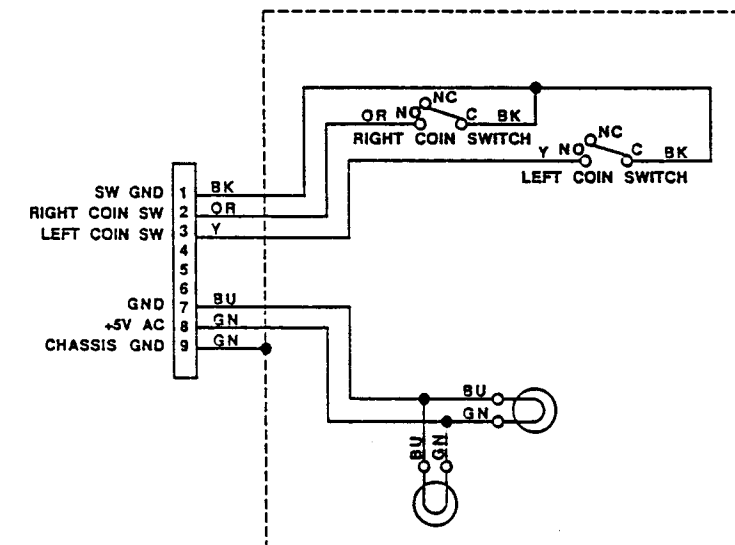


Switching/Linear Power Supply



Hitron 5V 10A Switching Power Supply

ATARI PART NO: 149003-003 (120V)  
149003-103 (240V)



Coin Door Wiring Diagram

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Switching/Linear Power Supply, Hitron 5V, 10A Switching Power Supply, and Coin Door Wiring Diagrams



# Main Board Memory Map

## ROMEN: Program ROM {Read Only}

00 0000 - 01 FFFF	ROM 0	128K Bytes
02 0000 - 03 FFFF	ROM 1	128K Bytes
04 0000 - 05 FFFF	ROM 2	128K Bytes
06 0000 - 07 FFFF	ROM 3	128K Bytes
08 0000 - 09 FFFF	ROM 4	128K Bytes
0A 0000 - 0B FFFF	ROM 5	128K Bytes
0C 0000 - 0D FFFF	ROM 6	128K Bytes
0E 0000 - 0F FFFF	ROM 7	128K Bytes

## OPTO: Optical Steering Wheel Reader

40 0000	{R}	OPTORD	Read the Optical Counter
40 4000	{W}	OPTORES	Reset the Optical Counter
40 8000	{W}	CENRES	Reset the Optical Center Flag

## NBUS

60 0000	{R/W}	SCOM	Serial Sound Communications
60 4000	{R}	SCRES	Reset SCOM IC (Address Strobe) READ ONLY
60 4000	{W}		Latches on Address Strobe (Data is ignored)

60 4000	LED 1 off
60 4002	LED 2 off

60 4004	LC1ON	Aux Control 1 High	(Latched)
60 4006	LC2ON	Aux Control 2 High	(Latched)
60 4008	ZP1WEN	ZeroPower RAM Enable 1	(Latched)
60 400A	ZP2WDIS	ZeroPower RAM Disable 2	(Latched)

60 400C	GSP Reset Low
60 400E	MSP Reset Low

60 4010	LED 1 on		
60 4012	LED 2 on		
60 4014	LC1OFF	Aux Control 1 High	(Latched)
60 4016	LC2OFF	Aux Control 2 High	(Latched)

60 4018	ZP1WDIS	ZeroPower RAM Disable 1	(Latched)
60 401A	ZP2WEN	ZeroPower RAM Enable 2	(Latched)
60 401C	GSP Reset High		
60 401E	MSP Reset High		

60 8000	{W}	WDCLR	Clear Watch Dog (Address Strobe)
60 C000	{R}	SW1	

D15	Option Switch 7	(*0* = on)
D14	Option Switch 6	(*0* = on)
D13	Option Switch 5	(*0* = on)
D12	Option Switch 4	(*0* = on)
D11	Option Switch 3	(*0* = on)
D10	Option Switch 2	(*0* = on)
D9	Option Switch 1	(*0* = on)
D8	Option Switch 0	(*0* = on)

D7	Coin Switch 1	(*0* = on)
D6	Coin Switch 2	(*0* = on)
D5	Self-Test Switch	(*0* = on)

# Main Board Memory Map, Contd.

D4	8 Bit ADC, End of Conversion = '1'
D3	12 Bit A/D, End of Conversion = '1'
D2	Vertical Sync from GSP
D1	Horizontal Sync from GSP
D0	Diagnostic Switch (*0* = on)

60 C000	{W}	Clear Timer IRQ (Address Strobe)
---------	-----	----------------------------------

## LSBUS

A0 0000	{R}	
A0 0000	{W}	WR0, Write to Shifter Interface and Coin Counters. Latches on Address Strobe (Data is ignored)

A0 0000	SEL 1 Low
A0 0002	SEL 2 Low
A0 0004	SEL 3 Low
A0 0006	SEL 4 Low
A0 0008	SEL 4 Low
A0 000A	
A0 000C	Coin Counter 1 off
A0 000E	Coin Counter 2 off

A0 0010	
A0 0012	Coin Counter 1 on
A0 0014	Coin Counter 2 on
A0 0016	
A0 0018	
A0 001A	
A0 001C	
A0 001E	

A0 0010	SEL 1 High
A0 0012	SEL 2 High
A0 0014	SEL 3 High
A0 0016	SEL 4 High
A0 0018	SEL 4 High
A0 001A	
A0 001C	
A0 001E	

A0 0010	Coin Counter 1 on
A0 0012	Coin Counter 2 on
A0 0014	
A0 0016	
A0 0018	
A0 001A	
A0 001C	
A0 001E	

A8 0000	{R}	/SW2, Sixteen External Switch Inputs
A8 0000	{W}	/WR1, Shifter Interface Latch, D8 - D15

B0 0000	{R}	/RD2, Read 8 Bit A/D
B0 0000	{W}	/WR2, Steering Wheel Latch, D8- D15

B8 0000	{R}	/RD3, Read 12 Bit A/D
B8 0000	{W}	/WR3, A/D Control

D8 - AD12BS	12 Bit A/D Byte Select
D7 - AD12CON	12 Bit A/D Write
D6 - AD12B	12 Bit A/D Address 1
D5 - AD12A	12 Bit A/D Address 0

D3 - ALE, SC	8 Bit A/D Write
D2 - ADDC	8 Bit A/D Address C
D1 - ADDB	8 Bit A/D Address B
D0 - ADDA	8 Bit A/D Address A

## RAMEN: Ram and DUART {R/W}

FF 0000	DUART
FF 4000	- FF 4FFE ZRAM (4K Bytes)
FF 8000	- FF BFFF RAM 0 (16K Bytes)
FF C000	- FF FFFF RAM 1 (16K Bytes)

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## S.T.U.N. Runner™ Memory Map

