

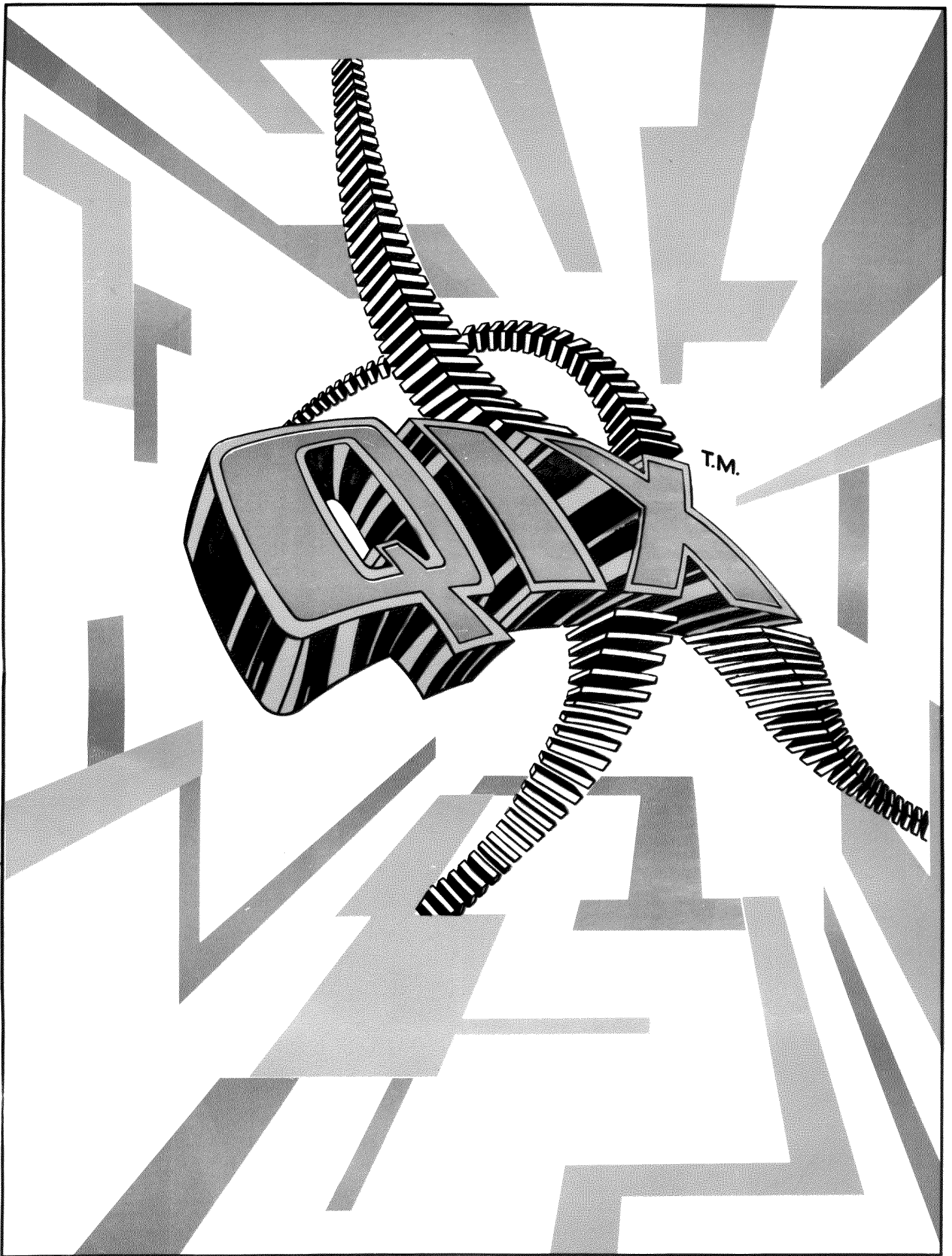
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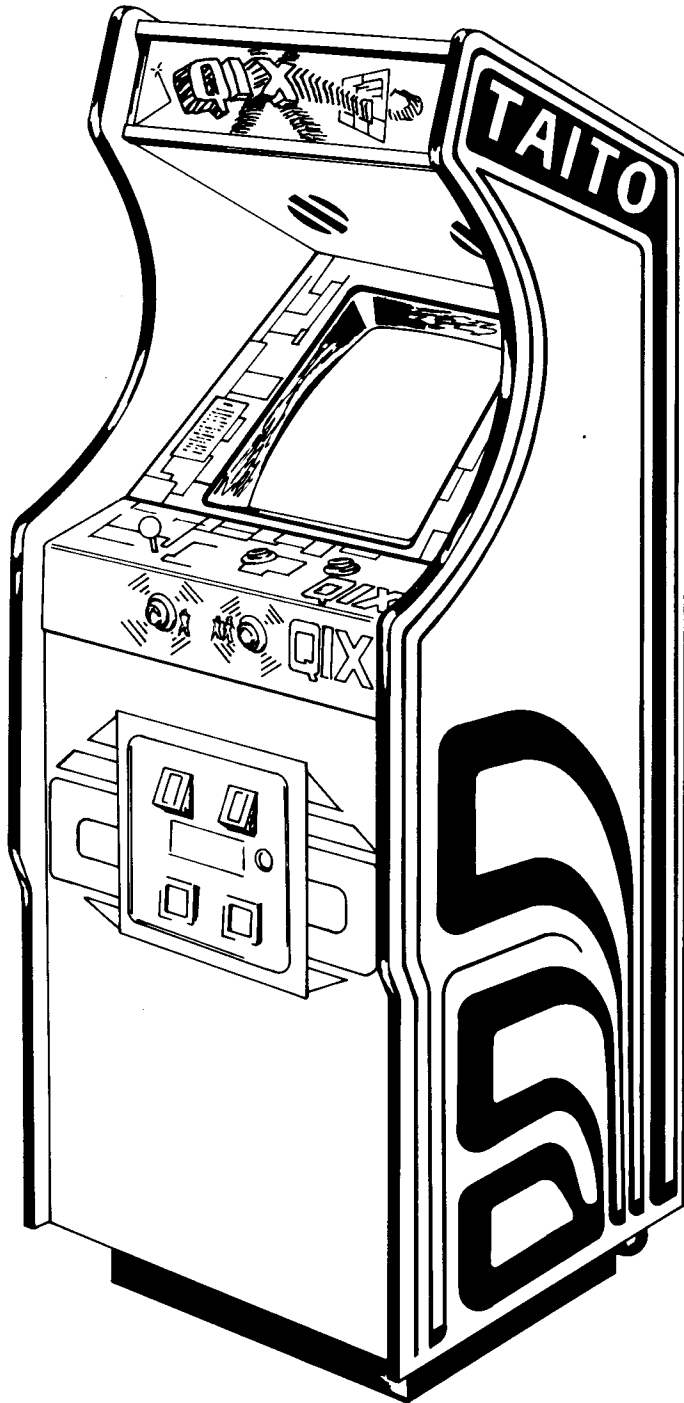


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“QIX”™

OPERATION, MAINTENANCE AND SERVICE MANUAL
Complete with Illustrated Parts Catalog

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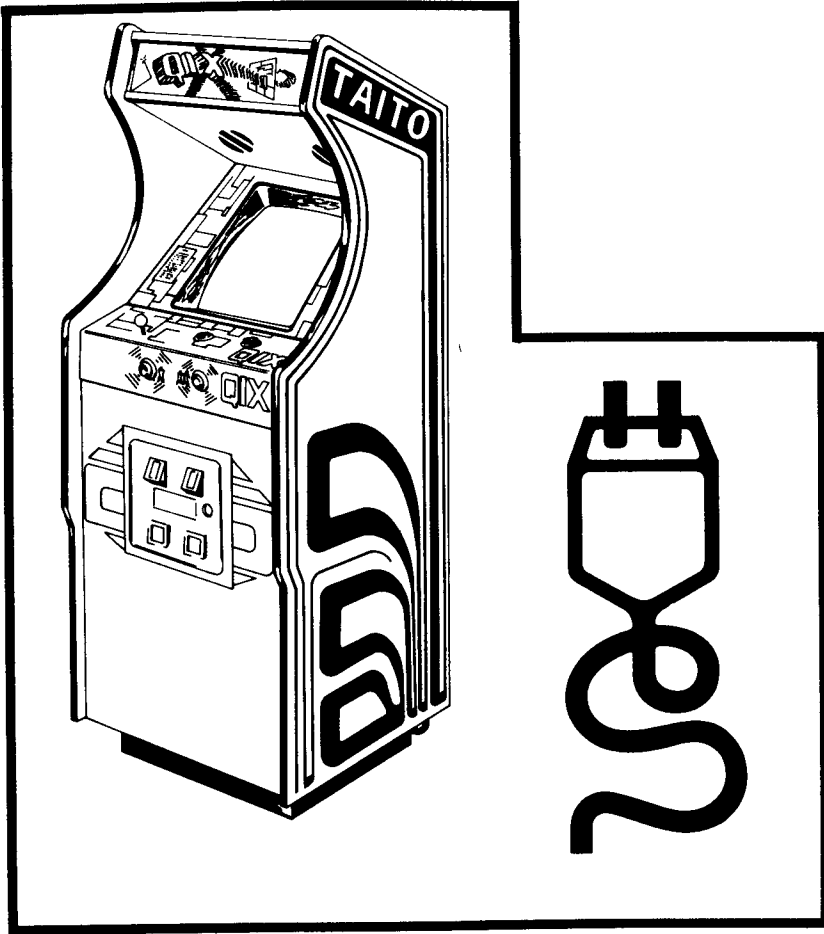
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Game Set-Up

1

1. GAME SET-UP

1.1 GAME FEATURES

TAITO AMERICA CORPORATION'S "QIX"™ upright game is housed in a highly serviceable cabinet designed with many added features.

By putting wheels on the cabinet, moving the game from one location to another is made much easier.

A larger security designed cash box has been incorporated into the design of this cabinet.

The Control Panel has a polycarbonate overlay, so cigarette marks and mars can be easily wiped clean. This overlay can be replaced if necessary.

The Marquee and Coverglass are made with fully Tempered Glass to minimize breakage.

The Back Service Door houses all the PC Boards for the system making servicing of the game, if needed, much easier.

Lighted Instructions are provided to further enhance the game and attract players, by making the Instructions easier to read.

TAITO AMERICA CORPORATION proudly presents our improved Self-Test capability, making servicing of the game easier, which keeps your game up and running with less down time.

1.2 INTRODUCTION

TAITO AMERICA CORPORATION'S "QIX"™ upright game is designed for one or two players.

The object of the game is to claim as much screen as possible without getting in the path of the spinning "QIX"™, while avoiding the traveling "Sparx"™. The game is set so a minimum prescribed area must be claimed before moving on to the next screen.

The "Sparx"™ are timed, which is indicated at the top of the video screen by a Red Timing Line. When the ends of the upper Red Line meet, more "Sparx"™ are released. When the alarm sounds these "Sparx"™ turn into Super "Sparx"™ and become more aggressive and follow the Marker on the outside boarder.

If while claiming your area, your Marker is caught in the Spiral Death Trap you will be destroyed, since you cannot cross your own path. If you hesitate and do not complete your area a fuse will be ignited and destroy the Marker. A Slow Draw and Fast Draw Button are provided. If you claim your area using the Slow Draw Button the point values will double.

1.3 GAME INSPECTION

TAITO AMERICA CORPORATION'S "QIX"™ upright game is shipped ready for operation, but a last visual check should be made to insure the game is in good condition. Please verify the following before turning the game on.

Check the exterior of the game for shipping damage, chips, dents, or broken parts.

Open the Rear Service Door and check for any interior damage.

- * Make sure there isn't any damage to the wiring.
- * Check Printed Circuit Boards, making sure there is no damage to the components.
- * Check fuses making sure they are firmly in their holders.
- * Check for loose foreign objects, especially metal objects which may cause electrical problems.
- * Check Plug-in Connectors making sure they are firmly in their sockets.
- * Check the Coin Door for any possible damage, especially the switches.

The Video Monitor is properly adjusted before shipping. If there are any adjustments necessary, refer to our Video Monitor Manual (72-00009-001). This Manual contains all the Manufacturers recommendations for adjusting the Video Monitor.

1.4 GAME PRE-INSTALLATION

The following precautions should be followed when installing the game.

- * Avoid rough handling of the game, the picture tube is fragile.
- * Install the game on a level surface.
- * Avoid installing the game where it may receive excessive sunlight or heat, to prevent the game from rising internal temperatures.
- * Do not install in a damp or dusty location.
- * For a short time after connecting the power to the game, the picture may be temporarily distorted.

The monitor's purity is affected by the earth's magnetic field, causing a variation of color. By turning the game on for 10 or 15 seconds and then off for 20 to 30 minutes the automatic degaussing circuit applies a degaussing field around the edges of the monitor. Doing this several times will correct the problem.

Another way to correct this problem is to purchase a degaussing coil or bulk tape eraser at any Electronics store. This will help to immediately demagnetize the Video tube.

CAUTION

Caution must be used with a degaussing coil so the magnetic field of the degaussing coil is not allowed to become too intense at any one place on the picture tube, thereby causing a localized color distortion.

If you move the game to another location after degaussing the problem may reappear.

Refer to Monitor Manual 72-00009-001 for details.

1.4.1 POWER REQUIREMENTS

TAITO AMERICA CORPORATION'S "QIX"™ game is shipped ready for operation at 120 or 240VAC, 60Hz with a power consumption of approximately 250 Watts.

The following line voltages may be selected:

- 100VAC ± 10% 50/60Hz
- 120VAC ± 10% 50/60Hz
- 200VAC ± 10% 50/60Hz
- 220VAC ± 10% 50/60Hz
- 240VAC ± 10% 50/60Hz

A voltage Programming Block is located on the primary side of the Transformer to compensate for high/low conditions. (See Figure 1-1).

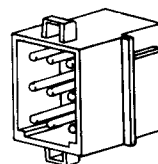


FIGURE 1-1 PROGRAMING PLUG

CAUTION

For safe operation it is recommended the cabinet be grounded. This game is equipped with a three conductor power cable. The third conductor is the ground conductor and when the cable is plugged into an appropriate receptacle, the game is grounded. The offset pin on the power cable's three-prong connector is the ground connection.

1.5 POWER ON/OFF SWITCH, INTERLOCK SWITCHES, MEMORY PROTECT SWITCH, SELF TEST SWITCH, VOLUME CONTROL, AND SERVICE OUTLET

To minimize the hazard of electrical shock while servicing the game a Power ON/OFF Switch, and two (2) Interlock Switches are provided. Two (2) Self Test Switches, a Volume Control and a Service Outlet have also been provided. (See Figures 5 and 6 for location of Switches).

1.5.1 POWER ON/OFF SWITCH, INTERLOCK SWITCHES

A Power ON/OFF Switch is located in the front of the game at the bottom left side of the cabinet. There are two Power Interlock Switches, one is located on the inside of the Coin Door, the other switch is located at the inside rear of the Service Door. This switch removes all the power from the game without unplugging it from the wall outlet. Power may be restored for servicing by pulling out on the Interlock Switch Buttons.

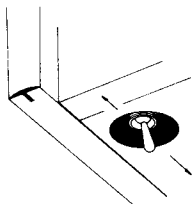


FIGURE 1-2 POWER ON/OFF SWITCH

1.5.2 MEMORY PROTECT SWITCH

The Memory Protect Switch is used to prevent erroneous writes to locations in the CMOS RAM which store the location program variables.

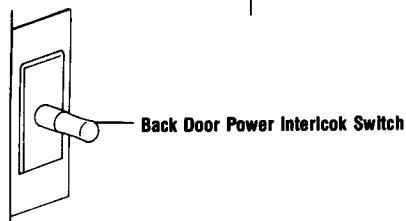
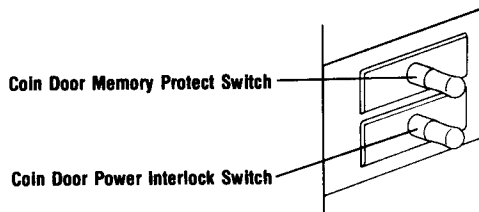


FIGURE 1-3 INTERLOCK SWITCHES & MEMORY PROTECT SWITCH

1.5.3 SELF TEST SWITCH

There are two (2) Self Test Switches and four (4) positions, located on the inside of the Coin Door. See Figure 5. The "QIX"™ game is capable of testing itself and provides data to demonstrate that the games circuitry and the controls are working properly. For further information on the Self Test Procedure refer to Section 1.8 and Figure 1-8.

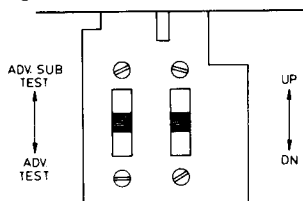


FIGURE 1-4 SELF TEST SWITCH

| SWITCH | FUNCTION |
|------------------|---|
| Up | Reset To Factory Setting (Reset Line Lit) Increment Number (Variable Line Lit) |
| Down | Decrement Number |
| Advance Sub-Test | Move To Next Line |
| Advance Test | Move To The Next Screen |

TABLE 1-1 SELF TEST SWITCHES

1.5.4 VOLUME CONTROL SETTING

The Volume Control Setting is located on the Data/Sound P. C. Board, which is on the rear of the Service Door. The volume increases when turned clockwise as indicated in Figure 1-5.

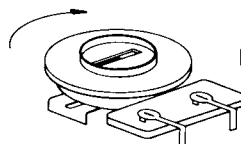


FIGURE 1-5 VOLUME CONTROL SETTING

1.5.5 SERVICE OUTLET

A Power Receptacle has been provided to further aid servicing. The voltage at this receptacle will be the same as the line voltage the game is set at.

1.6 ELECTRONIC ACCEPTORS

This game is equipped with the capability of using 12VDC Electronic Coin Acceptors, such as Third Wave Electronics, Model TW12 or equivalent. Power for these units may be obtained from the Coin Entry Lamp terminals which provide 12VDC.

1.6.1 COIN METER

This game is also equipped with the capability of using a Coin Meter. See Illustration below.

Connect one lead to the +12VDC supply (available from the Coin Entry Lamp), another connection from the other lead on the Coin Meter to Connector J15-13 on the ROM/IO Board

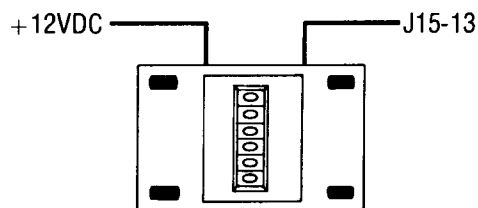


FIGURE 1-6 COIN METER

1.7 GAME INSTALLATION

Open the Coin Door and pull out the bottom Interlock Switch. Turn the game on. The language selection frame should be displayed. If the game is in the game mode, push the door switch toward ADV SUB Test. The game will go into self test. If after a minute, the switch test frame is not displayed, refer to the manual on self test after the switch test is displayed, push the door switch toward ADV set four times.

Then the language selection frame should be displayed, push the door switch toward ADV SUB Test until the language you want is green. Push the left door switch toward ADV Test and then all the print should be in the language you select. Push door switch toward ADV Test four more times the game should now be in game mode. For more information on the options the operator can use, see Section 1.8.17 through 1.8.21.

1.7.1 GAME ADJUSTMENTS

There are several adjustments you can make to the game to make the play easier or more difficult.

First the percentages of screen that needs to be filled can be adjusted anywhere from 0 to 99 percent of the screen. The game is factory set for 75%.

The Time Line can also be adjusted from 0 to 99 seconds. The longer the Time Line the easier the game is to play. The shorter the Time Line the harder the game is to play. The game is factory set at 37 seconds.

Next the difficulty of each screen can be set independently using settings from 0 to 3. Screen 1, has 1 "QIX" and can be set from 0 to 3 the higher the setting the more aggressive the "QIX" become. Screen 2 has 1 "QIX". Screen 3 and 4 have 2 "QIX" per screen. Standard factory settings are, Screen 1 is set at 0, Screens 2, 3 and 4 are set at 1.

1.8 SELF TEST PROCEDURE

1.8.1 GENERAL

The Self Test Procedure is performed using the two (2) Switches located on the inside of the Coin Door, and the Self Test Button and the LED'S on the Video PC Board. (See Figure 1-7).

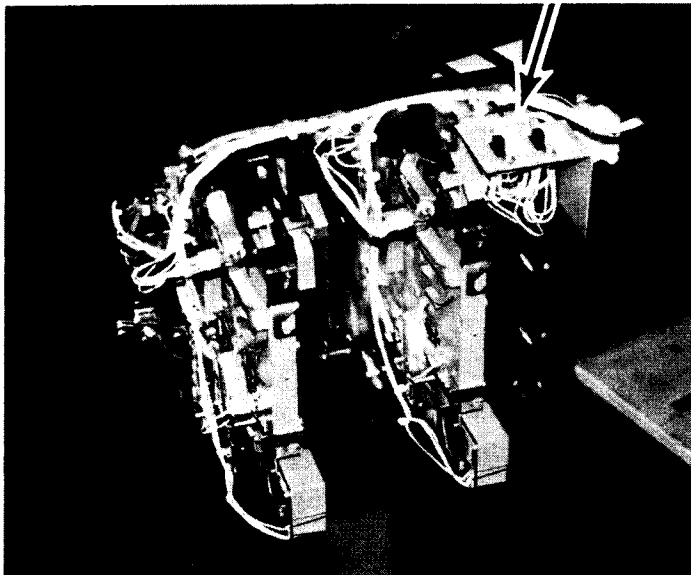


FIGURE 1-7 SELF TEST BUTTON

1.8.2 ENTERING INTO THE SELF TEST MODE

To enter the Self Test Mode, press the Advance Sub-Test Switch on the Coin Door or the Self Test Button found near the LED display. All the LED'S should blink on and the Hardware Tests should start. The Diagnostics can be entered at the Location Programming Screen (Section 1.8.16) by pressing the Advance Test Switch on the Coin Door. If a continual test of the Video Board is desired, press the Self Test Button twice to start the Video Test in the Auto Test Mode. In this mode, the machine will continually run the Hardware test until powered off. If the message "OPEN COIN DOOR TO TEST" appears the Coin Door must be opened or a jumper connected across J19, 1-2. This is because the CMOS RAM Test (Section 1.8.6) cannot be performed with the memory protected by the Coin Door Switch.

1.8.3 HARDWARE TESTS

These tests are performed in the following order:

| VIDEO BOARD | DATA BOARD |
|--------------------|--------------------|
| ROM Checksum | ROM Checksum |
| Communications RAM | Local RAM |
| CMOS RAM | Communications RAM |
| Color RAM | Handshake Test |
| Screen RAM | |

TABLE 1-2 HARDWARE TESTS

All LED values are shown Left to Right. 0 is OFF, 1 is ON and X is dependant upon the test results.

1.8.4 VIDEO BOARD ROM CHECKSUM

The ROM Checksum calculates the checksum of each Video ROM and compares it to the checksum stored for that ROM. If it differs from the stored value, the machine will halt and the value of the ROM with the bad checksum will be shown on the LED'S.

LED VALUES: TEST IN PROGRESS: 00 0001
FAILURE: 01 XXXX

| LED VALUE | VIDEO | 2716 | 2732 |
|-----------|-----------|------|------|
| 01 0000 | A000-A7FF | N/A | U5 |
| 01 0001 | A800-AFFF | N/A | U5 |
| 01 0010 | B000-B7FF | N/A | U6 |
| 01 0011 | B800-BFFF | N/A | U6 |
| 01 0100 | C000-C7FF | U3 | U7 |
| 01 0101 | C800-CFFF | U4 | U7 |
| 01 0110 | D000-D7FF | U5 | U8 |
| 01 0111 | D800-DFFF | U6 | U8 |
| 01 1000 | E000-E7FF | U7 | U9 |
| 01 1001 | E800-EFFF | U8 | U9 |
| 01 1010 | F000-F7FF | U9 | U10 |
| 01 1011 | F800-FFFF | U10 | U10 |

TABLE 1-3 VIDEO BOARD ROM CHECKSUM

If the Checksum ROM is bad, it will show U10 to be bad first. If this test fails, the ROM indicated on the LED display will need to be replaced. The E-PROM Memory in a given game may be implemented as banks of either 2716 or 2732 E-PROMS. The E-PROM type for each bank is selected by the decoding jumper 26-00002-016 for 2716 or 26-00002-032 for 2732.

| E-PROM BANK | LOCATION |
|-------------|----------|
| VIDEO | U1 |
| DATA | U22 |
| SOUND | U29 |

TABLE 1-4 DECODING JUMPER LOCATION

1.8.5 COMMUNICATIONS RAM FROM VIDEO BOARD

The Communications RAM Test determines the stability of memory shared by the two processors by storing a predefined series of numbers throughout the RAM, then reading it back to insure that it was stored correctly.

LED VALUE: 00 0010

A failure has been detected when the machine halts with the above display. Failure of Communications RAM during Video Board Tests may result from either defective RAM circuitry or failure of the Data Board. To isolate the failure, disconnect the Data Board at P6 and re-enter the test. A failure means trouble in U3, U4 or associated circuits. Passing the retest suggests Data Board problems.

1.8.6 VIDEO BOARD CMOS RAM

After saving values in another portion of memory, the CMOS RAM is tested in the same manner as the Communications RAM. If the CMOS RAM passes the test, all of the locations are restored to their previous values.

LED VALUE: 00 0011

A failure of the CMOS RAM has been detected when the machine halts with the above LED value displayed. If this occurs U85 and U86 or associated decoding should be checked.

1.8.7 VIDEO BOARD COLOR RAM

This tests the system Color RAM by storing predefined sequences of numbers in the Color RAM, then reading them back while testing for accuracy.

LED VALUE: 00 0100

A failure is indicated by the processor halting with the above value displayed on the LED'S. This signifies the need to check U56, U57 and associated multiplexing and decoding.

1.8.8 VIDEO BOARD SCREEN RAM

The Screen RAM is tested by writing a pattern to each page on the screen. The results of these writes is then compared to the original pattern. Any discrepancy causes the machine to halt with the LED displaying the faulty RAM.

LED VALUE: TEST IN PROGRESS: 00 0101
FAILURE: 1X XXXX

| LED VALUE | RAM | 11 XXXX | RAM |
|-----------|-----|---------|-----|
| 10 1000 | U26 | 11 1000 | U48 |
| 10 0001 | U32 | 11 0001 | U65 |
| 10 0010 | U31 | 11 0010 | U64 |
| 10 0011 | U30 | 11 0011 | U63 |
| 10 0100 | U29 | 11 0100 | U62 |
| 10 0101 | U28 | 11 0101 | U61 |
| 10 0110 | U27 | 11 0110 | U60 |
| 10 0111 | U26 | 11 0111 | U59 |
| 10 1000 | U17 | 11 1000 | U48 |
| 10 1001 | U16 | 11 1001 | U47 |
| 10 1010 | U15 | 11 1010 | U46 |
| 10 1011 | U14 | 11 1011 | U45 |
| 10 1100 | U13 | 11 1100 | U44 |
| 10 1101 | U12 | 11 1101 | U43 |
| 10 1110 | U11 | 11 1110 | U42 |
| 10 1111 | U10 | 11 1111 | U41 |

TABLE 1-5 VIDEO BOARD RAM CHECKSUM

Upon failure of a screen RAM, locate the problem RAM and replace it. Exchange the suspected RAM with a known good location to determine if the problem moves with the RAM, IC or whatever the problem is in the supporting circuitry. Further testing can be done with the Color Bar Test.

If this Diagnostic appears to halt without indicating a RAM failure (00 0101 on LED'S), a failure to begin the next test (Data Hardware) is indicated. The interconnection to the Data Processor must be in place and the Data Processor must be functional to continue.

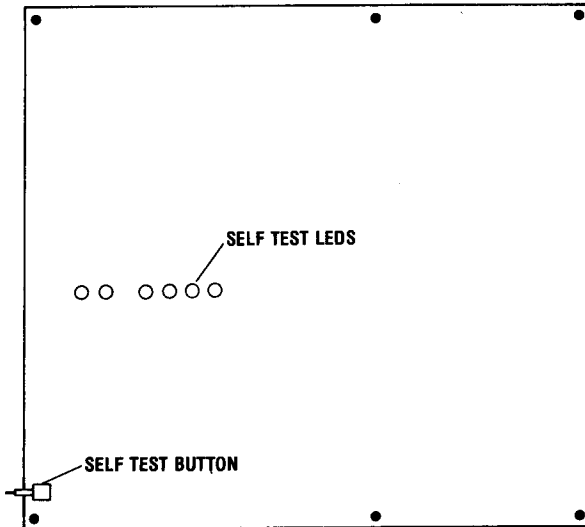


FIGURE 1-8 VIDEO BOARD (ON BACK SERVICE DOOR)

1.8.9 DATA/SOUND BOARD SELF TESTS DATA HARDWARE (ROM CHECKSUM)

The ROM Checksum calculates the checksum of each Data ROM and compares it to the checksum stored for that ROM. If it differs from the stored value, the machine will halt and the value of the ROM with the bad checksum will be shown on the LED'S.

LED VALUE: TEST IN PROGRESS: 00 0110
FAILURE: 01 XXXX

| LED VALUE | DATA | 2716 | 2732 |
|-----------|------|------|------|
| 01 0000 | A000 | N/A | U14 |
| 01 0001 | A800 | N/A | U14 |
| 01 0010 | B000 | N/A | U15 |
| 01 0011 | B800 | N/A | U15 |
| 01 0100 | C000 | U12 | U16 |
| 01 0101 | C800 | U13 | U16 |
| 01 0110 | D000 | U14 | U17 |
| 01 0111 | D800 | U15 | U17 |
| 01 1000 | E000 | U16 | U18 |
| 01 1001 | E800 | U17 | U18 |
| 01 1010 | F000 | U18 | U19 |
| 01 1011 | F800 | U19 | U19 |

TABLE 1-6 DATA/SOUND BOARD ROM CHECKSUM

If this test fails in the field, the bad ROM will need to be replaced.

1.8.10 DATA/SOUND BOARD LOCAL MEMORY

The Data Processor uses a known sequence of numbers to test the bits in its Local Memory. If a bad bit is found the machine will halt with the following display.

LED VALUE: 00 0111

1.8.11 COMMUNICATIONS RAM ADDRESSING

The function of this test is to ensure that both the Data and the Video Processor address the Communications RAM in the same manner. The Data Processor requests the Video Processor to fill the RAM with a known pattern then, the Data Processor compares the result to the expected pattern. If it does not match, one of the processors is probably decoding the address incorrectly as the RAM itself was previously tested for stability by the Video Processor. The machine will halt with the following display.

LED VALUE: 00 1000

1.8.12 DATA/VIDEO HANDSHAKE

This test ensures that the Data Processor can send priority commands via interrupts to the Video Processor. The Video Processor is halted, then restarted by the data Processor after the proper command acknowledgements are received. The machine will halt with the following display.

LED VALUE: 00 1001

1.8.13 SWITCH TEST

This screen is used to determine all switches are in working order before entering the switch dependent self-test screens. The Wiring Diagram supplied with each game will indicate the number associated with a particular switch. The switch number appears in green if the switch is closed and white if it is open.

The Advance Test Switch (Switch Number 9) is always RED in order to set it apart from the other switches on the screen. Switches 29, 30, 31 and 32 are not used and remain Green. The user should check all other switches before pressing the Advance Test Switch, as this would move him to the next screen. In addition to the switches required, by the game, the User should be sure to test the Advance Sub-Test, UP and DOWN Switches located in the Coin Door for proper closure as the switches are used to move about in the Self-Tests Screens. To advance to the next screen, activate the Advance Test Button on the Coin Door.

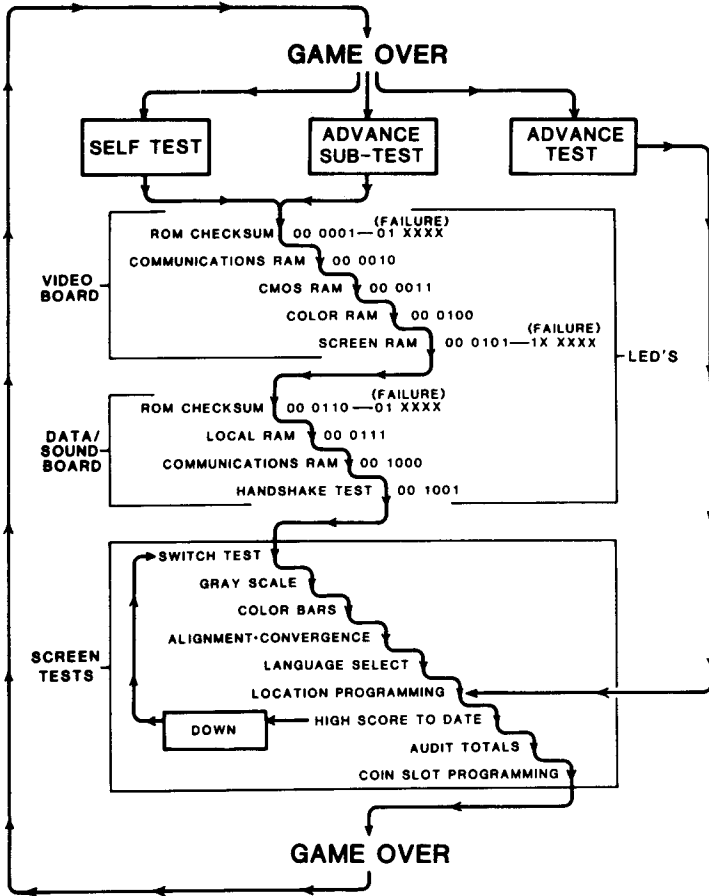
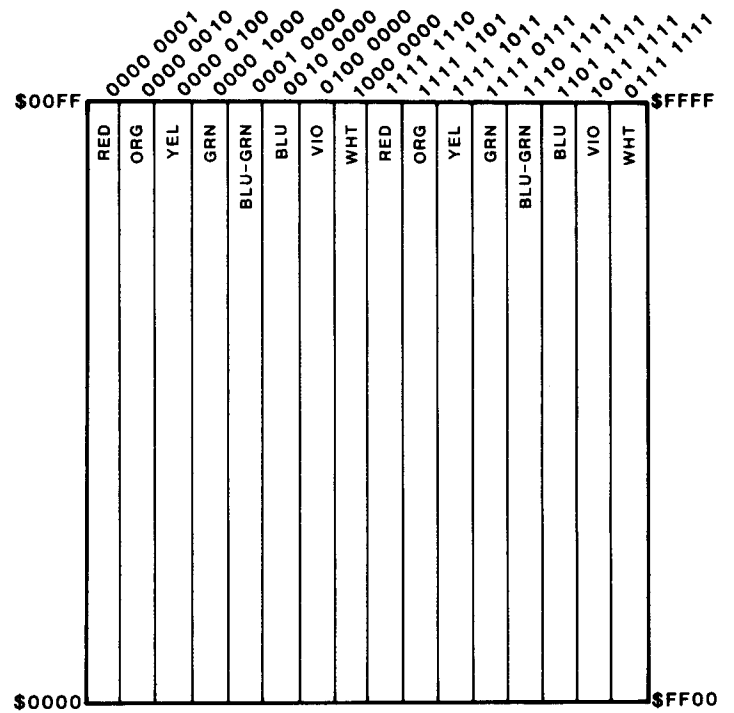


FIGURE 1-9 FLOW CHART



COLOR BAR DIAGNOSTIC

NORMAL

FIGURE 1-10 COLOR BAR

1.8.14 COLOR BALANCE AND INTENSITY ADJUST SCREEN

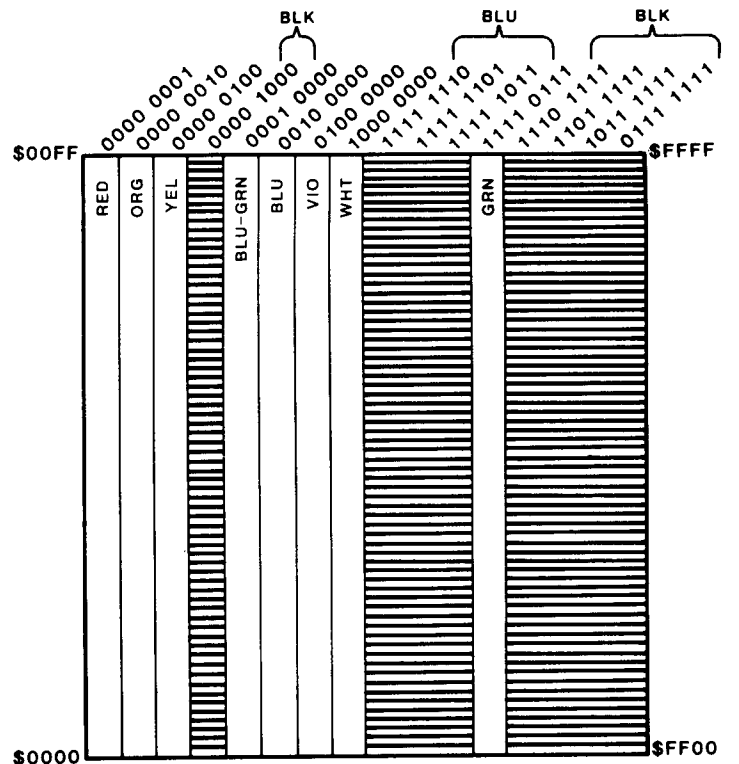
This screen is comprised of two sections. The first section provides a method for adjusting the intensity level of each color gun, and achieving an initial color balance.

Three squares, one blue, one green and one red, are drawn along the top of the screen at Maximum intensity and brightness. The color guns should be adjusted so that these squares are barely visible and equal intensity.

To complete the color adjustments, a gray scale is provided at the bottom of the screen. Fine tune the color balance with this scale, the double check that the squares at the top are barely visible. To advance to the next screen, activate the Advance Test Switch located on the Coin Door.

1.8.15 COLOR BARS

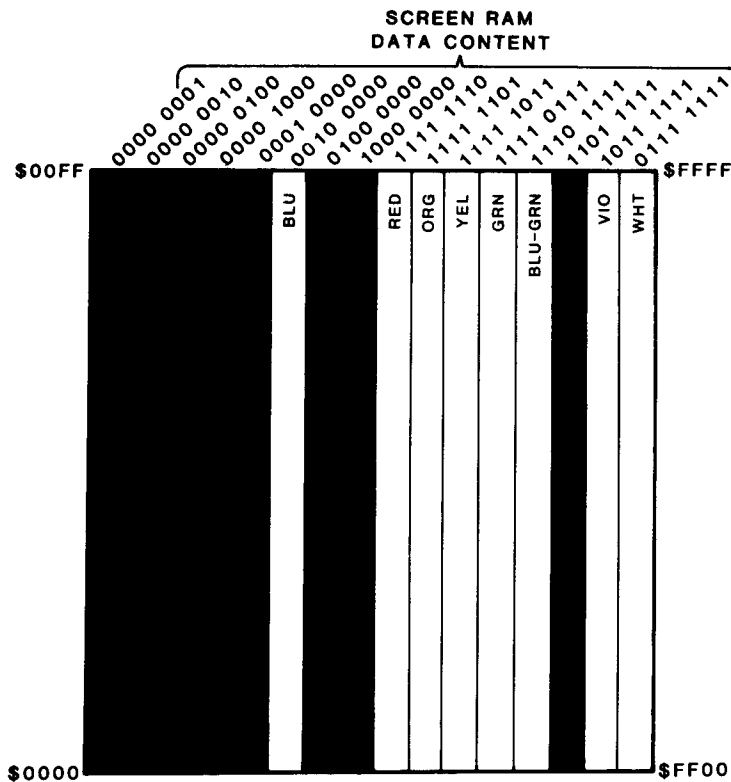
The CPU divides the screen RAM into 16 areas corresponding to 16 bars on the screen. Each area is written with a data value from the Table below. Each value exercise one bit in the Screen RAM. The Color RAM is written with a pattern which outputs each data value with a recognizable color from the Table. All other data values are coded black. This results in a normal screen of 16 color bars per the following table.



COLOR BAR DIAGNOSTIC

BIT 03 STUCK LOW IN 1-BANK

FIGURE 1-11 COLOR BAR



| SCREEN RAM CONTENT COLOR RAM ADDRESS | | | | |
|---|------------|-----|-----------|------------|
| BAR # | COLOR | HEX | BINARY | BIT TESTED |
| 1 | Red | 01 | 0000 0001 | 0 |
| 2 | Orange | 02 | 0000 0010 | 1 |
| 3 | Yellow | 04 | 0000 0100 | 2 |
| 4 | Green | 08 | 0000 1000 | 3 |
| 5 | Blue Green | 10 | 0001 0000 | 4 |
| 6 | Blue | 20 | 0010 0000 | 5 |
| 7 | Violet | 40 | 0100 0000 | 6 |
| 8 | White | 80 | 1000 0000 | 7 |
| 9 | Red | FE | 1111 1110 | 0 |
| 10 | Orange | FD | 1111 1101 | 1 |
| 11 | Yellow | FB | 1111 1011 | 2 |
| 12 | Green | F7 | 1111 0111 | 3 |
| 13 | Green Blue | EF | 1110 1111 | 4 |
| 14 | Blue | DF | 1101 1111 | 5 |
| 15 | Violet | B7 | 1011 1111 | 6 |
| 16 | White | F7 | 0111 1111 | 7 |
| None | Black | XX | XXXX XXXX | |

TABLE 1-7

NOTES

If the Self-Test pass, errors in those circuits which affect CPU accesses are ruled out. This leaves latches U91, U94, shift registers U95, U96 and U105-109, direction select U81 and U104 and the CR side of the Color RAM MUX U55, U73, and U74.

Stuck bits may be indentified by observing abnormal bars. A bit stuck high will result in black bars (two bit high) on the left or top half of the screen except for the bar associated with the stuck bit. On the right of bottom half, the bar associated with the stuck bit will be black. The converse is true of a bit stuck low.

An error across the entire bar indicates an error in the shift registers, direction select, or color RAM MUX which affects every pixel. Lines of error running crosswise to the bars indicate an error in one bank of RAM of every eighth pixel. To move to the next screen, activate the Advance Test Button.

If self test fails, the Color Bars still may be useful. This screen may now be entered without going through on-board self test. Use "Advance Test" to enter the High Score Screen then "Down" to enter the Switch Test. Advance Test may then be used to access the Color Bars.

1.8.16 ALIGNMENT AND CONVERGENCE TEST

This screen is provided to align the color guns and correct the convergence on the screen. The screen is composed of a red and a green rectangle and white grid.

Adjust the screen width and length so that the red rectangle is slightly within the boundaries of the tube. The adjustment is to be made on the center of the lines which make up the rectangle. The corners of the rectangle will extend beyond the shadow mask. The green rectangle defines the normal playfield and so should be visible from the players view point.

A grid of white squares is provided to help detect and correct any convergence problems the tube may have. Adjust the monitor until the squares are of equal size throughout the screen.

To advance to the next screen, activate the Advance Test Button on the Coin Door.

1.8.17 LOCATION PROGRAMMING SCREEN(LANGUAGE SELECTION)

This screen allows the user to select the language in which the Location Programming and the game will operate. Four (4) languages are provided. Use the Advance Sub-Test Button to move through the offered languages. When the desired language is green, depress the Advance Test Button, to advance to the next screen.

1.8.18 LOCATION PROGRAMMING

This screen allows the location to define the difficulty factor for the game. It also allows the location to set a maximum number of credits allowed in the machine prior to a game start up.

The user selects the line to be changed by using, the Advance Sub-Test Button until the desired line is changed to green. The value associated with this line is then modified with the UP and DOWN Switch. If the machine is to be reset to the factory settings, use the Advance Sub-Test Button until the reset line is lit in green, then press the UP Switch. The values will be reset and the user will be placed back on the first line for futher adjustments. Advance test will move to the next screen at any time.

The backup HSTD (High score to date) value is used to reset the high score on the next screen. Its value will initially determine the score needed for a player to have his own initials show with his score in the high scores.

The maximum credit defines a limit for the machine, which when crossed will disable the coin slots. This allows the location to set a limit on the amount of games a player will get if there is a line of people waiting. This value ranges from 1 to 99. However, it should not be set so close to 99 that a single coin can overflow the credits issued (maximum 99). A Free Play Mode may be selected by setting maximum credits to 0. The credits per coin are set in the coin slot programming screen.

1.8.19 HIGH SCORE TO DATE SCREEN

This screen shows the scores and initials of the players with the ten highest scores. It is used as an audit for the game. To reset the values to the backup HSTD selected on the previous screen, press the UP Switch. This will also set the initials to "TAC".

When the UP Button is activated it resets to default scores. To move to the next screen, activate the Advance Test Button on the Coin Door.

1.8.20 AUDIT TOTALS

This screen provides the audit totals for the game. Once they are recorded, they may be zeroed by pressing the UP Switch. The following audits are kept.

| | |
|--------------------|---|
| Total Credits | The total number of paid credits issued. This total is never zeroed, but it will wrap around to zero when its total reaches 1,000,000. The only time this total can be zeroed is by physically removing the battery or jumper W1, while the power is off. |
| Left Coins | The number of coins dropped into the left slot. |
| Center Coins | The number of coins dropped in the center slot. |
| Right Coins | The number of coins dropped into the right slot. |
| Paid Credits | The number of credits issued for coins. |
| Awarded Credits | The number of credits awarded by the game. |
| % Free Plays | $\text{Awarded credits} / \text{paid credits} + \text{awarded credits} * 100$ |
| Minutes Played | Number of minutes the game has been in play mode. |
| Minutes Awarded | Number of minutes the game has been in extended or awarded play. |
| % Free Time | $\text{Awarded minutes} / \text{minutes played} * 100$. |
| Average Game (Sec) | $\text{Minutes played} / \text{paid credits} + \text{awarded credits} * 60$ |
| High Scores | The number of times which a player scored high enough to bump someone else from the high score list. |

TABLE 1-8 AUDIT TOTALS

The UP Switch is used to zero the audits. To advance to the next screen, activate the Advance Test Button on the Coin Door.

1.8.21 COIN SLOT PROGRAMMING

This screen allows the user to either select a standard coinage setting for the game or program his own. If a standard setting is desired, use the UP and DOWN Switch to adjust the coinage setting while it is lit in green. The values for the variable will change as this number is altered. When the right selection is set, use Advance Test to return to the game.

If a non-standard setting is desired, use Advance Sub-Test Switch to move down to the variables so that they may be programmed individually. Once this switch is pressed, the setting number is set to zero to show that the location has supplied their own settings. As the lower variables are unchanged, the user may minimize his effort by first selecting a setting close to the one he desires. Once in the programming mode, the Advance Sub-Test Switch is used to move among the variables. It will also take you back to the standard settings, if you press it by mistake. The UP and DOWN Switches are used to increment or decrement the values. Advance Test Switch will return to the game when pressed.

The coin multiplier tells how many coin units are issued for each coin through a particular slot. Coin units for credit show the number of units necessary before a credit is issued. Coin units for bonus gives the number of units necessary before a bonus credit is issued.

Minimum coin is an optional value which will keep the credits from accumulating until the specified minimum amount of coin units is reached. It is not used in any of the standard settings.

1.8.22 CMOS MEMORY FAILURE

If the message "Memory Failure - Service Required" appears on the screen, the CMOS RAM which stores all of the location programming has failed. All the values stored in the RAM are set back to factory defaults. This condition probably indicates a battery failure or a Failure of U85 or U86. Refer to Section 2 on Maintenance 2.8 CMOS RAM.

STANDARD COIN SETTINGS

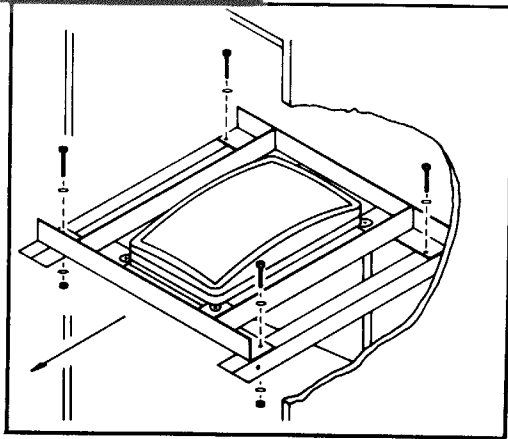
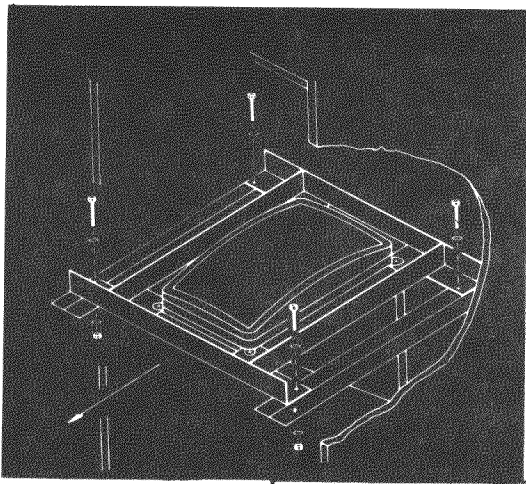
TABLE 1-9

| | | Standard Setting | Left coin slot multiplier | Center coin slot multiplier | Right coin slot multiplier | Coin units for credit | Coin units for bonus | Minimum coin units |
|-----------------------------|-------------------|---------------------|---------------------------|-----------------------------|----------------------------|-----------------------|----------------------|--------------------|
| COIN DOOR MECHANISMS | | CREDIT/MONEY | | | | | | |
| STANDARD | 1/.25, 4/*1 | 01 | 01 | 04 | 01 | 01 | 00 | 00 |
| | 1/.50, 3/*1, 6/*2 | 02 | 01 | 04 | 01 | 02 | 04 | 00 |
| | 1/.50 | 03 | 01 | 04 | 01 | 02 | 00 | 00 |
| 1 DM, 5 DM | 1/1DM, 6/5DM | 04 | 06 | 00 | 01 | 01 | 00 | 00 |
| 1 FRANC, 5 FRANC | 1/2F, 3/5F ONLY | 05 | 01 | 16 | 06 | 02 | 00 | 00 |
| 25 CENTS, 1 GUILDER | 1/25, 4/1G | 06 | 01 | 00 | 04 | 01 | 00 | 00 |
| 5 FRANCS, 10 FRANCS | 1/5F, 2/10F | 07 | 01 | 00 | 02 | 01 | 00 | 00 |
| | 1/10F | 08 | 01 | 00 | 02 | 02 | 00 | 00 |
| 1 FRANC, 2 FRANC | 2/1F, 5/2F | 09 | 00 | 04 | 01 | 04 | 00 | 00 |
| 1 UNIT, 5 UNITS | 1/2, 3/5 | 10 | 01 | 00 | 06 | 02 | 00 | 00 |
| TWIN COIN | 1/1 COIN | 01 | 01 | 04 | 01 | 01 | 00 | 00 |
| | 1/2 COINS | 03 | 01 | 04 | 01 | 02 | 00 | 00 |

CUSTOM COIN SETTINGS

TABLE 1-10

| | | Standard Setting | Left coin slot multiplier | Center coin slot multiplier | Right coin slot multiplier | Coin units for credit | Coin units for bonus | Minimum coin units |
|-----------------------------|----------------------|---------------------|---------------------------|-----------------------------|----------------------------|-----------------------|----------------------|--------------------|
| COIN DOOR MECHANISMS | | CREDIT/MONEY | | | | | | |
| STANDARD | 1/.25, 5/*1 | 00 | 01 | 04 | 01 | 01 | 04 | 00 |
| | 2/.50, 5/*1 | 00 | 01 | 04 | 01 | 01 | 04 | 02 |
| | 2/.50, 4/*1 | 00 | 01 | 04 | 01 | 01 | 00 | 02 |
| | 1/.50, 3/*1, 4/*1.25 | 00 | 03 | 12 | 03 | 04 | 15 | 00 |
| | 1/.50, 3/*1, 7/*2 | 00 | 12 | 48 | 12 | 14 | 96 | 24 |
| 25 CENTS, 1 GUILDER | 1/.25, 5/1G | 00 | 01 | 00 | 04 | 01 | 04 | 00 |
| 100 LIRE, 200 LIRE | 1/200 LIRE | 00 | 01 | 00 | 02 | 02 | 00 | 00 |
| TWIN COIN | 1/3 COIN, 2/5 | 00 | 02 | 00 | 02 | 05 | 00 | 00 |
| 1 UNIT, 5 UNITS | 1/1, 5/5 | 00 | 01 | 00 | 05 | 01 | 00 | 00 |
| | 1/3, 2/5 | 00 | 02 | 00 | 10 | 05 | 00 | 00 |



Maintenance

ALL GAMES REQUIRE A CERTAIN AMOUNT OF MAINTENANCE TO KEEP THEM IN GOOD WORKING ORDER. A PERIODIC CHECK OF THE MECHANICAL CONTROLS WOULD BE BENEFICIAL TO THE SUCCESS OF YOUR GAME.

2

2. MAINTENANCE

2.1 CLEANING

The exterior of the game, all metal parts and all plastic parts can be cleaned with a non-abrasive cleanser. Caution should be used when cleaning the glass, a dry cloth can cause scratches and result in a foggy appearance.

2.2 COIN DOOR

The Coin Door used in the "QIX" game needs little or no maintenance. See Figure 2-1. If desired a special coin mechanism cleanser, that leaves no residue, can be obtained from your distributor. Refer to the manufacturers documentation if additional information is needed.

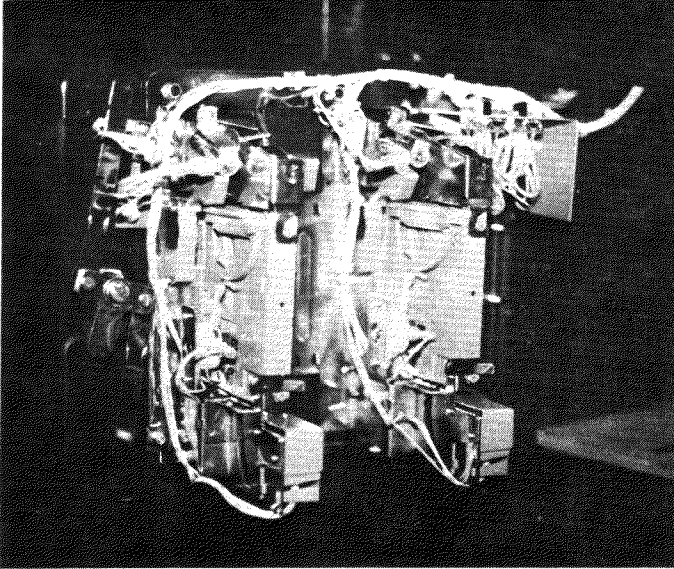


FIGURE 2-1 COIN DOOR

2.3 FUSE REPLACEMENT

This game contains 8 fuses. Seven of these fuses can be found on the Power Supply Assembly, five (5) are on the PCB and two (2) are on the Power Supply Bracket. One (1) is located at the bracket where the AC line cord comes into the cabinet. See Figure 2-2 for location of these fuses.

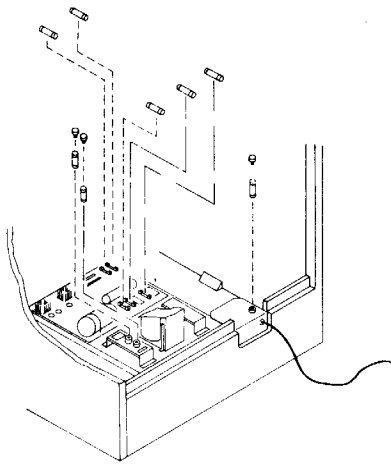


FIGURE 2-2 FUSE REPLACEMENT

2.4 MONITOR REMOVAL

If you need to remove the Video Monitor, follow the instructions listed below:

CAUTION

It is recommended the game be left disconnected for at least one hour before removing the video monitor. This will probably discharge the video tube but EXTREME CAUTION is still necessary.

- * Disconnect power from the line voltage.
- * Disconnect the monitor cable connector.
- * Remove the wire cable clamp.
- * Take out the two side bolts, one on each side of the cabinet.
- * Remove the four mounting bolts and disconnect the green ground wire.
- * Slide the Monitor out by pulling the Monitor toward you.

CAUTION

Use EXTREME CAUTION and do not touch electrical parts of the Monitor Yoke area with your hands or with any metal object in your hands! High voltages may exist in any Monitor, even with power disconnected.

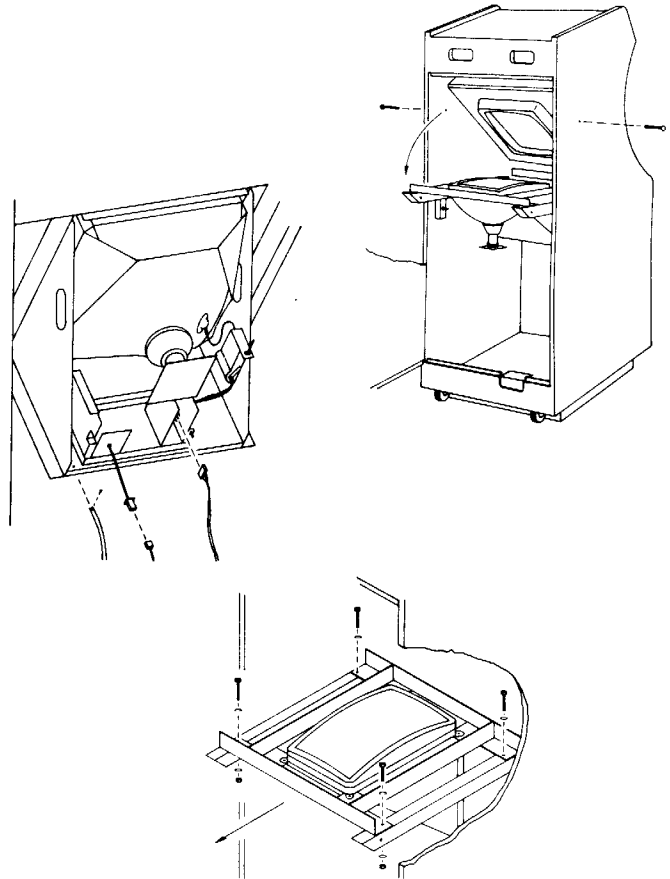


FIGURE 2-3 MONITOR REMOVAL

2.5 COVER GLASS REMOVAL

To remove the Cover Glass follow the instructions listed below:

1. Remove the Control Panel.
2. Loosen three (3) screws on the Cover Glass, front bracket.
3. Open Service Door and remove the (Rear) Cover Glass bracket.
4. Slide glass out through the Service Door.

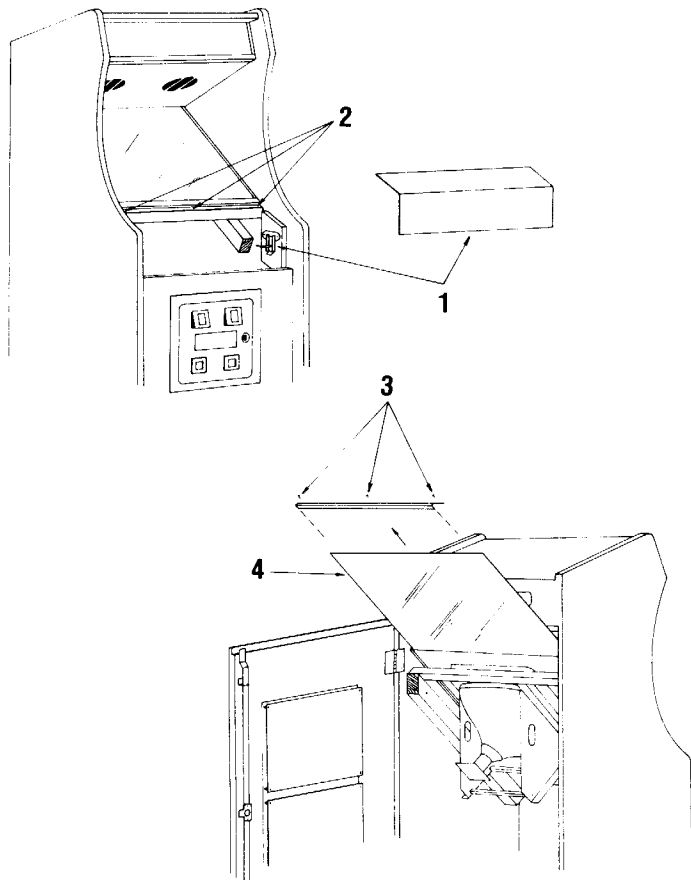


FIGURE 2-4 COVER GLASS REMOVAL

2.6 PRINTED CIRCUIT BOARD REPLACEMENT

You may wish to remove the "QIX"™ printed circuit board, Video Processor (998846), Data/Sound Board (998845), or ROM I/O Board (998847) for servicing. Refer to Figure 2-5.

The "QIX"™ Printed Circuit Boards (PCB) are located on the inside of the rear service door for easy access.

To remove the boards the following steps should be followed:

1. Open the rear service door, the power will automatically be removed by the Interlock Switch located on the inside of the door frame.
2. Disconnect the connectors from the board or boards you wish to remove.
3. Disconnect the ribbon cable, connecting the boards by spreading eject latches on the connector.
4. Remove the screws for the board you wish to remove.

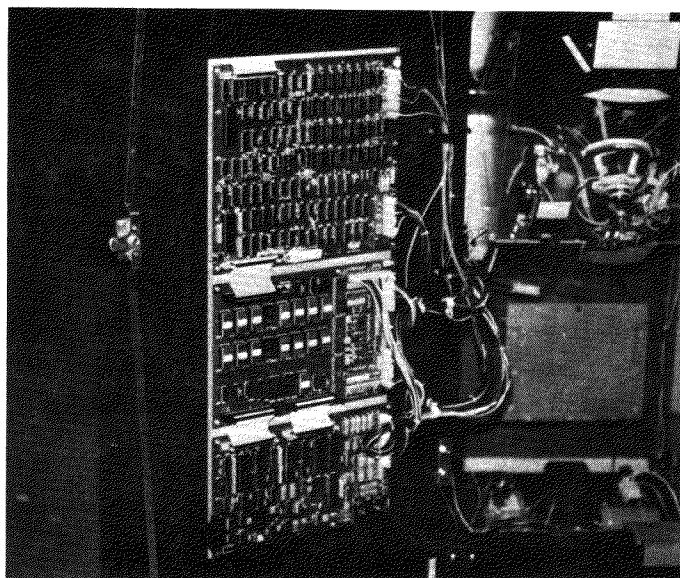


FIGURE 2-5 PRINTED CIRCUIT BOARD

2.7 POWER SUPPLY

The Power Supply produces all the necessary game voltage requirements. Refer to Figure 2-6 while reading the following circuit description.

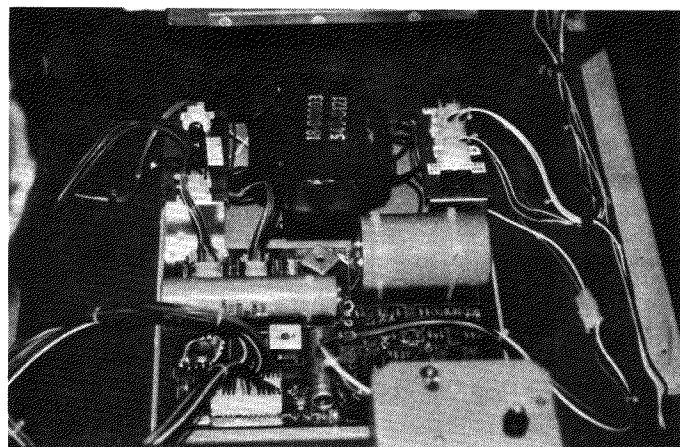


FIGURE 2-6 POWER SUPPLY

2.7.1 AC INPUT

The AC Input Voltage is applied to the main Power Supply via the AC Line Cords, Line Filter, Line Fuse, Power Switch and Interlock Switch. Different Line Cords are used for 120V and for 240V. The Line Fuse is located on the Line Cord Assembly near the Strain Relief. A Voltage Programming Block is located on the primary side of the Transformer to compensate for high/low voltage conditions. The following line voltages may be inserting the appropriate Programming Plug.

| Line Voltage | | Line Fuse |
|---------------|---------|-----------|
| 100 VAC ± 10% | 50/60Hz | 3 AMP |
| 120 VAC ± 10% | 50/60Hz | 3 AMP |
| 200 VAC ± 10% | 50/60Hz | 1.5 AMP |
| 220 VAC ± 10% | 50/60Hz | 1.5 AMP |
| 240 VAC ± 10% | 50/60Hz | 1.5 AMP |

TABLE 2-1 LINE VOLTAGE

CAUTION

For continous protection against fire hazard, replace only with a fuse of the same type having the same electrical rating.

There are five secondary sources. Three go to the Regulator PCB providing +5VDC, +12VDC, -12VDC, and -5VDC. The other two are fused 6.3VAC used for the incandescent lighting and fused 120VAC used for the monitor, and in certain models for a fluorescent lamp and fan. These secondary fuses are located on the bracket adjacent to the Power Transformer.

| Circuit | Secondary Fuse |
|---------|----------------|
| 120VAC | 2.0AMP SLO-BLO |
| 6.3VAC | 2.5AMP |

TABLE 2-2 SECONDARY FUSES

2.7.2 -5VDC AND -12VDC REGULATORS

The AC Input for the negative voltages comes into the Regulator PCB on J1-5 and J1-6 from the transformer. Fuse F3 protects against short circuits. The AC voltage is then full wave rectified by BR3 and filtered by C16. The raw DC is then applied to Reg 1, a three terminal -12V Regulator. The output of this Regualtor is the -12VDC output for the system and is also the input voltage for Reg 2, a -5V Regulator. The output of this Regulator is the -5VDC for the system.

Capacitors C17, C18, C19 are to improve the transient response and stability of the minus voltage regulator. Diodes D8 and D9 provide protection against C18 and C19 being shorted through the Regulator.

Resistors R34 and R35 provide current limiting for LED'S 3 and 4 which will light when there is voltage present at the regulation outputs.

2.7.3 +5VDC REGULATOR

The AC Input for the +5VDC Regulator circuit comes in on J1-4 and J1-2, via F1 into BR1. BR1 full wave rectifies the AC Input. This raw DC is applied to the collectors of (2) series pass transistors, mounted on the Heat Sink Assembly. The regulation is done by U3, which is a voltage regulator whose output controls the gain of Q5, which in turn controls the gain of the series pass transistors. The emitter of the series pass transistor return to the Regulators PCB and through R11 and R12, which serve to force current sharing between the series pass devices. The voltage at the output of R11 and R12 are the +5VDC for the system. R11 and R12 are voltage set and current foldback adjustments respectively. These are factory adjusted to $5V \pm .25V$. at 7AMPS.

Q8, D3 and R20 comprise a SCR-Type Crowbar Circuit which will trigger when the DC output voltages rise above 5.8V. Once the SCR fires, the Power Supply has to be turned off to reset the device. R19 is a current limiter for the voltage indicator LED 1. R16 is used to set the output voltage of the Regulator.

C8, D2, R13 and Q4 delay the start-up of the 5V Regulator to allow the -5VDC Regulator to stabilize first.

2.7.4 +12VDC REGULATOR

This circuit is essentially the same as the 5V Regulator described above. The AC current comes in on J1-3 and J1-4, via fuse F2 into BR2. The AC is rectified by BR2 and filtered by C9. The raw DC is fed to a single series pass transistor on the Heat Sink Assembly and also powers the +12V and +5V Regulator. R28 and R25 are voltage set and current foldback and factory adjusted to 12 Volts $\pm .25V$ at 4 AMPS. D7, Q9, and R31 are SCR Crowbar Circuits which trigger at 13VDC output which causes supply to go into current foldback. There is an RC delay as in the 5V circuit to delay the +12V rise time.

2.7.5 RESET CIRCUIT

The reset circuit will output a 2sec active low MRST pulse at J3-14 J4-14 when the power is first turned ON and whenever power fails for more than 35ms.

The reset circuitry is comprised of a Dual Timer (556) and a fullwave type optical coupler across an AC secondary. The output of U1 is the input to one half of the 556 which is configured as a missing pulse detector. C1 and R3 determine the time before the output goes active. This is set for about 35ms. When two or more cycles are missing, the output of the first timer triggers the second timer which drives the MRST low for about 2 seconds. The timer constant for the second timer is set by R4 and C6.

Power on reset is generated by C4, and R39 and D12 on the trigger input of the second timer. Q3 inverts the signal out of the 556 so it is active low. R7 insures MRST is low while the power is rising.

2.7.6 POWER SUPPLY ADJUSTMENTS

VOLTAGE Adjust voltages on +5V and +12V for +5.00V to +5.05V and +12.00V to +12.05V.

CURRENT LIMIT Adjust control (5I and 12I) counterclockwise until voltage just changes, then turn control clockwise until voltage goes back to original value with pointer, mark position of arrow on potentiometer then turn control until beginning of 1st notch is aligned with the pointer. On the controls with the Blue Disk turn approximately 30°.

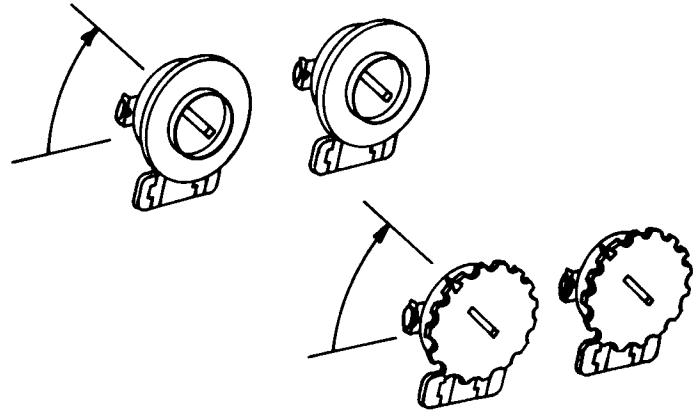


FIGURE 2-7 CURRENT LIMIT ADJUSTMENT

NOTE: If Voltage adjustment will not bring voltage up, set current limit adjustment to $\frac{1}{2}$ value.

2.8 CMOS RAM

If when powering the game up, it will not coin up because the battery is low. The following Procedure should be followed.

Open the Back Door of the game, pull W1 out on the Video Board (Blue jumper). Wait 2 minutes, power back on and insert W1 back in. Open the Coin Door and pull out bottom Interlock Switch. If the Language Select frame does not come on the CRT, power down, remove W1 again. Short pins 18 and 9 on U85, power back on and insert W1 back in. Leave the game on for 12 hours. If this Procedure does not work when you turn the game back on the battery may need to be replaced.

2.9 TEST POINTS

The following is a list of Test Points to be used when troubleshooting.

DATA/SOUND BOARD

| | | |
|-------|-------------|-------------------------------|
| DTP1 | E | (Master Clock) |
| DTP2 | Q | (Master Clock) |
| DTP3 | DMA/BREQ | |
| DTP4 | SA 15 | (Address Line) |
| DTP5 | DA 15 | (Address Line) |
| DTP6 | Voice Clock | |
| DTP7 | SBSC | (Sound Processor Data Enable) |
| DTP8 | DBSC | (Data Processor Data Enable) |
| DTP10 | +5V | |
| DTP11 | Ground | |

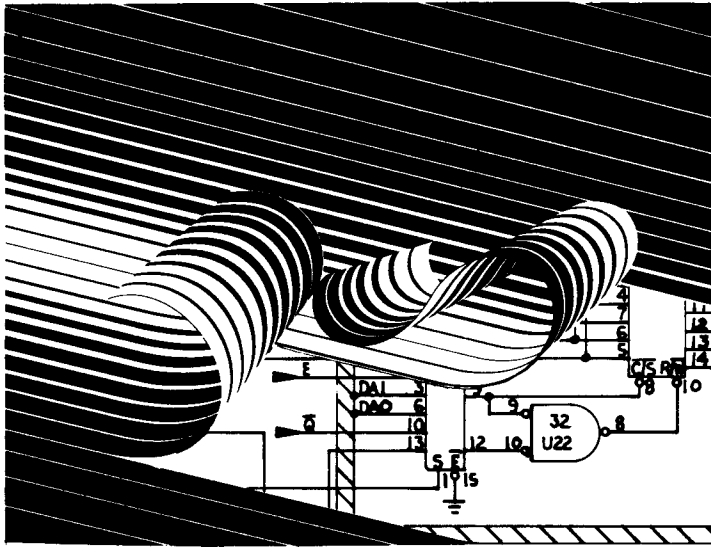
TABLE 2-3 DATA/SOUND BOARD TEST POINTS

VIDEO BOARD

| | | |
|------|---------|-------------------------|
| VTP1 | Invert | |
| VTP2 | 10 MHZ | |
| VTP3 | VQ | (Clock Video Processor) |
| VTP4 | VE | (Clock Video Processor) |
| VTP5 | Extal | (External Clock) |
| VTP6 | DMA/BRK | |
| VTP7 | VBSC | (Video Data Enable) |
| VTP8 | VA 15 | (Address Line) |

TABLE 2-4 VIDEO BOARD TEST POINTS

If you ground any Data Enable Test Point (DTP7, DTP8, VTP7) the related processor will receive no OP and the address line will act like a 16 Bit Counter.



Theory Of Operation

THIS SECTION PROVIDES A TECHNICAL DESCRIPTION OF THE "QIX"™ GAME. THE GAME ELECTRONICALLY CONSISTS OF PRINTED CIRCUIT BOARDS, TV MONITOR, POWER SUPPLY, AND SPEAKERS WHICH ARE DESCRIBED IN DETAIL IN THE FOLLOWING TEXT.

3

3. THEORY OF OPERATION

3.1 GENERAL

The TAITO AMERICA CORPORATION'S arcade video system game is an advanced multiprocessor based circuit utilizing the Motorola 6809E microprocessor.

The system is organized in three logical blocks:

- A. The Data Processor, which supervises the operation of the entire system.
- B. The Video Processor, which performs all screen based functions, such as playfield image motion, line drawing, etc.
- C. The Sound Processor, which generates sounds under the direct control of the Data Processor.

In order to facilitate easy inter-system communications, the Data and the Video Microprocessors run synchronously using clock and timing signals developed on the Video Board. For this reason, discussion will begin by examining the Video Board.

3.2 VIDEO BOARD

3.2.1 SYSTEM CLOCK

The fundamental system clock is developed by the 20MHz crystal, inverters U24 and U39, and components. The 20MHz signal is divided by the high speed flip flop U38 to obtain a 10MHz main clock with a precise 50 percent duty cycle. This 10MHz signal generates all other fundamental timing signals for the video system, including the Data Processor. IC23 divides the 10MHz signal to obtain 5MHz, 2.5MHz and CCLK, and their respective inversions. IC's U9, U37, and U38 combine these signals, presenting them to U25, which synchronizes the output signal to the system 10MHz clock. This circuit produces waveforms whose active edges are synchronized to 15ns worse case, 2ns average.

The characteristics of the clock circuit may be noted by reference to the Timing Diagram, Figure 3-1.

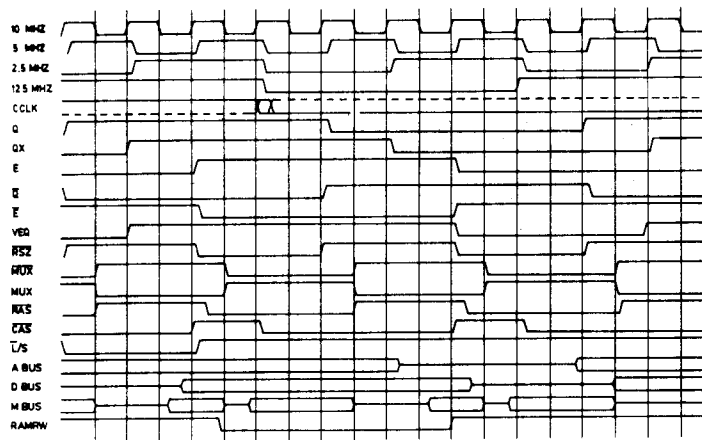


FIGURE 3-1 CLOCK TIMING

3.2.2 SCREEN RAM

The Video Processor controls a Screen RAM of 256 x 256 pixels with 8 bits per pixel. In order to access of this information, the screen is divided into two pages, top and bottom, chosen under software control. These pages are both addressed at 0000 - 7FFF with address 0 corresponding to the lower left corner of the screen (horizontal scan). All CRT accesses to this RAM are transparent to the processor and the RAM may be read or written any time.

The timing of the Screen RAM and the eventual scan is controlled by a 6845/6545/46505 CRT Controller Chip. It's address outputs are gated by U19, U20, U50, and U51 for inversion when used a cocktail table mode. The scan addresses are multiplexed with the address present on the microprocessor address bus by U35, U52, U53, and U54 for standard RAS-CAS accessing. The desired bank of memory is addressed by U87, a one of four decoder.

Data written into the Screen RAM comes directly from the system data bus, buffered by 33 Ohm resistors. If a processor read is taking place, the data is placed on the data bus by U77, U78, U79, and U80. First byte, screen reads are latched by 374's U91, U92, U93, and U94. A second byte screen read is then performed, and this data, together with the data from the first screen read latched by the 374's is loaded in to the eight (8) 74LS299 shift registers. These registers may be shifted in either direction for cocktail table implementation. The byte stream then proceeds to the Color RAM.

| | ADDRESS | VIDEO BOARD MEMORY MAP |
|----|---------|---------------------------------------|
| A. | \$8000 | Dual Port RAM |
| B. | \$8400 | CMOS Battery Backup Memory |
| C. | \$8800 | LED Output and Color RAM Page Select |
| D. | \$8C00 | Data FIRQ Activation Address |
| | \$8C01 | Video FIRQ Deactivation Address |
| E. | \$9000 | Color RAM |
| F. | \$9402 | Address Latch Hi-Byte |
| | \$9403 | Address Latch Lo-Byte |
| | \$9400 | Address Latch Indexed Screen Location |
| G. | \$9800 | Scan Line Readback Location |
| H. | \$9C00 | CRT Controller Base Address |

TABLE 3-1 VIDEO BOARD MEMORY MAP
(\$=HEXADECIMAL)

3.2.3 DUAL PORT RAM

This RAM may be accessed in its entirety by either processor. This is arbitrated as follows:

1. The Data Processor runs in quadrature with (one quarter clock cycle ahead of) the Video Processor. In other words, E is inverted for use as DQ, and Q becomes DE. Refer to Timing Diagram, Figure 3-2.
2. The Data Processor, by nature of this timing, accesses the Dual Port RAM 1/4 cycle before the Video Processor. At this point the Video Processor is guaranteed to not be accessing the RAM. The Data Processor access is flagged by U36, which causes a cycle to be stolen from the Video Processor's main clock, VQ and VE.
3. The Video Processor is unable to access the Dual Port RAM unless the Data Processor is not accessing it as it will not be receiving clocks during that time. The cycle steal is accomplished by the generation of signal DPMUX by U36. This signal directly steals the cycle, and also folds over multiplexers U5, U6, and U21, switching the address lines, R/W and gating signals. U1 and U2 gate the data to or from the disired processor. U22 insures that no spurious writes are generated during foldover.

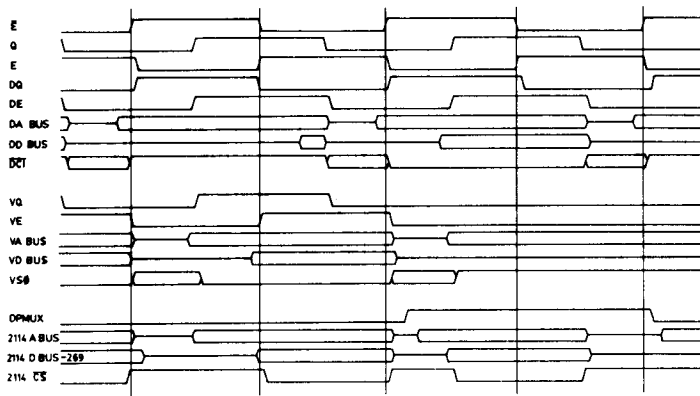


FIGURE 3-2 DUAL PORT RAM TIMING

3.2.4 CMOS RAM

The CMOS RAM is implemented for use as both a battery back-up storage area and a work area for the Video Processor. The gating U100, U101, U102, and U103 insure that writes to the block RAM from \$8700 - 87FF cannot be performed unless the Coin Door is open (J19-2 grounded). The 3.6V NiCAD battery is trickle charged by Q8, R64, and R65 when the system is powered. When turned off, supply current for U85, U86, and U100 is provided by this battery. U100 is included to solidly gate the MRST signal and prevent invalid operations during power Up and Down. LED and Color RAM Page Latch, U72 is addressed at address \$8800. The upper six bits drive LED'S on the circuit board for diagnostics which cannot be done through the screen. The lower 2 bits select the Color RAM page and will be discussed later.

3.2.5 BI DIRECTIONAL FIRQ CAPABILITY

To provide for immediate inter-system communication on demand a Bi-Directional FIRQ Capability has been provided. Any access of address \$8C00 by the Video Processor will generate a FIRQ to the Data Processor. Any access of \$8C01 by the Video Processor will remove a FIRQ generated by the Data Processor to the Video Processor. This is accomplished by U7, U8, and U9.

3.2.6 COLOR RAM

The Color RAM is used as a translation matrix so that a number of different pixel values may access a given color, or to change the color of a given area of the screen without rewriting the Screen RAM. The serial bit stream, eight bits wide, comes from the shift registers of the Screen RAM to be presented to multiplexers U55, U73, and U74. These select between the Video Processor bus and the serial bit stream. As processor access times are considerably greater than the basic bit time (200ns), it is necessary to access this register only during retrace times. Bus read/write occur through U75, and serial output is latched by U76. This Data Stream is converted to a color pallet of 64 colors and four intensities. When the serial bit is selected for access, the two high order bits are provided by the LED output latch. This allows the Programmer to select between four pages of RAM rapidly.

3.2.7 ADDRESS LATCH CIRCUITRY

Two methods of Screen Memory Address are provided:

1. A 16 bit address may be written into latch U70 and U71 addressed at \$9402 and \$9403. The addressed location may be accessed by reference to location \$9400.
2. The high order bit of the latch selects one of two pages which may be directly addressed by reference to locations \$0000 - \$7FFF. U36, U70, and U71 latch the address. U36 is used in conjunction with U70 as U70 and U71 are tri-stated when inactive. The screen address deposited on the LA bus by U84 and U98 for Processor Bus accesses, and by U70 and U71 for latched address. Decoding is performed by U87 and U88.

3.2.8 SCAN LINE READBACK

When read, this location is the number of the scan line currently being drawn by the beam. U34 latches the last row address drawn, and U101 prevents erratic updating at the end of a horizontal line. There are 256 valid scan lines 00 - FF.

3.2.9 CRT CONTROLLER

The 6845/6545/46505 is a software programmable sync and scan generator. It has two ports based at \$9C00 and \$9C01. It is recommended that the reader consult Motorola, Hitachi, Rockwell, or Synertek supplied documentation. Register initialization are as follows:

| Register | Description | Initialization (decimal) |
|----------|--------------------------|--------------------------|
| R0 | Horizontal total-1 | 40 |
| R1 | Horizontal displayed | 32 |
| R2 | Horizontal sync position | 35 |
| R3 | Sync pluse width | 03 |
| R4 | Vertical total-1 | 31 |
| R5 | Vertical hold adjust | 17 |
| R6 | Vertical displayed | 32 |
| R7 | Vertical sync position | 32 |
| R9 | Scan lines per row-1 | 07 |

TABLE 3-2 REGISTER INITIALIZATION

All other registers are cleared. The interlace capability which differentiates the various types is not used in this application.

3.3 DATA/SOUND BOARD

The Data Processor runs synchronously to the Video Processor, as was described in this (Section Dual) Port Memory. All basic timing signals originate on the Video Processor Board and are bussed onto the Data Processor Board. The Sound Processor and Amplifier circuitry also resides on this Board.

3.3.1 MEMORY MAP

The following devices are available for access to the Data Processor.

| | | |
|----|--------|--------------------------------|
| A. | \$8000 | Dual Port Memory |
| B. | \$8400 | Local Memory |
| C. | \$8800 | ACIA Base Address |
| D. | \$8C00 | Video FIRQ Activation Address |
| | \$8C01 | Data FIRQ Deactivation Address |
| E. | \$9000 | Sound PIA |
| F. | \$9400 | Game PIA 1. |
| G. | \$9900 | Game PIA 2. |
| H. | \$9C00 | Game PIA 3. |

TABLE 3-3 DATA/SOUND MEMORY MAP
(\$=HEXADECIMAL)

3.3.2 DUAL PORT MEMORY

See discussion of Dual Port Memory under Video Processor Heading (Section 3.2).

3.3.3 LOCAL MEMORY

This is a 1K block of memory, U15 and U16, provided for scratch and work area for the Data Processor.

3.3.4 ACIA

A Motorola 6850 ACIA has been provided for diagnostic and other communications. Timing is generated by crystal oscillator Y1 - U23 and prescaled by U27 and U26. SW1 may be configured to allow one of eight baud rates (2 speeds may be software selected in the ACIA). Correct RS-232 levels are provided by U25 and U21.

3.3.5 BI-DIRECTIONAL FIRQ CAPABILITY

Any access of \$8C00 will generate a FIRQ to the Video Processor. Any access of \$8C01 will remove FIRQ generated by the Video Processor to the Data Processor. This is accomplished by U7, U8, and U9, which resides on the Video Board.

3.3.6 SOUND PIA

Both ports of PIA U20 have been dedicated to the control of the Sound Processor. Port A is used to select a sound number, which is initiated by strobbing the U20 (CA2) - U8 (CA1) interrupt line. Responses can be made using the reverse U8 (CA2) - U20 (CA1) interrupt. Port B is used to control the amplitude of the generated sound to the Stereo Amplifiers. The output of side B go to U24 and U28, which vary the ratio of the voltage divider across the non-inverting inputs of U29 and U30. This allows balance control of the sound to coincide with real time events occurring on the screen.

3.3.7 GAME PIA'S

Three 6820's are provided for interfacing with Play Controls and Coin Door Switches. These are located on the Game Board and are accessed through a Jumper Cable J16 and J15 respectively.

3.3.8 SOUND PROCESSOR

A Motorola 6802 also resides on the Data Board for sound generation. This Processor runs at 3.68MHz and accesses only two devices, PIA'S U7 and U8. U8 as mentioned previously, interface to the Data Processor. It also is the digital to analog output of the Sound Processor. Data from Port B is presented to U13. The current based output is converted to a voltage output by Q1, and controlled in amplitude by a potentiometer placed across J8. Speech circuitry is mixed with sound by R9, and the sum is sent to the Amplifiers. U7 controls the speech synthesis chip U19. The speech signal is shaped and filtered by the multipole bandpass filter U18.

3.4 ROM/I/O/ BOARD

This board contains the Program ROM for both the Data, Video and Sound Processors, along with the PIA'S needed to interface control, coils, lamps, etc.

3.4.1 GAME PIA'S

Three Game PIA'S are located on this board \$9400, \$9900, \$9C00. These devices, U11, U20, and U30 respectively, interface through noise control circuits A or B filters for those lines dedicated to inputs. Eleven (11) High Current Drivers have been provided utilizing circuit C. Each of these is capable of switching a 1.5AMP/24Volt DC load to ground.

3.4.2 ROM'S

Eight ROM locations are provided for the Data Processor, U12 - U19. These are selected by U21. Eight ROM'S, U3 - U10 selected by U2 are dedicated to the Video Processor. Sounds are supported by ROM'S U25, U26, and U27, with select U28.

ROM Bank U3 - U10 may consist of either 2716 or 2732 type EPROMS as determined by a jumper plug inserted in U1. It is assumed that all such EPROMS in the bank are of the same type. Likewise, ROM Bank U12 - U19 is determined by jumper plug at U22 ROM Bank jumpering for 2716's is as follows: Pin 1-14, 2-13, 3-12, 4-11 and 5-10. The highest address EPROM is U10, U19, or U27 in each bank with addresses of adjacent sockets progressing downward in \$800 byte blocks.

Jumpering for 2732's is as follows: Pin 2-14, 3-13, 4-12, 5-11, and 6-10. The highest address EPROM is U10, U19, or U27 in each bank with addresses of adjacent sockets progressing downward in \$1000 byte blocks.

3.5 SOFTWARE SECURITY MODULE

ENCRYPTION MODULE

Taito America's video system is designed to operate with a proprietary Encryption Module taking the place of the CPU.

This 40-Pin Module has the same logic and timing characteristics as the 6809E CPU it replaces, however, the module permits operation codes stored in EPROMS to be inciphered.

Troubleshooting is accomplished either through the Self Test capability discussed in Section 2 or by use of the "Taito Tech" Test Set which provides additional tests, monitor functions and support signature analysis by means of a self contained 6809E CPU.

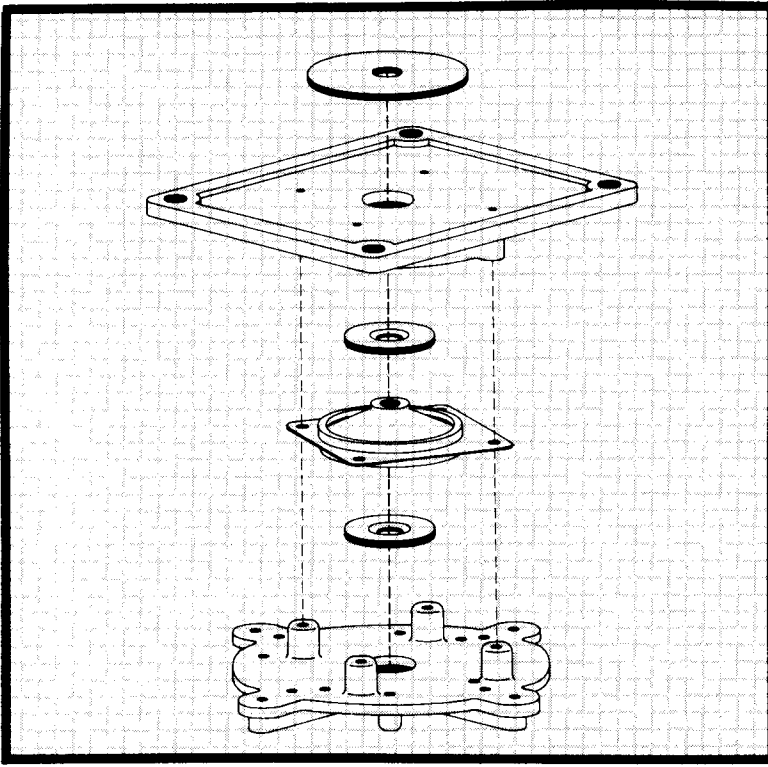


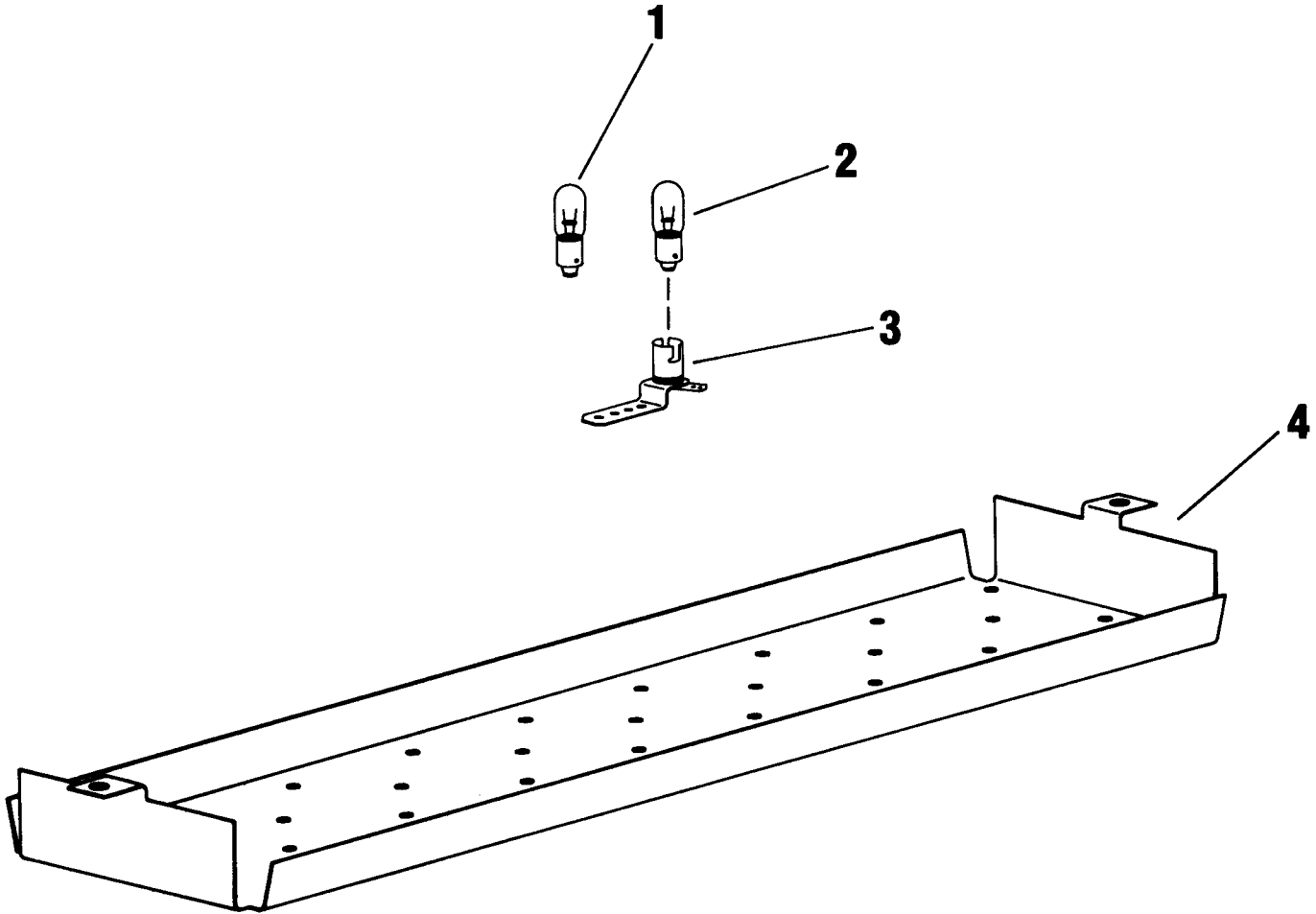
Illustration & Parts Lists

4

INCANDESCENT PANEL

FIGURE 1

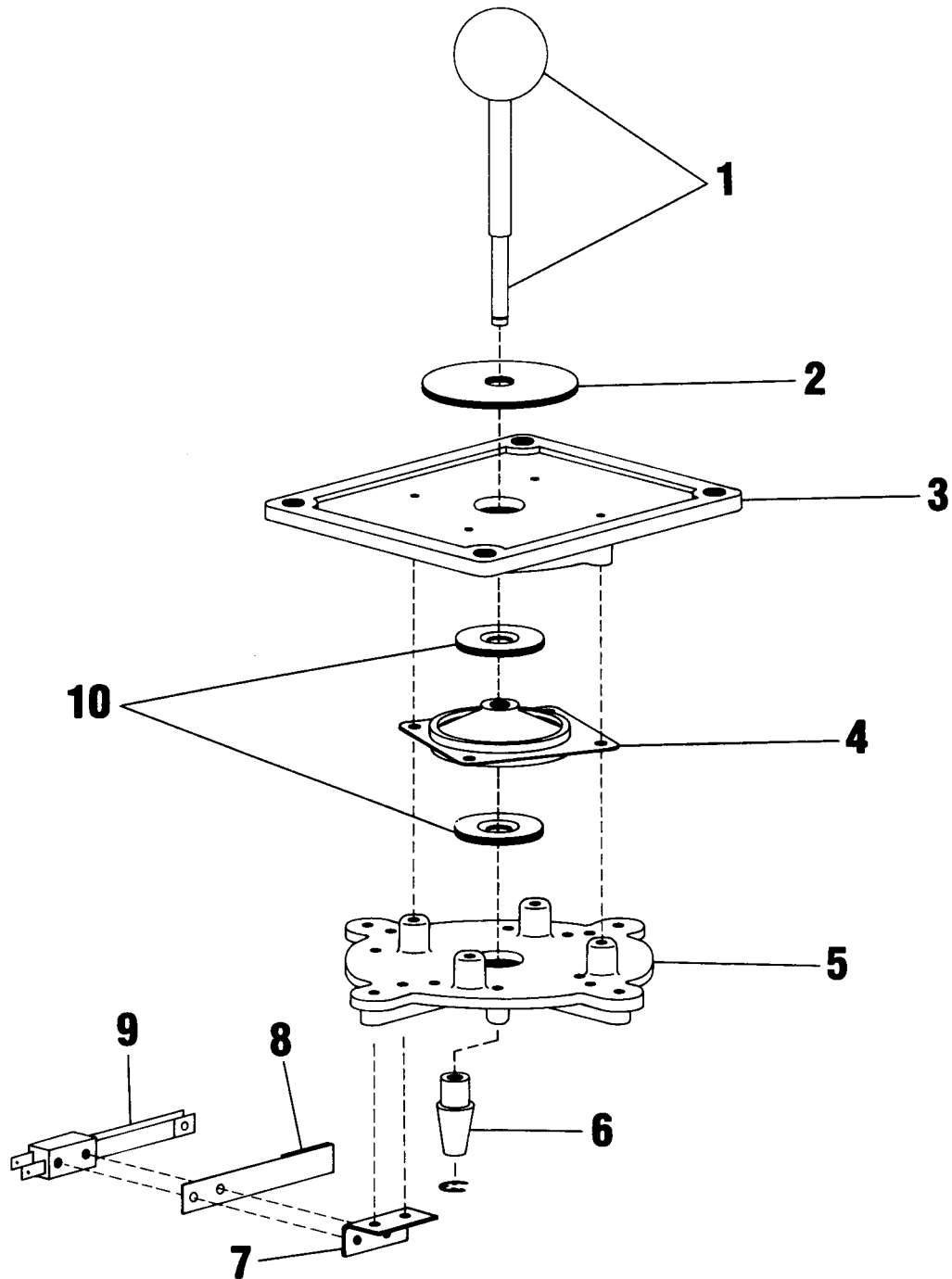
| ITEM | TAITO PART NO. | DESCRIPTION |
|------|----------------|------------------------|
| 1 | 27-00005-001 | Lamp #455 (Flasher) |
| 2 | 27-00006-001 | Lamp #47 |
| 3 | 26B00009-001 | Bayonet Base Socket |
| 4 | 26B00009-001 | Marquee Lighting Plate |



4-WAY JOYSTICK

FIGURE 2

| ITEM | TAITO PART NO. | DESCRIPTION |
|------|----------------|-----------------|
| 1 | 63A00031-001 | Ball & Shaft |
| 2 | 63A00021-001 | Mask |
| 3 | 63C00027-001 | Mounting Plate |
| 4 | 62A00002-001 | Shock Mount Pad |
| 5 | 63A00028-002 | Switch Plate |
| 6 | 63A00030-001 | Actuator |
| 7 | 61A00078-001 | "L" Bracket |
| 8 | 63A00026-001 | Switch Spacer |
| 9 | 29B00016-002 | Leaf Switch |
| 10 | 63A00029-001 | Spacer |



CONTROL PANEL

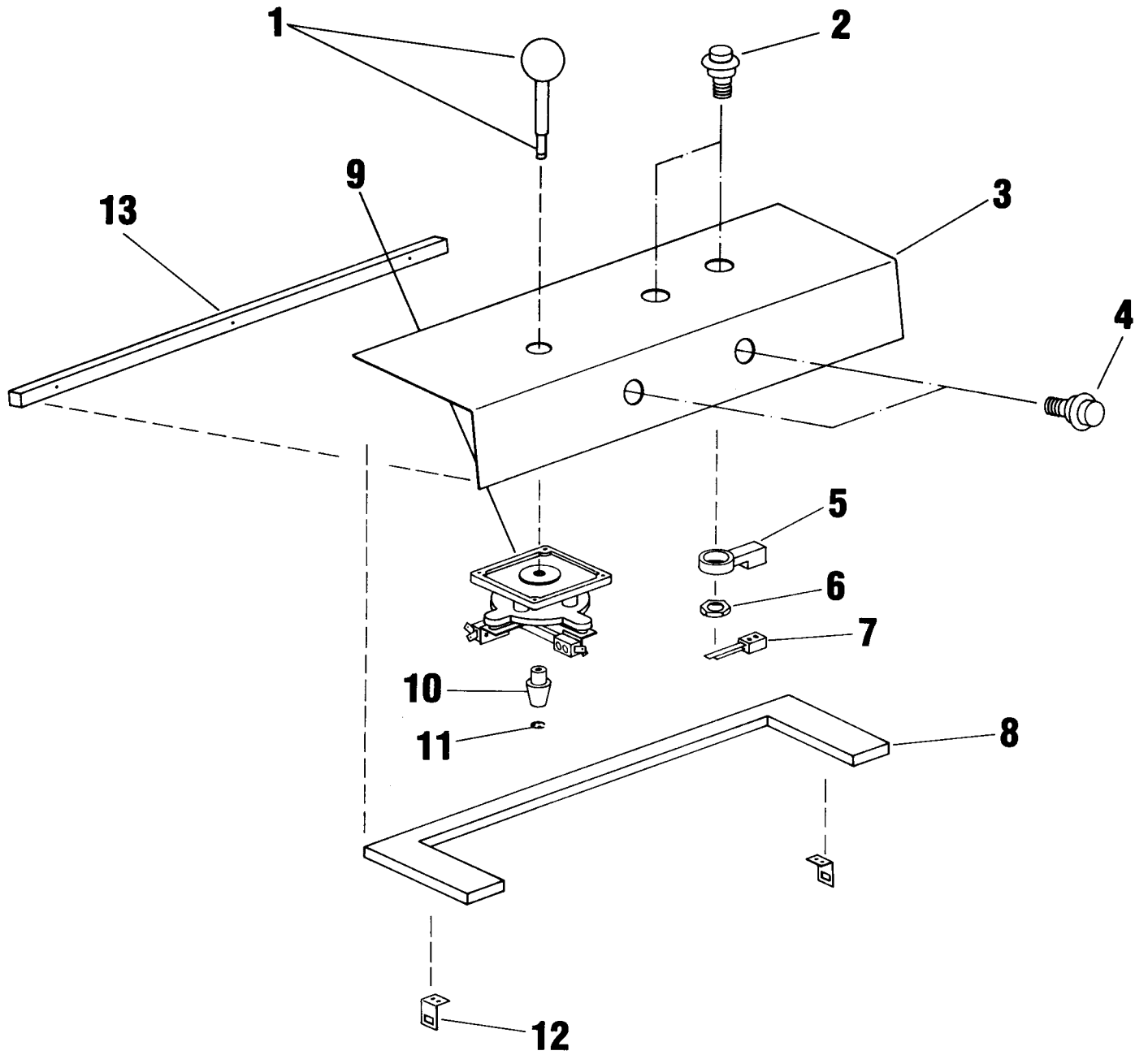
FIGURE 3

| ITEM | TAITO PART NO. | DESCRIPTION |
|------|----------------|-----------------------------|
| 1 | 63B00031-001 | Ball & Shaft |
| 2 | 63B00024-002 | Push Button (Red) |
| 3 | 07M00051-001 | Control Panel |
| 4 | 63B00024-001 | Push Button (White) |
| 5 | 63C00025-001 | Switch Support |
| 6 | 54A07001-008 | Stamped Nut 5/8-11 |
| 7 | 29B00016-001 | Leaf Switch |
| 8 | 42D00017-001 | Dash Panel |
| 9 | 63D00032-004 | Control (4-Way Leaf Switch) |
| 10 | 63B00030-001 | Actuator |
| 11 | 59B00020-017 | "E" Ring |
| 12 | 61A00015-001 | Strike Hook |
| 13 | 12B00108-001 | Cleat |
| *14 | 63-00050-001 | Decal, Lexan |

*Item not shown on drawing.

CONTROL PANEL

FIGURE 3



DOOR ASSEMBLY

FIGURE 4

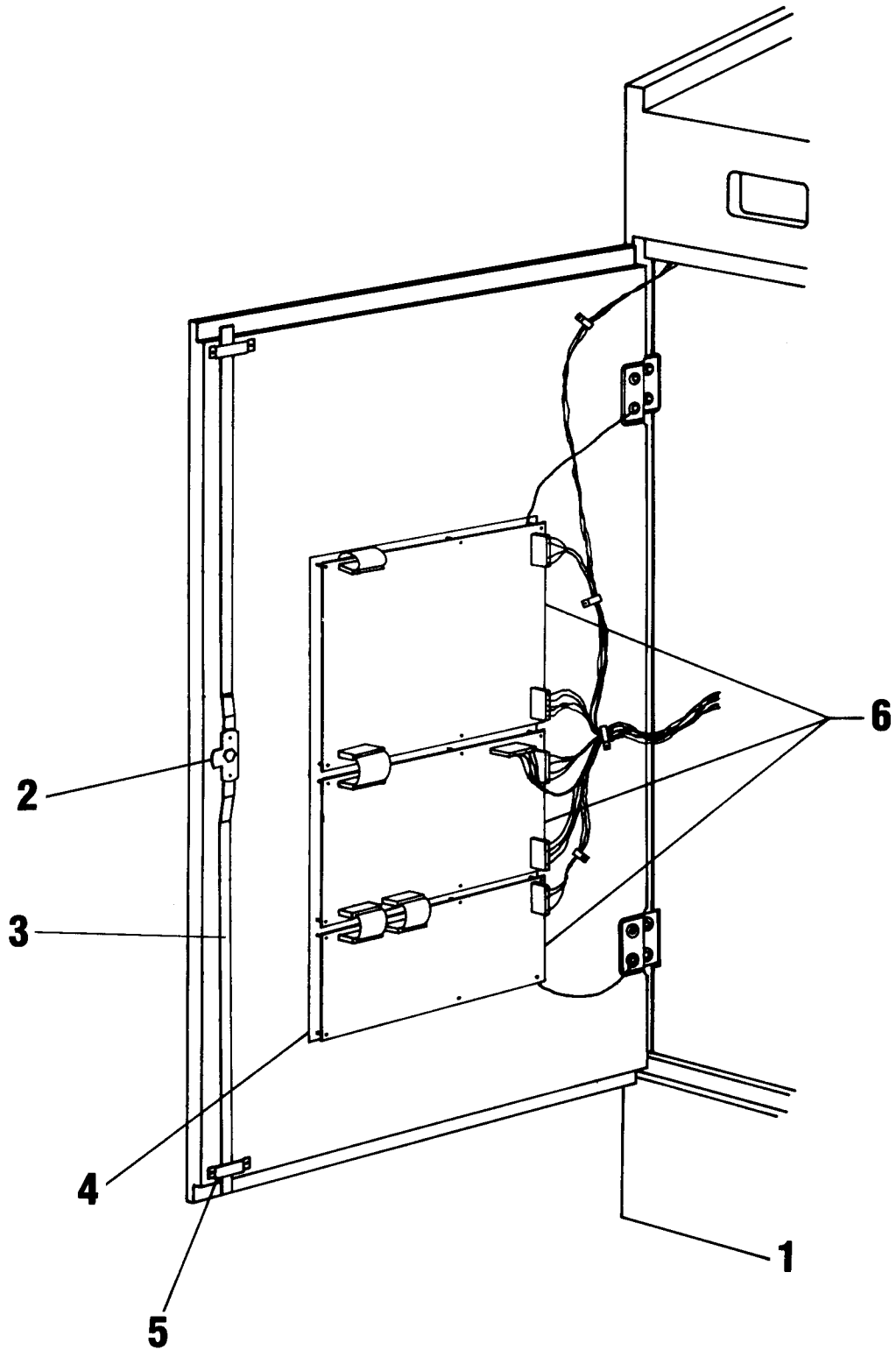
| ITEM | TAITO PART NO. | DESCRIPTION |
|------|----------------|---------------------------|
| 1 | 42D00067-001 | Door Assembly |
| 2 | 04-00037-002 | Lock Kit |
| 3 | 61B00142-001 | Lock Rod Assembly |
| 4 | 61D00079-001 | P.C. Board Mounting Plate |
| 5 | 61A00111-001 | Rod Lock Bracket |
| 6 | 08M00018-001 | Game P.C. Board Assembly |
| *7 | 79-00031-001 | L.E.D. Values Sheet |

*Item not shown on drawing.

NOTES

DOOR ASSEMBLY

FIGURE 4

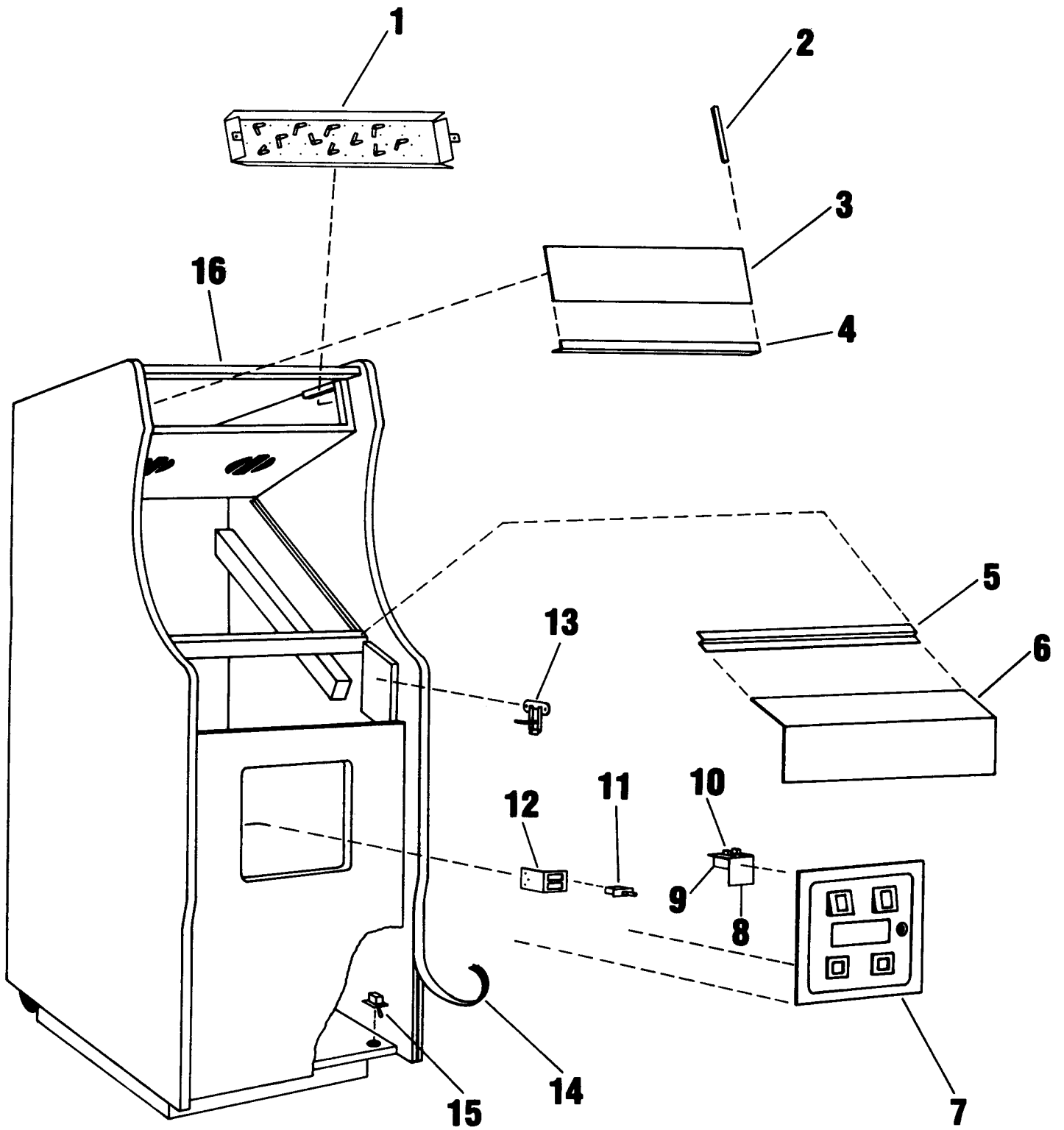


CABINET ASSEMBLY UPRIGHT FRONT VIEW**FIGURE 5**

| ITEM | TAITO PART NO. | DESCRIPTION |
|-------------|---------------------------|-----------------------------|
| 1 | 07M00055-001 | Incandescent Panel |
| 2 | 63B00006-001 | "U" Channel Bracket |
| 3 | 47D00012-002 | Marquee |
| 4 | 61C00115-001 | Marquee Retaining Bracket |
| 5 | 61D00012-001 | Lower Cover Glass |
| 6 | 07M00052-001 | Control Panel Assembly |
| 7 | 07-00050-001 | Coin Door |
| 8 | 61B00113-001 | Switch Bracket |
| 9 | 07M00057-001 | Service Switch Assembly |
| 10 | 29-00022-001 | Slide, Center Return Switch |
| 11 | 29B00015-001 | Interlock Switch |
| 12 | 61B00114-001 | Interlock Switch Bracket |
| 13 | 59-00008-001 | Latching Clamp |
| 14 | 63B00002-004 | "T" Molding |
| 15 | 29A00023-001 | Power ON/OFF Switch |
| 16 | 41D00009-001 | Finish Cabinet |

CABINET ASSEMBLY UPRIGHT FRONT VIEW

FIGURE 5

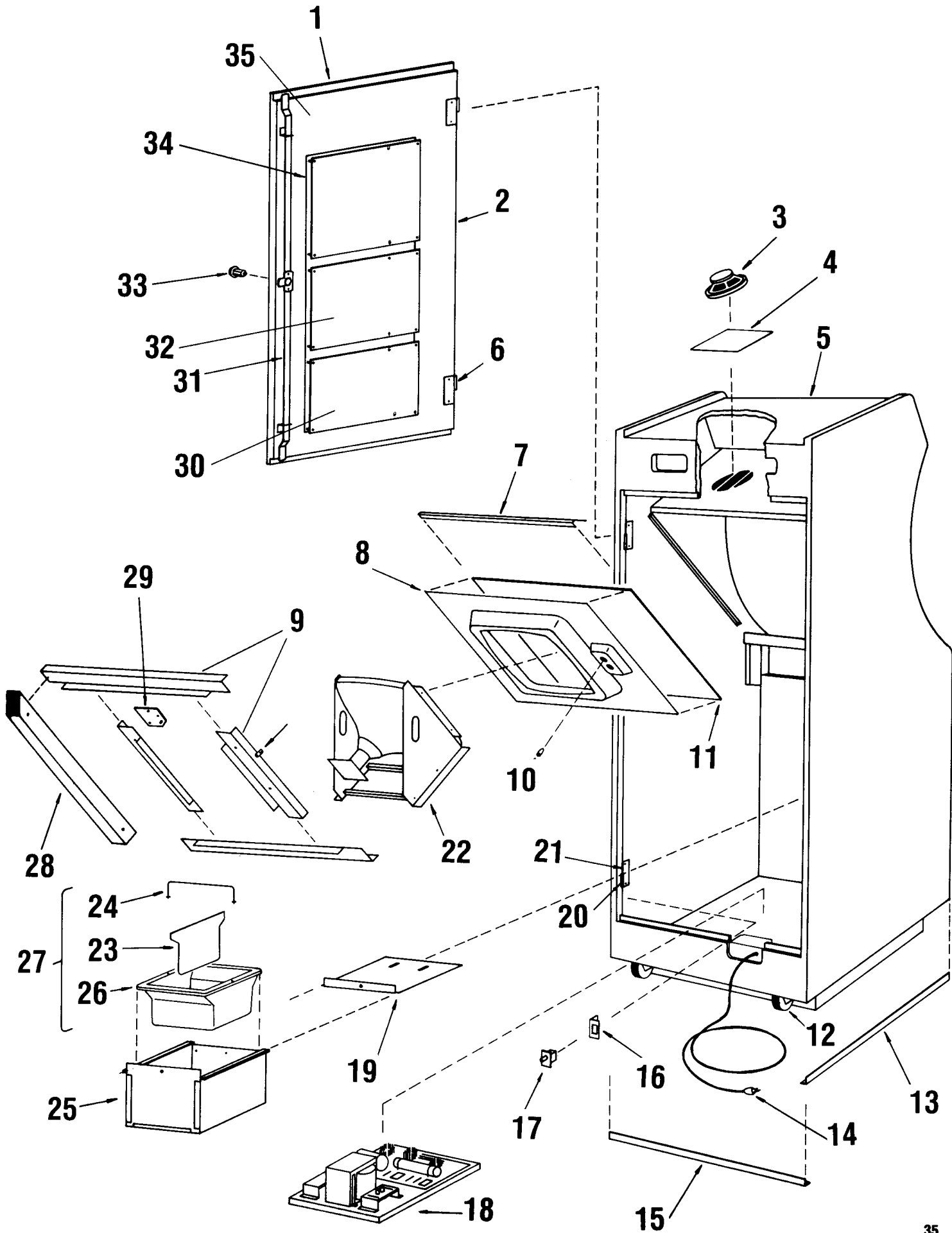


CABINET ASSEMBLY UPRIGHT REAR VIEW**FIGURE 6**

| ITEM | TAITO PART NO. | DESCRIPTION |
|-------------|-----------------------|--------------------------------|
| 1 | 42D00069-001 | Door & Board Mounting Assembly |
| 2 | 42D00016-001 | Door Panel |
| 3 | 21C00003-001 | Speaker 6" round |
| 4 | 61B00027-001 | Speaker Grill |
| 5 | 41D00009-002 | Finished Cabinet |
| 6 | 61B00057-001 | Leaf Hinge |
| 7 | 61C00006-001 | Upper Cover Glass Bracket |
| 8 | 63C00035-001 | Monitor Shroud |
| 9 | 61C00080-001 | Monitor Mounting Bracket |
| 10 | 27-00006-001 | #47 Bulb, Lighted Instr. |
| 11 | 47D00013-002 | Cover Glass |
| 12 | 44C00001-001 | Wheels |
| 13 | 63C00005-004 | "L" Molding |
| 14 | 07M00042-001 | A/C Line Cord Assembly |
| 15 | 63C00005-022 | "L" Molding |
| 16 | 61B00030-002 | Interlock Bracket |
| 17 | 29B00015-001 | Interlock Switch |
| 18 | 07M00039-001 | Power Supply |
| 19 | 61C00054-001 | Cash Box Lid |
| 20 | 61B00056-001 | Leaf Hinge |
| 21 | 61A00055-001 | Hinge Pin |
| 22 | 31-00006-001 | 19" Color Monitor |
| 23 | 63-00019-001 | Cash Tray Separator |
| 24 | 61-00039-001 | Cash Tray Handle |
| 25 | 61C00060-001 | Cash Box |
| 26 | 63-00010-001 | Cash Tray (Only) |
| 27 | 07M00054-001 | Cash Tray Assembly |
| 28 | 42C00013-001 | Monitor Support Cleat |
| 29 | 61C00086-001 | Corner Bracket |
| 30 | 08-00002-001 | Data/Sound P.C.B. |
| 31 | 61B00142-001 | Lock Rod Assembly |
| 32 | 08-00003-001 | ROM/IO P.C.B. |
| 33 | 04M00037-002 | Lock Kit |
| 34 | 08-00001-001 | Video Processor P.C.B. |
| 35 | 61D00079-001 | P.C.B. Mtg. Plate |

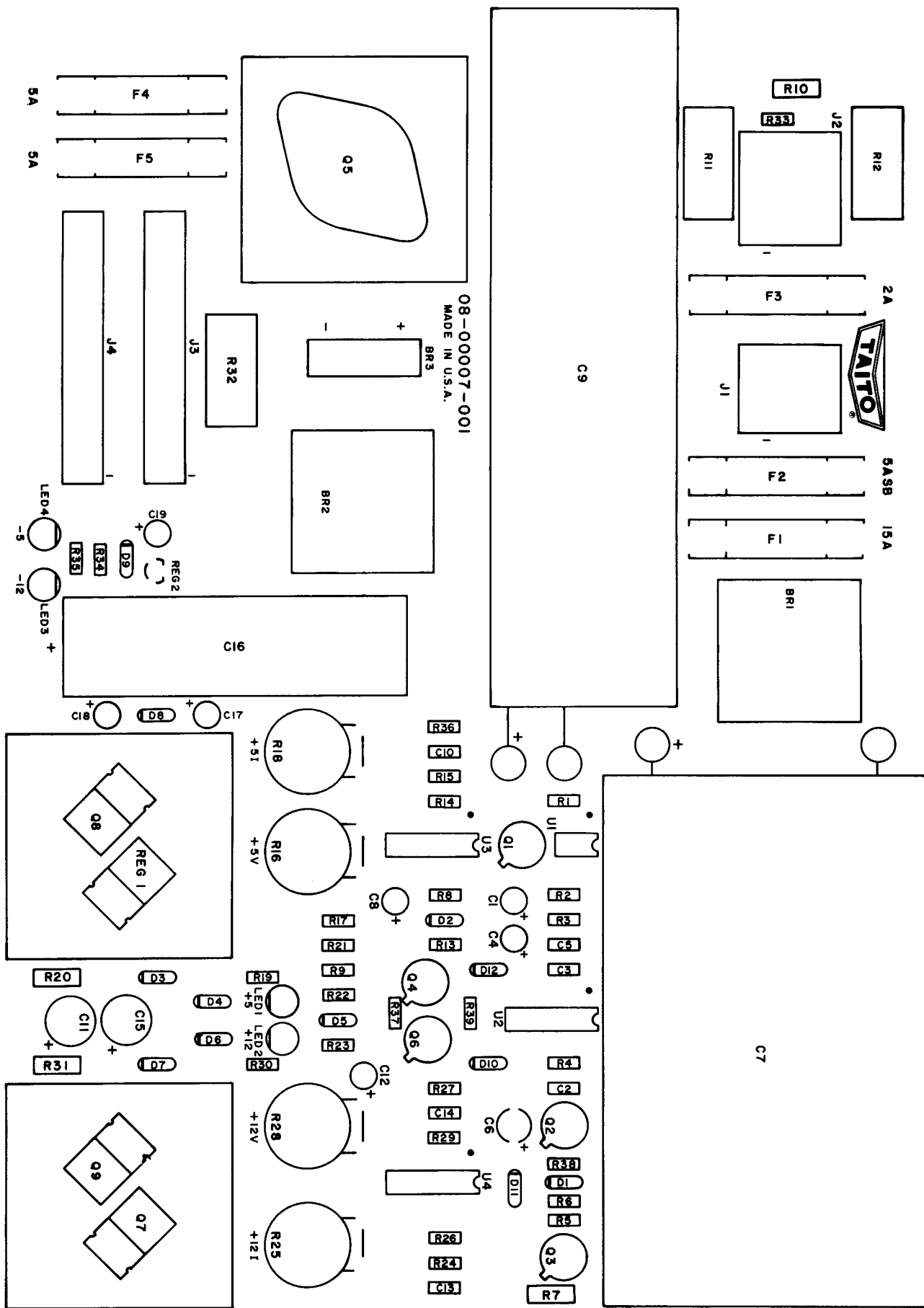
CABINET ASSEMBLY UPRIGHT REAR VIEW

FIGURE 6



POWER SUPPLY COMPONENT LAYOUT

FIGURE 7



POWER SUPPLY

FIGURE 7

| SYM | TAITO PART NO. | DESCRIPTION |
|-----|----------------|-------------------------------|
| R1 | 11-00001-102 | Resistor 1.0K 5% ¼W 5% |
| R2 | 11-00001-512 | Resistor 5.1K ¼W 5% |
| R3 | 11-00001-183 | Resistor 18K ¼W 5% |
| R4 | 11-00001-224 | Resistor 220K ¼W 5% |
| R5 | 11-00001-472 | Resistor 4.7K ¼W 5% |
| R6 | 11-00001-222 | Resistor 2.2K ¼W 5% |
| R7 | 11-10001-101 | Resistor 100 ¼W 5% |
| R8 | 11-00001-102 | Resistor 10K ¼W 5% |
| R9 | 11-00001-472 | Resistor 4.7K ¼W 5% |
| R10 | 11-10001-101 | Resistor 100 ½W 5% |
| R11 | 11-30001-015 | Resistor .15 4W 5% |
| R12 | 11-30001-015 | Resistor .15 4W 5% |
| R13 | 11-00001-472 | Resistor 4.7K ¼W 5% |
| R14 | 11-00001-222 | Resistor 2.2K ¼W 5% |
| R15 | 11-00001-222 | Resistor 2.2K ¼W 5% |
| R16 | 11-60001-252 | Pot 2.5K ¼W 20% |
| R17 | 11-00001-222 | Resistor 2.2K ¼W 5% |
| R18 | 11-60001-102 | Pot 1.0K ¼W 20% |
| R19 | 11-00001-511 | Resistor 510 ¼W 5% |
| R20 | 11-10001-470 | Resistor 47 ½W 5% |
| R21 | 11-00001-162 | Resistor 1.6K ¼W 5% |
| R22 | 11-00001-103 | Resistor 10K ¼W 5% |
| R23 | 11-00001-472 | Resistor 4.7K ¼W 34 |
| R24 | 11-00001-222 | Resistor 2.2K ¼W 5% |
| R25 | 11-60001-102 | Pot 1.0K ¼W 5% |
| R26 | 11-00001-472 | Resistor 407K ¼W 5% |
| R27 | 11-00001-222 | Resistor 2.2K ¼W 5% |
| R28 | 11-60001-252 | Pot 2.5K ¼W 20% |
| R29 | 11-00001-472 | Resistor 4.7K ¼W 5% |
| R30 | 11-00001-122 | Resistor 1.2K ¼W 5% |
| R31 | 11-10001-470 | Resistor 47 ¼W 5% |
| R32 | 11-30001-015 | Resistor .15 4W 5% |
| R33 | 11-00001-222 | Resistor 2.2K ¼W 5% |
| R34 | 11-00001-122 | Resistor 1.2K ¼W 5% |
| R35 | 11-00001-511 | Resistor 510 ¼W 5% |
| R36 | 11-00001-222 | Resistor 2.2K ¼W 5% |
| R37 | 11-00001-104 | Resistor 100K |
| R38 | 11-00001-103 | Resistor 10K ¼W 5% |
| R39 | 11-00001-224 | Resistor 220L ¼W 5% |
| C1 | 12-30001-225 | Capacitor, Tantalum 2.2uf 25V |
| C2 | 12-10004-103 | Capacitor, Ceramic .01uf |
| C3 | 12-10004-103 | Capacitor, Ceramic .01uf |
| C4 | 12-30001-105 | Capacitor, Tantalum 1.uf 35V |

| SYM | TAITO PART NO. | DESCRIPTION |
|------|----------------|----------------------------------|
| C5 | 12-10001-102 | Capacitor, .001uf |
| C6 | 12-30001-106 | Capacitor, Tantalum 10uf |
| C7 | 12-20003-509 | Capacitor, Electrolytic 50,000uf |
| C8 | 12-30001-105 | Capacitor, Tantalum 1.uf 35V |
| C9 | 12-20003-209 | Capacitor, Electrolytic 20,000uf |
| C10 | 12-10001-332 | Capacitor, Ceramic .0033uf |
| C11 | 12-30001-476 | Capacitor, Tantalum 47uf |
| C12 | 12-30001-105 | Capacitor, Tantalum 1.uf 35V |
| C13 | 12-10004-103 | Capacitor, Ceramic .01uf |
| C14 | 12-10001-102 | Capacitor, .001uf |
| C15 | 12-30001-476 | Capacitor, Tantalum 47uf |
| C16 | 12-20002-108 | Capacitor, Electrolytic 1,000uf |
| C17 | 12-30001-225 | Capacitor, Tantalum 2.2uf 25V |
| C18 | 12-30001-225 | Capacitor, Tantalum 2.2uf 25V |
| C19 | 12-30001-105 | Capacitor, Tantalum 1.uf 35V |
| F1 | 24-00003-010 | 10A Fuse |
| F2 | 24-00003-010 | 10A Fuse |
| F3 | 24-00003-003 | Fuse, 2A |
| F4 | 24-00003-004 | Fuse, 4A |
| F5 | 24-00003-004 | Fuse, 4A |
| BR1 | 13-00100-025 | Diode Bridge 25A, 100V |
| BR2 | 13-00100-012 | Diode Bridge 12A, 100V |
| BR3 | 13-00100-002 | Diode Bridge 2A, 100V |
| D1 | 13-14002-001 | Diode IN4002 |
| D2 | 13-14002-001 | Diode IN4002 |
| D3 | 13-10752-001 | Diode, Zener IN752 |
| D4 | 13-14002-001 | Diode IN4002 |
| D5 | 13-14002-001 | Diode IN4002 |
| D6 | 13-14002-001 | Diode IN4002 |
| D7 | 13-10964-001 | Diode, Zener IN964 |
| D8 | 13-14002-001 | Diode IN4002 |
| D9 | 13-14002-001 | Diode IN4002 |
| D10 | 13-14002-001 | Diode IN4002 |
| D11 | 13-14002-001 | Diode IN4002 |
| D12 | 13-14002-001 | Diode IN4002 |
| LED1 | 13-00001-001 | LED (Red) |
| LED2 | 13-00001-001 | LED (Red) |
| LED3 | 13-00001-001 | LED (Red) |
| LED4 | 13-00001-001 | LED (Red) |
| U1 | 15-62500-001 | Opto Coupler H11AA2 |
| U2 | 15-50556-001 | Timer (Dual) 556 |
| U3 | 15-50723-001 | Voltage Regulator 723 |
| U4 | 15-50723-001 | Voltage Regulator 723 |

POWER SUPPLY

FIGURE 7

| SYM | TAITO PART NO. | DESCRIPTION |
|------------|---------------------------|-----------------------------|
| REG1 | 15-57912-001 | Voltage Regulator 7912 |
| REG2 | 15-57905-001 | Voltage Regulator 79L05 |
| Q1 | 14-22905-001 | Transistor 2N2905 |
| Q2 | 14-22905-001 | Transistor 2N2905 |
| Q3 | 14-22905-001 | Transistor 2N2905 |
| Q4 | 14-22905-001 | Transistor 2N2905 |
| Q5 | 14-23055-001 | Transistor 2N3055 |
| Q6 | 14-22905-001 | Transistor 2N2905 |
| Q7 | 14-20030-001 | Transistor TIP-30A |
| Q8 | 14-26401-001 | SCR 2N6401 |
| Q9 | 14-26401-001 | SCR 2N6401 |
| J1 | 25-00022-006 | Connector, 1-380999-0 6Pin |
| J2 | 25-00022-008 | Connector, 350212-1 8Pin |
| J3 | 25-00002-014 | Connector, 09-60-1141 14Pin |
| J4 | 25-00002-014 | Connector, 09-60-1140 14Pin |
| | 24-10001-001 | Fuse Clips |
| | 30-00220-002 | Heat Sink Dual To-220 |
| | 30-00003-001 | Heat Sink Single To-3 |

VIDEO PROCESSOR

FIGURE 8

| SYM | TAITO PART NO. | DESCRIPTION |
|------|----------------|--|
| C99 | 12-10002-104 | Capacitor Ceramic, .1uf,50V, +80/-20% |
| C100 | 12-10002-104 | Capacitor Ceramic, .1uf,50V, +80/-20% |
| C101 | 12-10003-100 | Capacitor Ceramic, 10pf,10% NPO Axial Lead 20% |
| C102 | 12-10002-104 | Capacitor Ceramic, .1uf,50V, +80/-20% |
| C103 | 12-10002-104 | Capacitor Ceramic, .1uf,50V, +80/-20% |
| C104 | 12-10002-104 | Capacitor Ceramic, .1uf,50V, +80/-20% |
| C105 | 12-10002-104 | Capacitor Ceramic, .1uf,50V, +80/-20% |
| C106 | 12-10002-104 | Capacitor Ceramic, .1uf,50V, +80/-20% |
| C107 | 12-10002-104 | Capacitor Ceramic, .1uf,50V, +80/-20% |
| C108 | 12-10002-104 | Capacitor Ceramic, .1uf,50V, +80/-20% |
| C113 | 12-10001-471 | Capacitor Ceramic, 50V, 10% 470PF Axial Lead |
| R1 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R2 | 11-00001-152 | Resistor 1.5K, ¼W, 5% |
| R3 | 11-00001-271 | Resistor 270 OHM, ¼W, 5% |
| R4 | 11-00001-271 | Resistor 270 OHM, ¼W, 5% |
| R5 | 11-00001-271 | Resistor 270 OHM, ¼W, 5% |
| R6 | 11-00001-332 | Resistor 3.3K, ¼W, 5% |
| R7 | 11-00001-221 | Resistor 220 OHM, ¼W, 5% |
| R8 | 11-00001-222 | Resistor 2.2K, ¼W, 5% |
| R9 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R10 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R11 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R12 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R13 | 11-00001-820 | Resistor 82 OHM, ¼W, 5% |
| R14 | 11-00001-181 | Resistor 180 OHM, ¼W, 5% |
| R15 | 11-00001-271 | Resistor 270 OHM, ¼W, 5% |
| R16 | 11-00001-151 | Resistor 150 OHM, ¼W, 5% |
| R17 | 11-00001-151 | Resistor 150 OHM, ¼W, 5% |
| R18 | 11-00001-271 | Resistor 270 OHM, ¼W, 5% |
| R19 | 11-00001-181 | Resistor 180 OHM, ¼W, 5% |
| R20 | 11-00001-820 | Resistor 82 OHM, ¼W, 5% |
| R21 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R22 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R23 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R24 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R25 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R26 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R27 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R28 | 11-00001-181 | Resistor 180 OHM, ¼W, 5% |
| R29 | 11-00001-471 | Resistor 470 OHM, ¼W, 5% |
| R30 | 11-00001-471 | Resistor 470 OHM, ¼W, 5% |
| R31 | 11-00001-471 | Resistor 470 OHM, ¼W, 5% |
| R32 | 11-00001-471 | Resistor 470 OHM, ¼W, 5% |
| R33 | 11-00001-471 | Resistor 470 OHM, ¼W, 5% |
| R34 | 11-00001-681 | Resistor 680 OHM, ¼W, 5% |
| R35 | 11-00001-391 | Resistor 390 OHM, ¼W, 5% |
| R36 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |

| SYM | TAITO PART NO. | DESCRIPTION |
|------|----------------|---------------------------------|
| R37 | 11-00001-473 | Resistor 47K OHM, ¼W, 5% |
| R38 | 11-00001-332 | Resistor 3300 OHM, ¼W, 5% |
| R39 | 11-00001-331 | Resistor 330 OHM, ¼W, 5% |
| R40 | 11-00001-331 | Resistor 330 OHM, ¼W, 5% |
| R41 | 11-00001-331 | Resistor 330 OHM, ¼W, 5% |
| R42 | 11-00001-331 | Resistor 330 OHM, ¼W, 5% |
| R43 | 11-00001-331 | Resistor 330 OHM, ¼W, 5% |
| R44 | 11-00001-331 | Resistor 330 OHM, ¼W, 5% |
| R45 | 11-00001-151 | Resistor 150 OHM, ¼W, 5% |
| R46 | 11-00001-820 | Resistor 82 OHM, ¼W, 5% |
| R47 | 11-00001-471 | Resistor 470 OHM, ¼W, 5% |
| R48 | 11-00001-181 | Resistor 180 OHM, ¼W, 5% |
| R49 | 11-00001-271 | Resistor 270 OHM, ¼W, 5% |
| R50 | 11-00001-473 | Resistor 47K OHM, ¼W, 5% |
| R51 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R52 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R53 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R54 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R55 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R56 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R57 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R58 | 11-00001-330 | Resistor 33 OHM, ¼W, 5% |
| R59 | 11-00001-473 | Resistor 47K OHM, ¼W, 5% |
| R60 | 11-00001-332 | Resistor 3300 OHM, ¼W, 5% |
| R61 | 11-00001-391 | Resistor 390 OHM, ¼W, 5% |
| R62 | 11-00001-332 | Resistor 3.3K, ¼W, 5% |
| R63 | 11-00001-102 | Resistor 1K, ¼W, 5% |
| R64 | 11-00001-121 | Resistor 120 OHM, ¼W, 5% |
| R65 | 11-00001-151 | Resistor 150 OHM, ¼W, 5% |
| R66 | 11-00001-332 | Resistor 3.3K, ¼W, 5% |
| R67 | 11-00001-332 | Resistor 3300 OHM, ¼W, 5% |
| R68 | 11-00001-332 | Resistor 3.3K, ¼W, 5% |
| R69 | 11-00001-332 | Resistor 3.3K, ¼W, 5% |
| FB1 | 17-00001-001 | Ferrite Bead |
| FB2 | 17-00001-001 | Ferrite Bead |
| FB3 | 17-00001-001 | Ferrite Bead |
| FB4 | 17-00001-001 | Ferrite Bead |
| FB5 | 17-00001-001 | Ferrite Bead |
| FB6 | 17-00001-001 | Ferrite Bead |
| FB7 | 17-00001-001 | Ferrite Bead |
| FB8 | 17-00001-001 | Ferrite Bead |
| FB9 | 17-00001-001 | Ferrite Bead |
| FB10 | 17-00001-001 | Ferrite Bead |
| FB14 | 17-00001-001 | Ferrite Bead |
| Q1 | 14-23904-001 | Transistor NPN Silicon (2N3904) |
| Q2 | 14-23904-001 | Transistor NPN Silicon (2N3904) |
| Q3 | 14-23904-001 | Transistor NPN Silicon (2N3904) |
| Q4 | 14-23904-001 | Transistor NPN Silicon (2N3904) |

VIDEO PROCESSOR

FIGURE 8

| SYM | TAITO PART NO. | DESCRIPTION |
|------|----------------|------------------------------------|
| Q5 | 14-23904-001 | Transistor NPN Silicon (2N3904) |
| Q6 | 14-23904-001 | Transistor NPN Silicon (2N3904) |
| Q7 | 14-23904-001 | Transistor NPN Silicon (2N3904) |
| Q8 | 14-23905-001 | Transistor NPN Silicon (2N3905) |
| LED1 | 13-00001-001 | L.E.D. RED, TL-1¼ |
| LED2 | 13-00001-001 | L.E.D. RED, TL-1¼ |
| LED3 | 13-00001-001 | L.E.D. RED, TL-1¼ |
| LED4 | 13-00001-001 | L.E.D. RED, TL-1¼ |
| LED5 | 13-00001-001 | L.E.D. RED, TL-1¼ |
| LED6 | 13-00001-001 | L.E.D. RED, TL-1¼ |
| Y1 | 19-00003-001 | CRYSTAL, 20,000MHZ |
| BATT | 20-00001-001 | Battery, NICAD, 3.6V, 1/3 AA |
| SW1 | 29-00017-001 | Switch Momentary |
| TP1 | 59-00021-001 | Test Point |
| TP2 | 59-00021-001 | Test Point |
| TP3 | 59-00021-001 | Test Point |
| TP4 | 59-00021-001 | Test Point |
| TP5 | 59-00021-001 | Test Point |
| TP6 | 59-00021-001 | Test Point |
| TP7 | 59-00021-001 | Test Point |
| TP8 | 59-00021-001 | Test Point |
| RP1 | 11-50001-102 | 1K OHM Resistor Sip Pack |
| RP2 | 11-50001-473 | 47K OHM Resistor Sip Pack |
| RP3 | 11-50001-332 | 3.3K Resistor Sip Pack |
| RP4 | 11-50001-332 | 3.3K Resistor Sip Pack |
| RP5 | 11-50001-332 | 3.3K Resistor Sip Pack |
| J1 | 25-00001-014 | Connector, 14 Pin .156 Center |
| J2 | 25-00002-014 | Connector, 14 Pin .156 Center |
| J3 | 25-00001-001 | Connector, 50 Pin Header Vertical |
| J6 | 25-00001-001 | Connector, 50 Pin Header Vertical |
| J19 | 25-00002-002 | Connector, 2 Pin .156 Center |
| W1 | 25-00021-002 | Connector .1 Center for W1 |
| W1 | 26-00007-001 | Shorting Pin |
| | 32-00001-001 | P.C.B. Video Processor Board |
| U1 | 15-20245-001 | Bus Transciever, Octal (74LS245) |
| U2 | 15-20245-001 | Bus Transciever, Octal (74LS245) |
| U3 | 15-10003-001 | Ram 1K x 4 NMOS Static (2114) |
| | 26-00001-018 | Socket DIP 18 Pin for U3 |
| U4 | 15-10003-001 | Ram 1K x 4 NMOS Static (2114) |
| | 26-00001-018 | Socket DIP 18 Pin for U4 |
| U5 | 15-20157-001 | Multiplexer Quad 2-Input (74LS157) |
| U6 | 15-20157-001 | Multiplexer Quad 2-Input (74LS157) |
| U7 | 15-20074-001 | Flip Flop, Dual D (74LS74) |
| U8 | 15-20032-001 | Quad 2 Input or (74LS32) |
| U9 | 15-20032-001 | Quad 2 Input or (74LS32) |
| U10 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U10 |

| SYM | TAITO PART NO. | DESCRIPTION |
|-----|----------------|--------------------------------------|
| U11 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U11 |
| U12 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U12 |
| U13 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U13 |
| U14 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U14 |
| U15 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U15 |
| U16 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U16 |
| U17 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U17 |
| U18 | 15-00003-001 | CRT CONTROLLER 68A45 |
| | 26-00001-040 | Socket DIP 40 Pin for U18 |
| U19 | 15-20086-001 | Quad 2 Input Exclusive or (74LS86) |
| U20 | 15-20086-001 | Quad 2 Input Exclusive or (74LS86) |
| U21 | 15-20157-001 | Multiplexer Quad 2-Input (74LS157) |
| U22 | 15-20032-001 | Quad 2 Input or (74LS157) |
| U23 | 15-20161-001 | Counter, 4 Bit Presettable (74LS161) |
| U24 | 15-20004-001 | Inverter, HEX (74LS04) |
| U25 | 15-70374-001 | Latch, Octal Shockey (74LS374) |
| U26 | 15-10001-001 | RAM 16K x1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U26 |
| U27 | 15-10001-001 | RAM 16K x1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U27 |
| U28 | 15-10001-001 | RAM 16K x1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U28 |
| U29 | 15-10001-001 | RAM 16K x1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U29 |
| U30 | 15-10001-001 | RAM 16K x1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U30 |
| U31 | 15-10001-001 | RAM 16K x1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U31 |
| U32 | 15-10001-001 | RAM 16K x1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U32 |
| U33 | 15-10001-001 | RAM 16K x1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U33 |
| U34 | 15-20374-001 | Latch, Octal (74LS374) |
| U35 | 15-20153-001 | Multiplexer, Dual 4-Input (74LS153) |
| U36 | 15-20074-001 | Flip Flop Dual-D (74LS74) |
| U37 | 15-20008-001 | Quad, 2-Input and (74LS08) |
| U38 | 15-70113-001 | Flip Flop JK Schottky (74LS113) |
| U39 | 15-20004-001 | Inverter, HEX (74LS04) |
| U40 | 15-30017-001 | Buffer/Driver, HEX (7417) |
| U41 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U41 |

VIDEO PROCESSOR

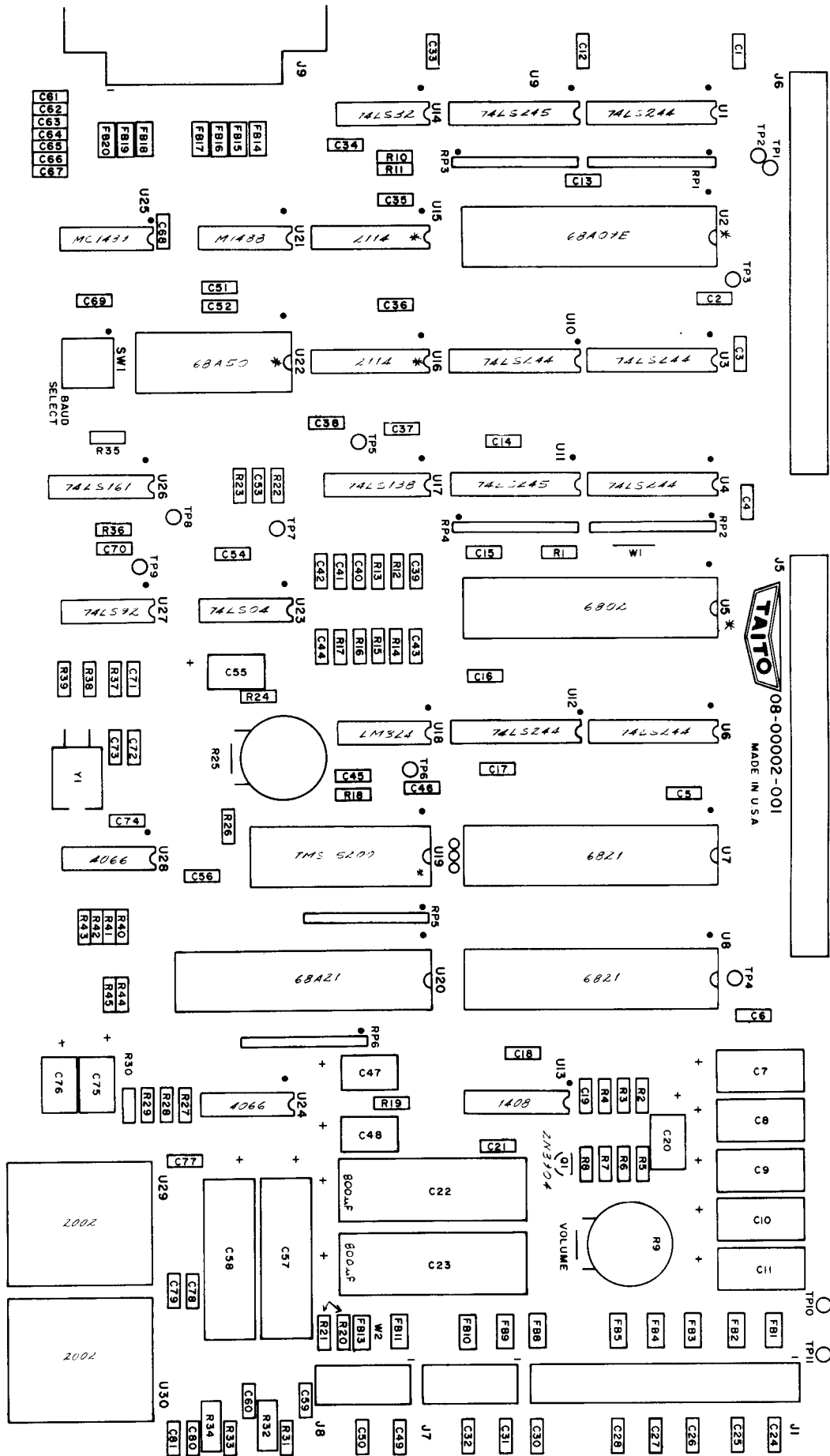
FIGURE 8

| SYM | TAITO PART NO. | DESCRIPTION |
|-----|----------------|-------------------------------------|
| U42 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U42 |
| U43 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U43 |
| U44 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U44 |
| U45 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U45 |
| U46 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U46 |
| U47 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U47 |
| U48 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| | 26-00001-016 | Socket DIP 16 Pin for U48 |
| U49 | 15-20032-001 | Quad 2-Input or (74LS32) |
| U50 | 15-20086-001 | Quad 2-Input Exclusive or (74LS86) |
| U51 | 15-20086-001 | Quad 2-Input Exclusive or (74LS86) |
| U52 | 15-20153-001 | Multiplexer, Dual 4-Input (74LS153) |
| U53 | 15-20153-001 | Multiplexer, Dual 4-Input (74LS153) |
| U54 | 15-20153-001 | Multiplexer, Dual 4-Input (74LS153) |
| U55 | 15-20157-001 | Multiplexer, Quad 2-Input (74LS157) |
| U56 | 15-10008-001 | RAM 1K x 4 HMOS Static (2148) |
| | 26-00001-018 | Socket DIP 18 Pin for U56 |
| U57 | 15-10008-001 | RAM 1K x 4 HMOS Static (2148) |
| | 26-00001-018 | Socket DIP 18 Pin for U57 |
| U58 | 15-30017-001 | Buffer/Driver, HEX (7417) |
| U59 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| U60 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| U61 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| U62 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| U63 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| U64 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| U65 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| U66 | 15-10001-001 | RAM 16K x 1 Dynamic (4116) |
| U67 | 15-20032-001 | Quad 2-Input or (74LS32) |
| U68 | 15-20244-001 | Octal Buffer (74LS244) |
| U69 | 15-20245-001 | BUS Transceiver, Octal (74LS245) |
| U70 | 15-20374-001 | Latch, Octal (74LS374) |
| U71 | 15-20374-001 | Latch, Octal (74LS374) |
| U72 | 15-20374-001 | Latch, Octal (74LS374) |
| U73 | 15-20157-001 | Multiplexer Quad 2-Input (74LS157) |
| U74 | 15-20157-001 | Multiplexer Quad 2-Input (74LS157) |
| U75 | 15-20245-001 | BUS Transceiver, Octal (74LS245) |
| U76 | 15-20273-001 | Register 8 Bit (74LS273) |
| U77 | 15-20373-001 | Latch, Octal (74LS373) |
| U78 | 15-20373-001 | Latch, Octal (74LS373) |
| U79 | 15-20373-001 | Latch, Octal (74LS373) |
| U80 | 15-20373-001 | Latch, Octal (74LS373) |

| SYM | TAITO PART NO. | DESCRIPTION |
|------|----------------|------------------------------------|
| U81 | 15-20157-001 | Multiplexer Quad 2-Input (74LS157) |
| U82 | 15-00002-001 | Microprocessor 68A09E |
| | 26-00001-040 | Socket DIP 40 Pin for U82 |
| U83 | 15-20244-001 | Octal, Buffer (74LS244) |
| U84 | 15-20244-001 | Octal, Buffer (74LS244) |
| U85 | 15-10002-001 | RAM 1K x 4 CMOS Static (6514) |
| | 26-00001-018 | Socket DIP 18 Pin for U85 |
| U86 | 15-10002-001 | RAM 1K x 4 CMOS Static (6514) |
| | 26-00001-018 | Socket DIP 18 Pin for U86 |
| U87 | 15-20139-001 | Decoder Dual 1 of 4 (74LS139) |
| U88 | 15-20032-001 | Quad 2-Input or (74LS32) |
| U89 | 15-20074-001 | Flip Flop, Dual-D (74LS74) |
| U90 | 15-20004-001 | Inverter, HEX (74LS04) |
| U91 | 15-20374-001 | Latch, Octal (74LS374) |
| U92 | 15-20374-001 | Latch, Octal (74LS374) |
| U93 | 15-20374-001 | Latch, Octal (74LS374) |
| U94 | 15-20374-001 | Latch, Octal (74LS374) |
| U95 | 15-20299-001 | Shift Register 8 Bit (74LS299) |
| U96 | 15-20299-001 | Shift Register 8 Bit (74LS299) |
| U97 | 15-20244-001 | Buffer, Octal (74LS244) |
| U98 | 15-20244-001 | Buffer, Octal (74LS244) |
| U99 | 15-20138-001 | Decoder, 1 of 8 (74LS138) |
| U100 | 15-40000-001 | Quad 2-Input NOR (74C00) |
| U101 | 15-20008-001 | Quad 2-Input AND (74LS08) |
| U102 | 15-20010-001 | Triple 3-Input AND (74LS10) |
| U103 | 15-20000-001 | Quad 2-Input NAND (74LS00) |
| U104 | 15-20157-001 | Multiplexer Quad 2-Input (74LS157) |
| U105 | 15-20299-001 | Shift Register 8 Bit (74LS299) |
| U106 | 15-20299-001 | Shift Register 8 Bit (74LS299) |
| U107 | 15-20299-001 | Shift Register 8 Bit (74LS299) |
| U108 | 15-20299-001 | Shift Register 8 Bit (74LS299) |
| U109 | 15-20299-001 | Shift Register 8 Bit (74LS299) |
| U110 | 15-20299-001 | Shift Register 8 Bit (74LS299) |

DATA/SOUND PROCESSOR COMPONENT LAYOUT

FIGURE 9



TAITO
08-00002-001
MADE IN U.S.A.

DATA/SOUND PROCESSOR

FIGURE 9

| SYM | TAITO PART NO. | DESCRIPTION |
|-----|----------------|--------------------------|
| R1 | 11-00001-473 | Resistor 47K ¼W ±5% |
| R2 | 11-00001-332 | Resistor 3.3K ¼W ±5% |
| R3 | 11-00001-332 | Resistor 3.3K ¼W ±5% |
| R4 | 11-00001-332 | Resistor 3300 OHM ¼W ±5% |
| R5 | 11-00001-472 | Resistor 4.7K ¼W ±5% |
| R6 | 11-00001-103 | Resistor 4.7K ¼W ±5% |
| R7 | 11-00001-103 | Resistor 10K ¼W ±5% |
| R8 | 11-00001-332 | Resistor 3.3K OHM ¼W ±5% |
| R9 | 11-60001-502 | Pot, P.C. Mount 5K |
| R10 | 11-00001-473 | Resistor 47K ¼W ±5% |
| R11 | 11-00001-473 | Resistor 47K ¼W ±5% |
| R12 | 11-00001-332 | Resistor 3.3K ¼W ±5% |
| R13 | 11-00001-332 | Resistor 3.3K ¼W ±5% |
| R14 | 11-00001-332 | Resistor 3.3K ¼W ±5% |
| R15 | 11-00001-332 | Resistor 3.3K ¼W ±5% |
| R16 | 11-00001-332 | Resistor 3.3K ¼W ±5% |
| R17 | 11-00001-332 | Resistor 3300 OHM ¼W ±5% |
| R18 | 11-00001-124 | Resistor 120K ¼W ±5% |
| R19 | 11-00001-472 | Resistor 4.7K ¼W ±5% |
| R20 | 11-00001-221 | Resistor 220 OHM ¼W ±5% |
| R21 | 11-00001-221 | Resistor 220 OHM ¼W ±5% |
| R22 | 11-00001-332 | Resistor 3.3K ¼W ±5% |
| R24 | 11-00001-182 | Resistor 1.8K ¼W ±5% |
| R25 | 11-60001-104 | POT, P.C. Mount 100K |
| R26 | 11-00001-103 | Resistor 10K ¼W ±5% |
| R27 | 11-00001-103 | Resistor 10K ¼W ±5% |
| R28 | 11-00001-223 | Resistor 22K ¼W ±5% |
| R29 | 11-00001-562 | Resistor 5.6K ¼W ±5% |
| R30 | 11-00001-332 | Resistor 3.3K ¼W ±5% |
| R31 | 11-00001-020 | Resistor 2.2 OHM ¼W ±5% |
| R32 | 11-00001-010 | Resistor 1 OHM ½W ±5% |
| R33 | 11-00001-020 | Resistor 2.2 OHM ¼W ±5% |
| R34 | 11-00001-010 | Resistor 1 OHM ½W ±5% |
| R35 | 11-00001-102 | Resistor 1.0K OHM ¼W ±5% |
| R36 | 11-00001-332 | Resistor 3.3K ¼W ±5% |
| R37 | 11-00001-152 | Resistor 1.5K ¼W ±5% |
| R38 | 11-00001-222 | Resistor 2.2K ¼W ±5% |
| R39 | 11-00001-221 | Resistor 220 OHM ¼W ±5% |
| R40 | 11-00001-332 | Resistor 3.3K ¼W ±5% |
| R41 | 11-00001-562 | Resistor 5.6K ¼W ±5% |
| R42 | 11-00001-223 | Resistor 22K ¼W ±5% |
| R43 | 11-00001-103 | Resistor 10K ¼W ±5% |
| R44 | 11-00001-103 | Resistor 10K ¼W ±5% |
| R45 | 11-00001-103 | Resistor 10K ¼W ±5% |
| R50 | 11-00001-472 | Resistor 4.7K ¼W ±5% |
| FB1 | 17-00001-001 | Ferrite Bead |
| FB2 | 17-00001-001 | Ferrite Bead |
| FB3 | 17-00001-001 | Ferrite Bead |
| FB4 | 17-00001-001 | Ferrite Bead |

| SYM | TAITO PART NO. | DESCRIPTION |
|------|----------------|--|
| FB5 | 17-00001-001 | Ferrite Bead |
| FB8 | 17-00001-001 | Ferrite Bead |
| FB9 | 17-00001-001 | Ferrite Bead |
| FB10 | 17-00001-001 | Ferrite Bead |
| FB11 | 17-00001-001 | Ferrite Bead |
| FB13 | 17-00001-001 | Ferrite Bead |
| FB14 | 17-00001-001 | Ferrite Bead |
| FB15 | 17-00001-001 | Ferrite Bead |
| FB16 | 17-00001-001 | Ferrite Bead |
| FB17 | 17-00001-001 | Ferrite Bead |
| FB18 | 17-00001-001 | Ferrite Bead |
| FB19 | 17-00001-001 | Ferrite Bead |
| FB20 | 17-00001-001 | Ferrite Bead |
| C1 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C2 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C3 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C4 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C5 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C6 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C7 | 12-20001-107 | Capacitor Electrolytic 100uf 16V |
| C8 | 12-20001-107 | Capacitor Electrolytic 100uf 16V |
| C9 | 12-20001-107 | Capacitor Electrolytic 100uf 16V |
| C10 | 12-20001-107 | Capacitor Electrolytic 100uf 16V |
| C11 | 12-20001-107 | Capacitor Electrolytic 100uf 16V |
| C12 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C13 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C14 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C15 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C16 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C17 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C18 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C19 | 12-10003-470 | Capacitor 47pf 10% NPO Axial Lead |
| C20 | 12-20001-105 | Capacitor Electrolytic 1uf |
| C21 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C22 | 12-20001-807 | Capacitor Electrolytic 800uf, 16V |
| C23 | 12-20001-807 | Capacitor Electrolytic 800uf, 16V |
| C24 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C25 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C26 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C27 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C28 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C30 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C31 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C32 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C33 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C34 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C35 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C36 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |

DATA/SOUND PROCESSOR

FIGURE 9

| SYM | TAITO PART NO. | DESCRIPTION |
|-----|----------------|--|
| C37 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C38 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C39 | 12-10001-123 | Capacitor Ceramic .012 50V Axial Lead |
| C40 | 12-10001-183 | Capacitor Ceramic .018 50V Axial Lead |
| C41 | 12-10004-103 | Capacitor Ceramic .01uf 50V Axial Lead |
| C42 | 12-10001-332 | Capacitor Ceramic .0033uf 50V Axial Lead |
| C43 | 12-10001-153 | Capacitor Ceramic .015uf 50V Axial Lead |
| C44 | 12-10001-563 | Capacitor Ceramic .056uf 50V Axial Lead |
| C45 | 12-10003-100 | Capacitor 10pf NPO Axial Lead |
| C46 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C47 | 12-20001-105 | Capacitor Electrolytic 1uf Axial Lead |
| C48 | 12-20001-105 | Capacitor Electrolytic 1uf Axial Lead |
| C49 | 12-10001-471 | Capacitor Ceramic 470uf 50V Axial Lead |
| C50 | 12-10001-471 | Capacitor Ceramic 470pf 50V Axial Lead |
| C51 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C52 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C53 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C54 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C55 | 12-20001-105 | Capacitor Electrolytic 1uf |
| C56 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C57 | 12-20001-477 | Capacitor Electrolytic 470uf, 16V |
| C58 | 12-20001-477 | Capacitor Electrolytic 470uf, 16V |
| C59 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C60 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C61 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C62 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C63 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C64 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C65 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C66 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C67 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C68 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C69 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C70 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C71 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C72 | 12-10003-101 | Capacitor 100pf 10% NPO Axial Lead |
| C73 | 12-10003-221 | Capacitor 220pf 10% NPO Axial Lead |
| C74 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C75 | 12-20001-105 | Capacitor Electrolytic 1uf |
| C76 | 12-20001-105 | Capacitor Electrolytic 1uf |
| C77 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C78 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C79 | 12-10002-104 | Capacitor Ceramic .1uf 50V Axial Lead |
| C80 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C81 | 12-10001-471 | Capacitor Ceramic 470pf 50V 10% Axial Lead |
| C83 | 12-10003-100 | Capacitor 10pf NPO Axial Lead |
| TP1 | 59-00021-001 | Test Point |
| TP2 | 59-00021-001 | Test Point |

| SYM | TAITO PART NO. | DESCRIPTION |
|------|----------------|--|
| TP3 | 59-00021-001 | Test Point |
| TP4 | 59-00021-001 | Test Point |
| TP5 | 59-00021-001 | Test Point |
| TP6 | 59-00021-001 | Test Point |
| TP7 | 59-00021-001 | Test Point |
| TP8 | 59-00021-001 | Test Point |
| TP9 | 59-00021-001 | Test Point |
| TP10 | 59-00021-001 | Test Point |
| TP11 | 59-00021-001 | Test Point |
| RP1 | 11-50001-332 | Resistor Sip Pack 3.3K |
| RP2 | 11-50001-332 | Resistor Sip Pack 3.3K |
| RP3 | 11-50001-471 | Resistor Sip Pack 47K |
| RP4 | 11-50001-471 | Resistor Sip Pack 47K |
| RP5 | 11-50001-103 | Resistor Sip Pack 10K |
| RP6 | 11-50001-332 | Resistor Sip Pack 3.3K |
| U1 | 15-20244-001 | Octal Buffer (74LS244) |
| U2 | 15-00002-001 | Microprocessor 68A09E |
| | 26-00001-040 | Socket 40P DIP-For 68A09E |
| U3 | 15-20244-001 | Octal Buffer (74LS244) |
| U4 | 15-20244-001 | Octal Buffer (74LS244) |
| U5 | 15-00007-001 | Microprocessor 6802 |
| | 26-00001-040 | Socket 40P DIP for 6802 |
| U6 | 15-20244-001 | Octal Buffer (74LS244) |
| U7 | 15-00004-002 | Parallel I/O 6821 |
| U8 | 15-00004-002 | Parallel I/O 6821 |
| U9 | 15-20245-001 | BUS Tranciever, Octal (74LS245) |
| U10 | 15-20244-001 | Octal Buffer (74LS244) |
| U11 | 15-20245-001 | BUS Tranciever, Octal (74LS245) |
| U12 | 15-20244-001 | Octal Buffer (74LS244) |
| U13 | 15-50001-001 | Digital to Analog Converter 8 Bit (1408) |
| U14 | 15-20032-001 | Quad 2-Input or (74LS32) |
| U15 | 15-10003-001 | RAM 1K x 4 NMOS Static (2114) |
| | 26-00001-018 | Socket 18P DIP for 2114 |
| U16 | 15-10003-001 | RAM 1K x 4 NMOS Static (2114) |
| | 26-00001-018 | Socket 18P DIP for 2114 |
| U17 | 15-20138-001 | Decoder 1 of 8 (74LS138) |
| U18 | 15-50003-001 | Quad OP AMP LM324 |
| U19 | 15-60004-001 | Speech Synthesis TMS5200 |
| | 26-00001-028 | Socket 28P DIP for TMS5200 |
| U20 | 15-00004-001 | Parallel I/O 68A21 |
| U21 | 15-60002-001 | Line Driver (MC1488) |
| U22 | 15-00005-002 | Serial I/O 68A50 |
| | 26-00001-024 | Socket 24P DIP for 68A50 |
| U23 | 15-20004-001 | Inverter, HEX (74LS04) |
| U24 | 15-44066-001 | Quad Analog Multiplexer (4066) |
| U25 | 15-60001-001 | Line Receiver (MC1489) |
| U26 | 15-20161-001 | Counter 4-Bit Presettable (74LS161) |
| U27 | 15-20092-001 | Counter Divide By Twelve (74LS92) |
| U28 | 15-44066-001 | Quad Analog Multiplexer (4066) |

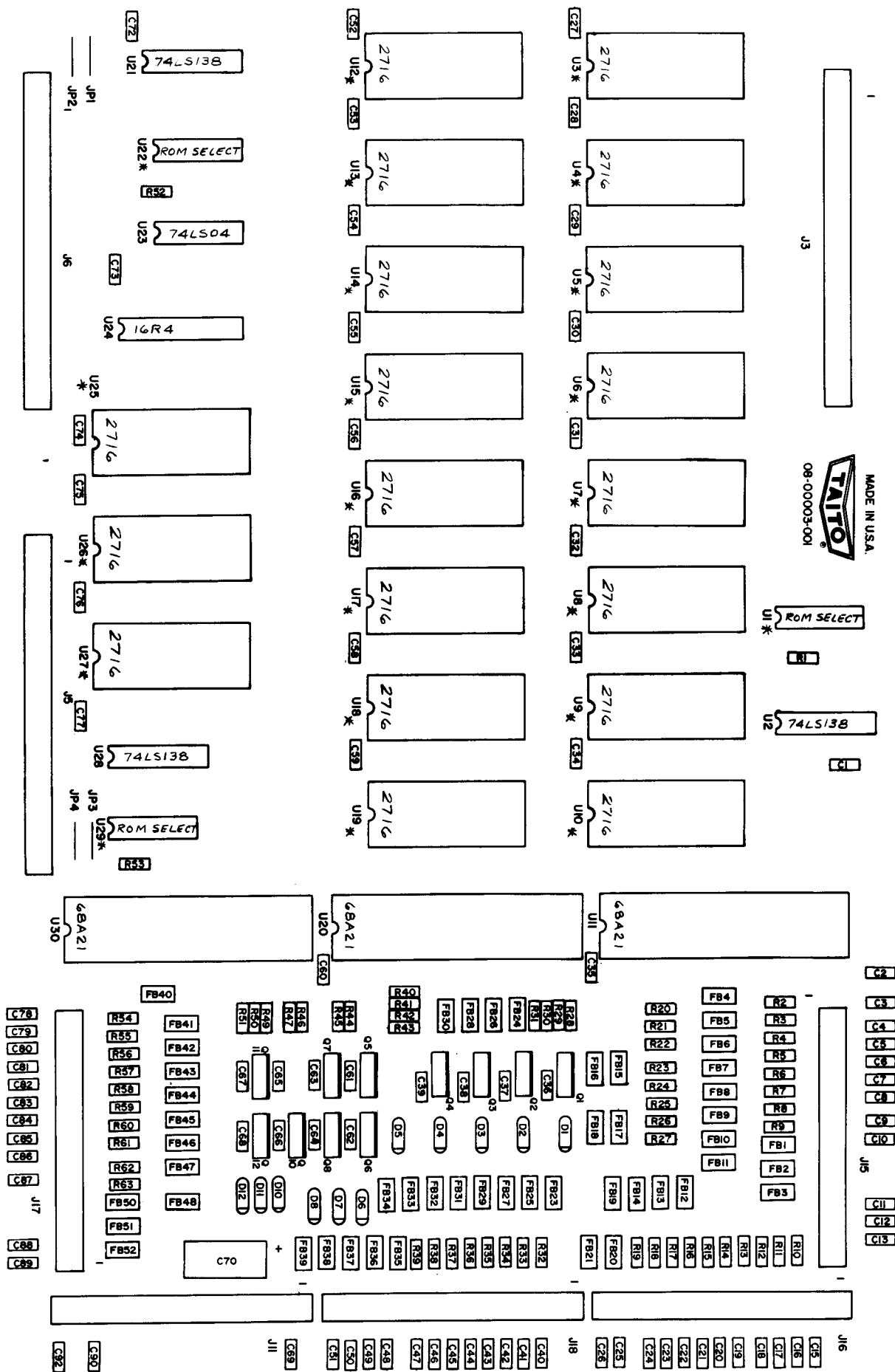
DATA/SOUND PROCESSOR

FIGURE 9

| SYM | TAITO PART NO. | DESCRIPTION |
|------------|---------------------------|-------------------------------|
| U29 | 15-50002-001 | Audio Amplifier (2002) |
| | 30-00001-001 | Heatsink to 220 |
| U30 | 15-50002-001 | Audio Amplifier (2002) |
| | 30-00001-001 | Heatsink to 220 |
| SW1 | 29-00001-001 | Switch, DIP 4 Pole |
| Y1 | 19-00002-001 | Crystal 7.3728 MHZ |
| Q1 | 14-23904-001 | Transistor NPN, Silcon 2N3904 |
| J1 | 25-00002-004 | Connector 14 PIN Locking |
| J5 | 25-00001-001 | Connector Header 50 PIN |
| J6 | 25-00001-001 | Connector Header 50 PIN |
| J7 | 25-00002-005 | Connector 5 PIN Locking |
| J8 | 25-00002-005 | Connector 5 PIN Locking |
| J9 | 25-00003-001 | Connector RS232 |

ROM/I/O P.C. ASSEMBLY COMPONENT LAYOUT

FIGURE 10



ROM/I/O P.C. ASSEMBLY

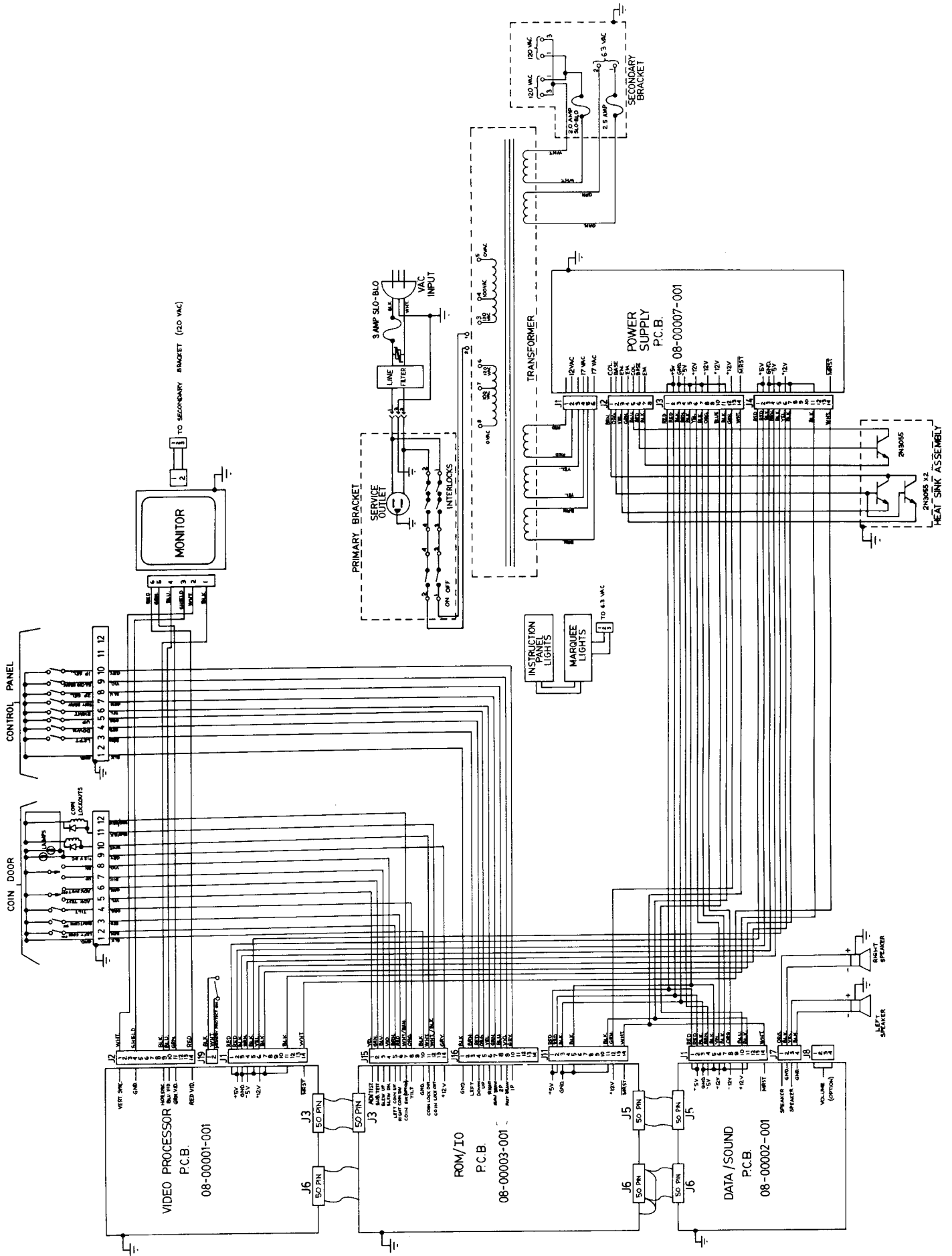
FIGURE 10

| SYM | TAITO PART NO. | DESCRIPTION |
|------|----------------|----------------------------------|
| FB42 | 17-00001-001 | Ferrite Bead |
| FB43 | 17-00001-001 | Ferrite Bead |
| FB44 | 17-00001-001 | Ferrite Bead |
| FB45 | 17-00001-001 | Ferrite Bead |
| FB46 | 17-00001-001 | Ferrite Bead |
| FB47 | 17-00001-001 | Ferrite Bead |
| FB48 | 17-00001-001 | Ferrite Bead |
| FB49 | 17-00001-001 | Ferrite Bead |
| FB50 | 17-00001-001 | Ferrite Bead |
| FB51 | 17-00001-001 | Ferrite Bead |
| FB52 | 17-00001-001 | Ferrite Bead |
| FB53 | 17-00001-001 | Ferrite Bead |
| D1 | 13-14001-001 | Diode IN4001 |
| D2 | 13-14001-001 | Diode IN4001 |
| D3 | 13-14001-001 | Diode IN4001 |
| D4 | 13-14001-001 | Diode IN4001 |
| D5 | 13-14001-001 | Diode IN4001 |
| D6 | 13-14001-001 | Diode IN4001 |
| D7 | 13-14001-001 | Diode IN4001 |
| D8 | 13-14001-001 | Diode IN4001 |
| D9 | 13-14001-001 | Diode IN4001 |
| D10 | 13-14001-001 | Diode IN4001 |
| D11 | 13-14001-001 | Diode IN4001 |
| D12 | 13-14001-001 | Diode IN4001 |
| Q1 | 14-00001-001 | Transistor NPN Darlington TIP120 |
| Q2 | 14-00001-001 | Transistor NPN Darlington TIP120 |
| Q3 | 14-00001-001 | Transistor NPN Darlington TIP120 |
| Q4 | 14-00001-001 | Transistor NPN Darlington TIP120 |
| Q5 | 14-00001-001 | Transistor NPN Darlington TIP120 |
| Q6 | 14-00001-001 | Transistor NPN Darlington TIP120 |
| Q7 | 14-00001-001 | Transistor NPN Darlington TIP120 |
| Q8 | 14-00001-001 | Transistor NPN Darlington TIP120 |
| Q9 | | Not Used |
| Q10 | 14-00001-001 | Transistor NPN Darlington TIP120 |
| Q11 | 14-00001-001 | Transistor NPN Darlington TIP120 |
| Q12 | 14-00001-001 | Transistor NPN Darlington TIP120 |
| U1 | 26-00002-016 | ROM Select |
| | 26-00001-014 | Socket 14P Dip, for U1 |
| U2 | 15-20138-001 | Decoder 1 of 8 (138) |
| U3 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U3 |
| U4 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U4 |
| U5 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U5 |

| SYM | TAITO PART NO. | DESCRIPTION |
|-----|----------------|-------------------------------------|
| U6 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U6 |
| U7 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U7 |
| U8 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U8 |
| U9 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U9 |
| U10 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U10 |
| U11 | 15-00004-001 | Paralell I/O 68A21 |
| U12 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U12 |
| U13 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U13 |
| U14 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U14 |
| U15 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24P Dip Used For E-PROM |
| U16 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U16 |
| U17 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U17 |
| U18 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U18 |
| U19 | | E-PROM "QIX"™ |
| | 26-00001-024 | Socket 24 Pin Dip for U19 |
| U20 | 15-00004-001 | Paralell I/O 68A21 |
| U21 | 15-20138-001 | Decoder 1 of 8 (138) |
| U22 | 26-00002-016 | ROM Select |
| | 26-00001-014 | Socket 24P Dip for U22 |
| U23 | 15-20004-001 | Inverter, HEX (74LS04) |
| U24 | | Not Used |
| U25 | | Not Used |
| U26 | | Not Used |
| U27 | | E-PROM "QIX"™ |
| | 26-00001-014 | Socket 14P Dip for U27 |
| U28 | 15-20138-001 | Decoder 1 of 8 (138) |
| U29 | | ROM Select |
| | 26-00001-014 | Socket 14P Dip Used For ROM Select |
| U30 | 15-00004-001 | Paralell I/O 6821 |
| J3 | 25-00001-001 | Connector Header 50PIN |
| J5 | 25-00001-001 | Connector Header 50PIN |
| J6 | 25-00001-001 | Connector Header 50PIN |
| J11 | 25-00002-014 | Connector 14 Pin Header .156 Center |
| J15 | 25-00002-014 | Connector 14 Pin Header .156 Center |
| J16 | 25-00002-014 | Connector 14 Pin Header .156 Center |
| J17 | 25-00002-014 | Connector 14 Pin Header .156 Center |

WIRING DIAGRAM

FIGURE 11





WARRANTY

TAITO AMERICA CORPORATION warrants that its printed circuit boards and parts are free from defects in material and workmanship under normal use and service for a period of ninety (90) days from the date of shipment. Seller warrants that its monitors are free from defects in material and workmanship under normal use for a period of thirty (30) days from the date of shipment. The factory also warrants all socketed parts for a period of ninety (90) days when furnished with the game serial number.

If the above products fail to conform to this Warranty Taito America Corporation has the option to repair, replace, or credit the Buyer's account.

The Buyer must notify Taito America Corporation in writing upon finding the defective product. Buyer must also return the defective product prepaid to Taito America Corporation's factory located in Elk Grove Village, Illinois.

If Taito America Corporation determines upon examining the returned product that damage was caused by accident, misuse, neglect, modification, or improper repair or testing, this Warranty will be void.

In no event will Taito America Corporation be held for loss of profits to Buyer.

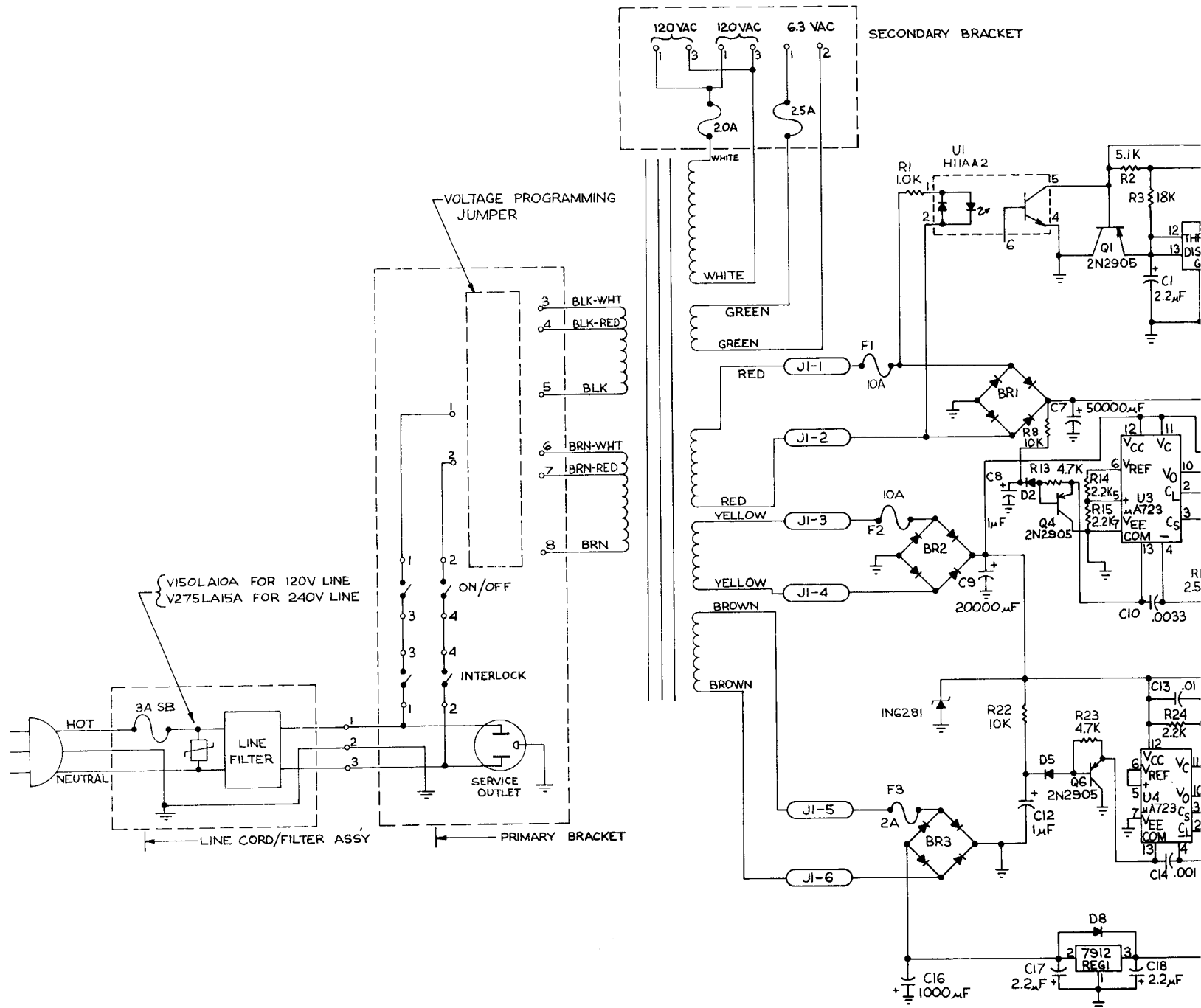


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POWER SUPPLY SCHE

FIGURE 12

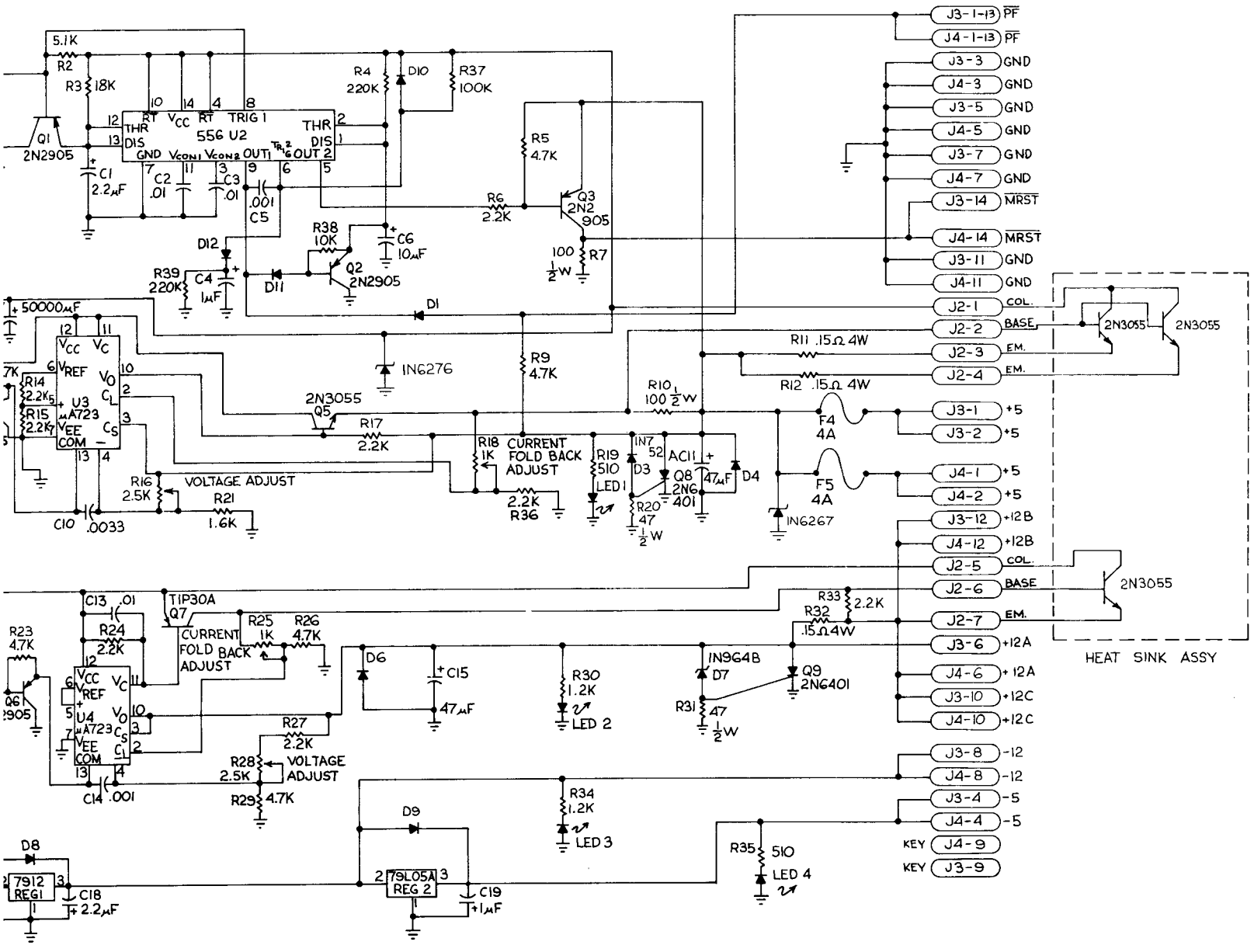


SUPPLY SCHEMATIC

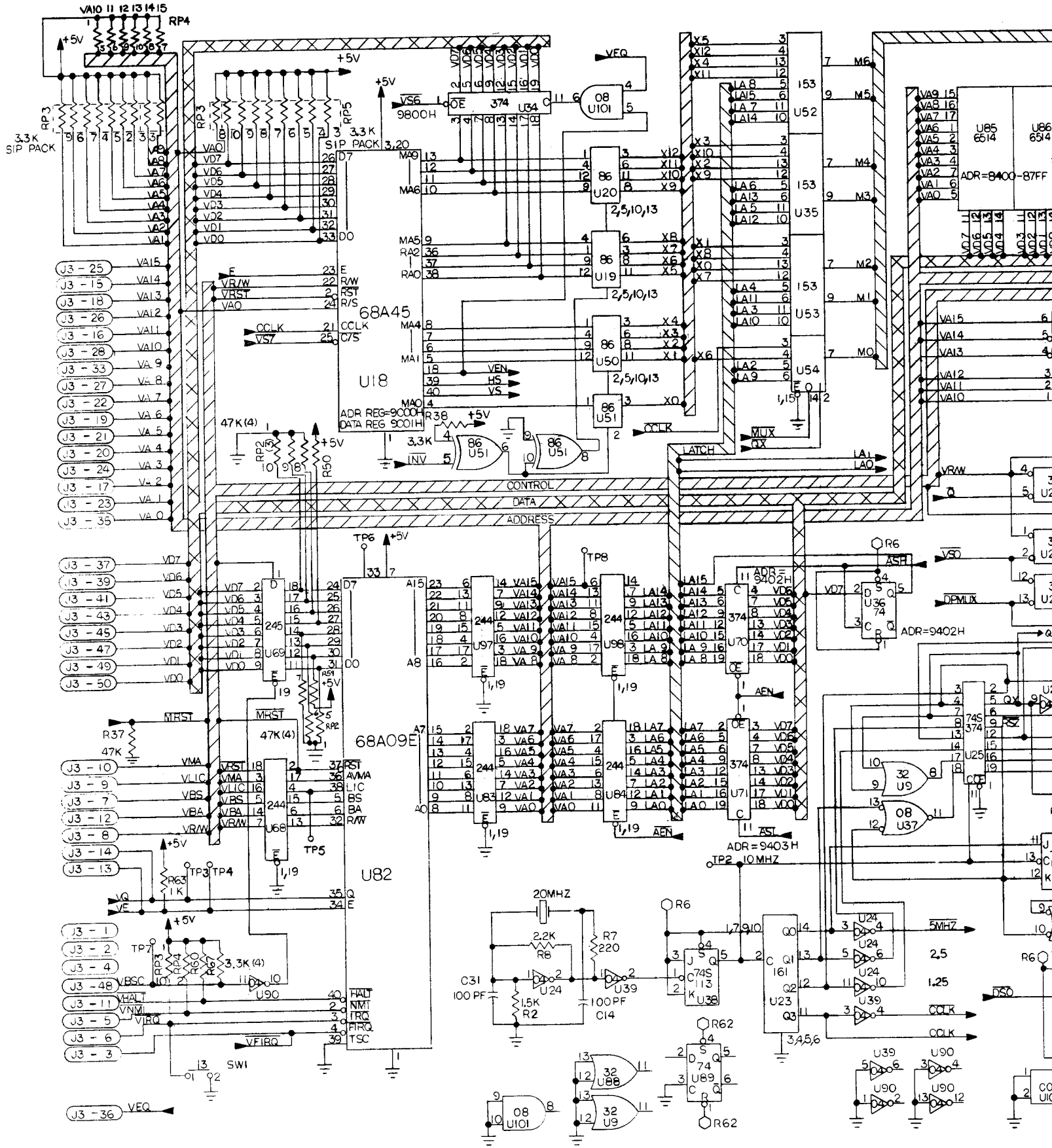
FIGURE 12

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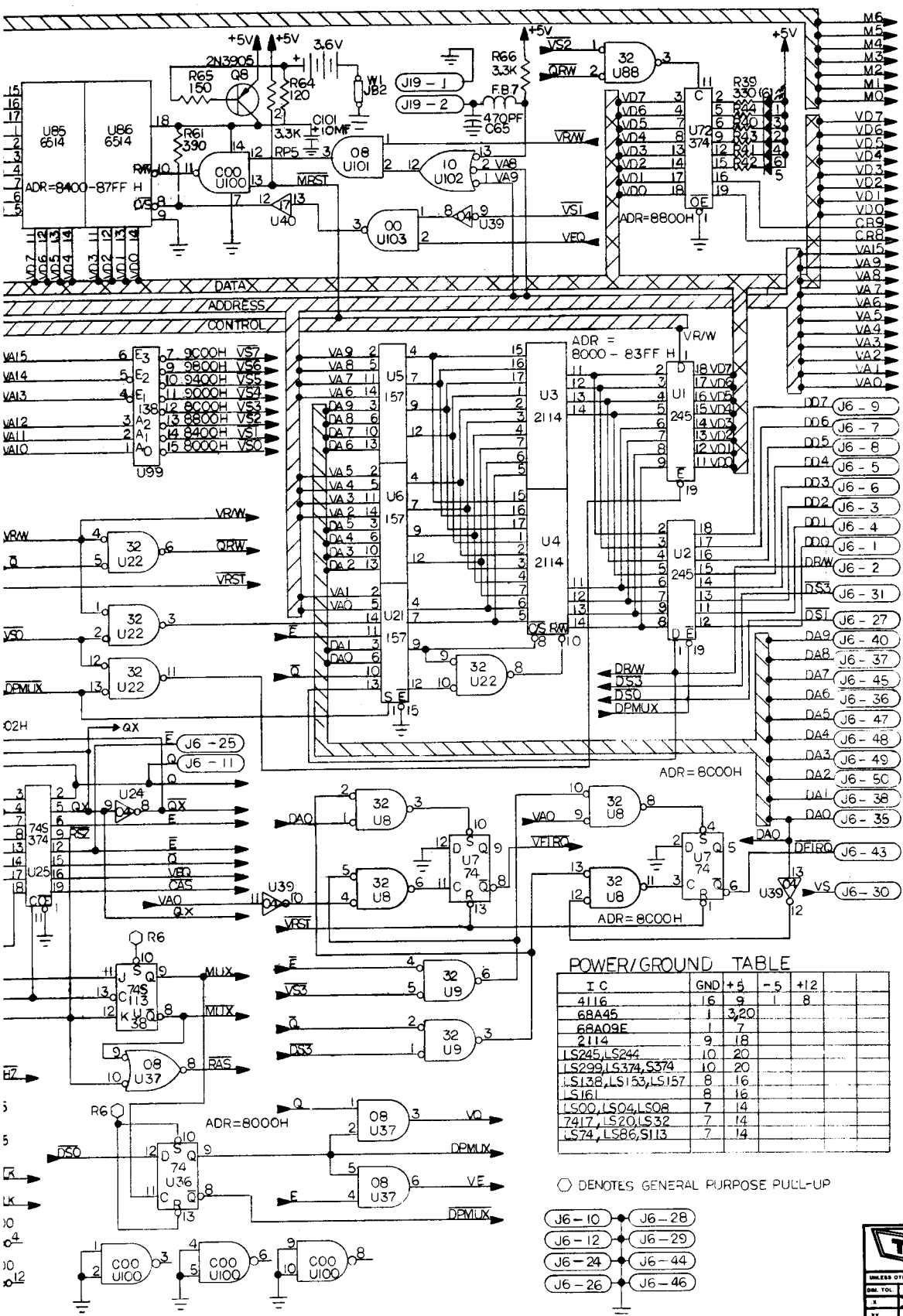


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| POWER SUPPLY ASSEMBLY | | | |
| | | USED ON | SHEET |
| | | | 1 of 1 |



SOR SCHEMATIC 1 OF 2

FIGURE 13



POWER/GROUND TABLE

| IC | GND | +5 | -5 | +12 |
|---------------------|-----|------|----|-----|
| 4116 | 16 | 9 | | 8 |
| 68A45 | 1 | 3,20 | | |
| 68A09E | | 1 | 7 | |
| 2114 | | 9 | 18 | |
| LS245, LS244 | | 10 | 20 | |
| LS299, LS374, S374 | | 10 | 20 | |
| LS138, LS153, LS157 | | 8 | 16 | |
| LS161 | | 8 | 16 | |
| LS00, LS04, LS08 | | 7 | 14 | |
| 7417, LS20, LS32 | | 7 | 14 | |
| LS74, LS86, S113 | | 7 | 14 | |

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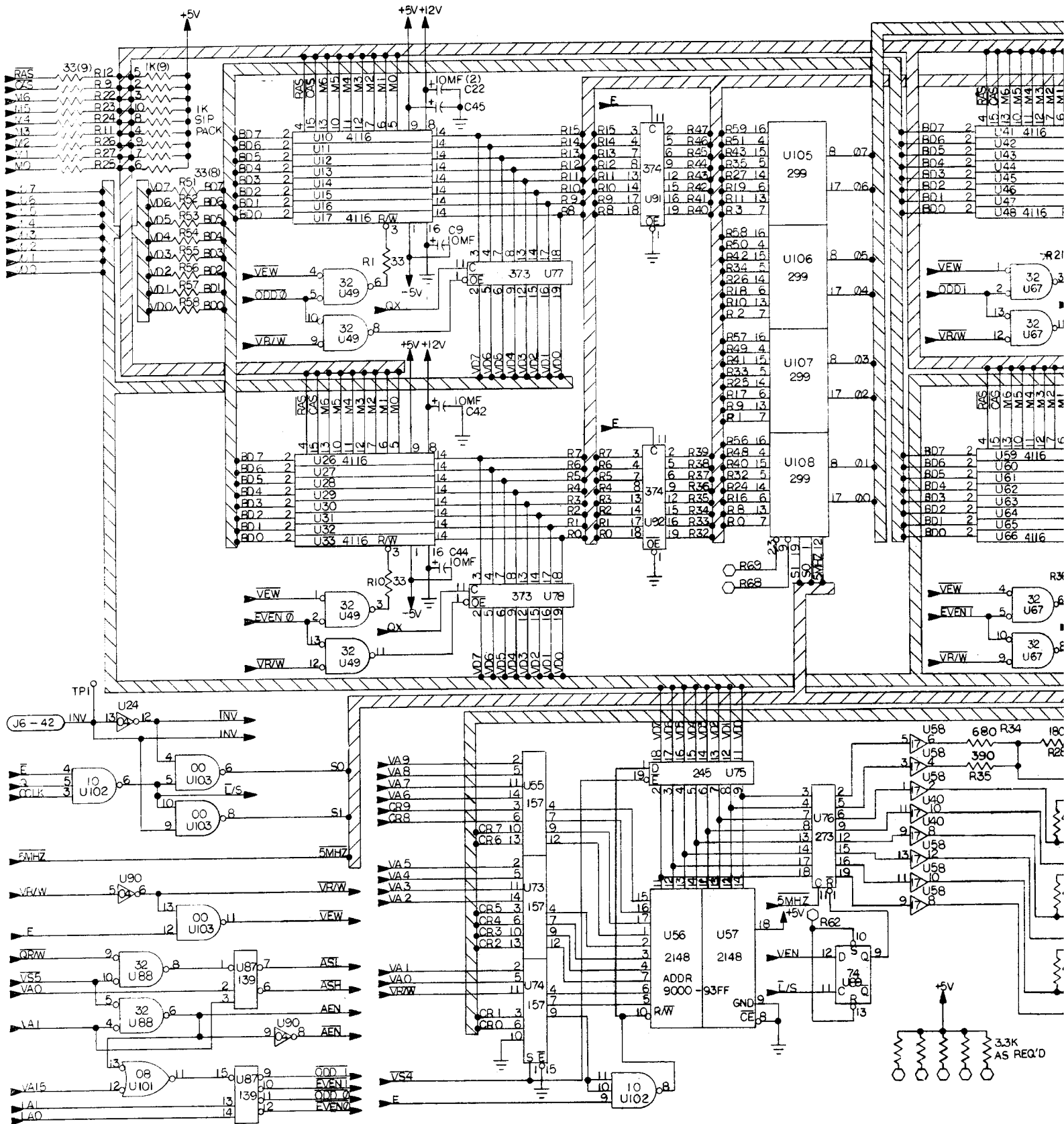
- DENOTES GENERAL PURPOSE PULL-UP
- J6-10
 - J6-12
 - J6-24
 - J6-26
 - J6-28
 - J6-29
 - J6-44
 - J6-46

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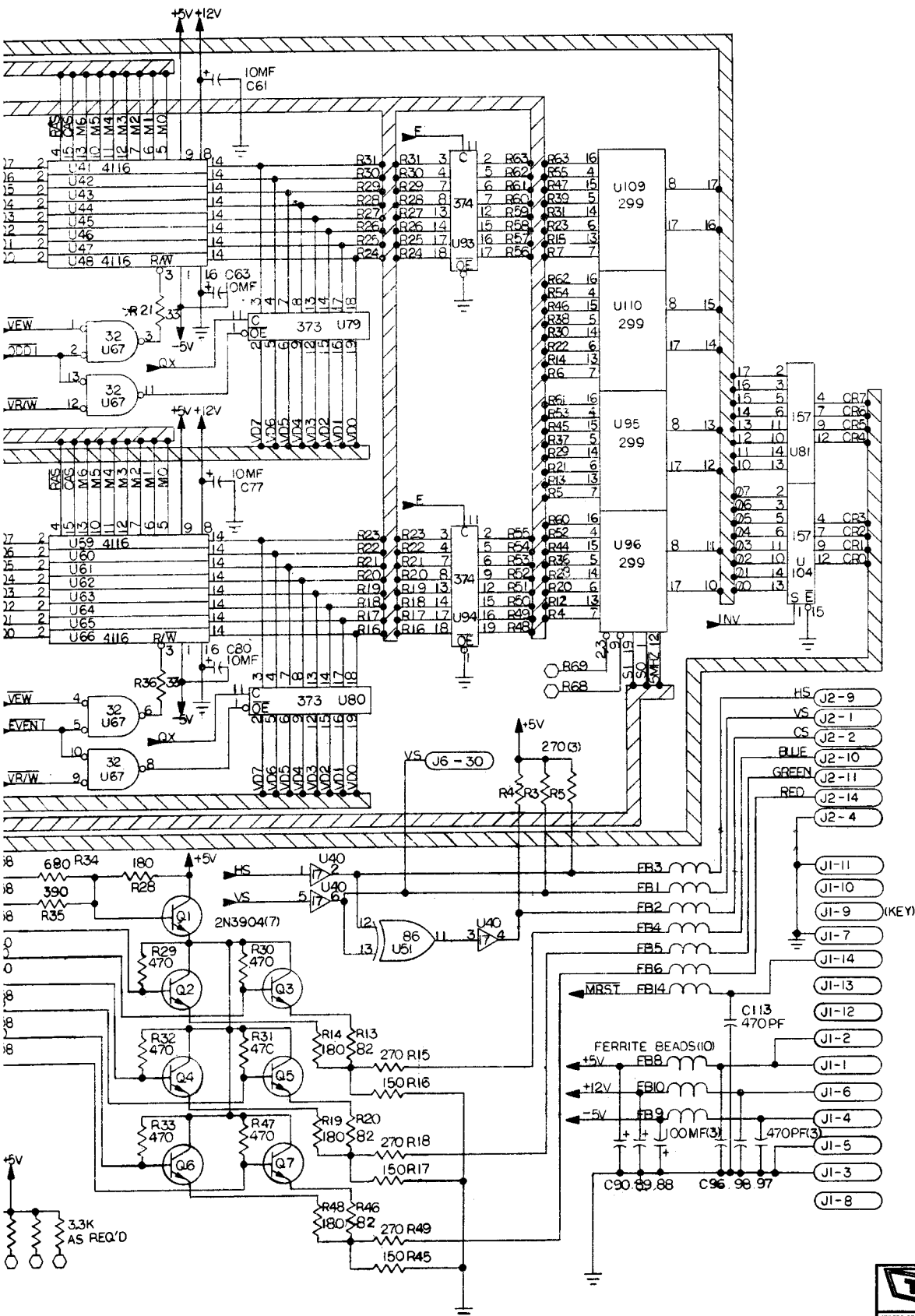
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ISOR SCHEMATIC 2 OF 2

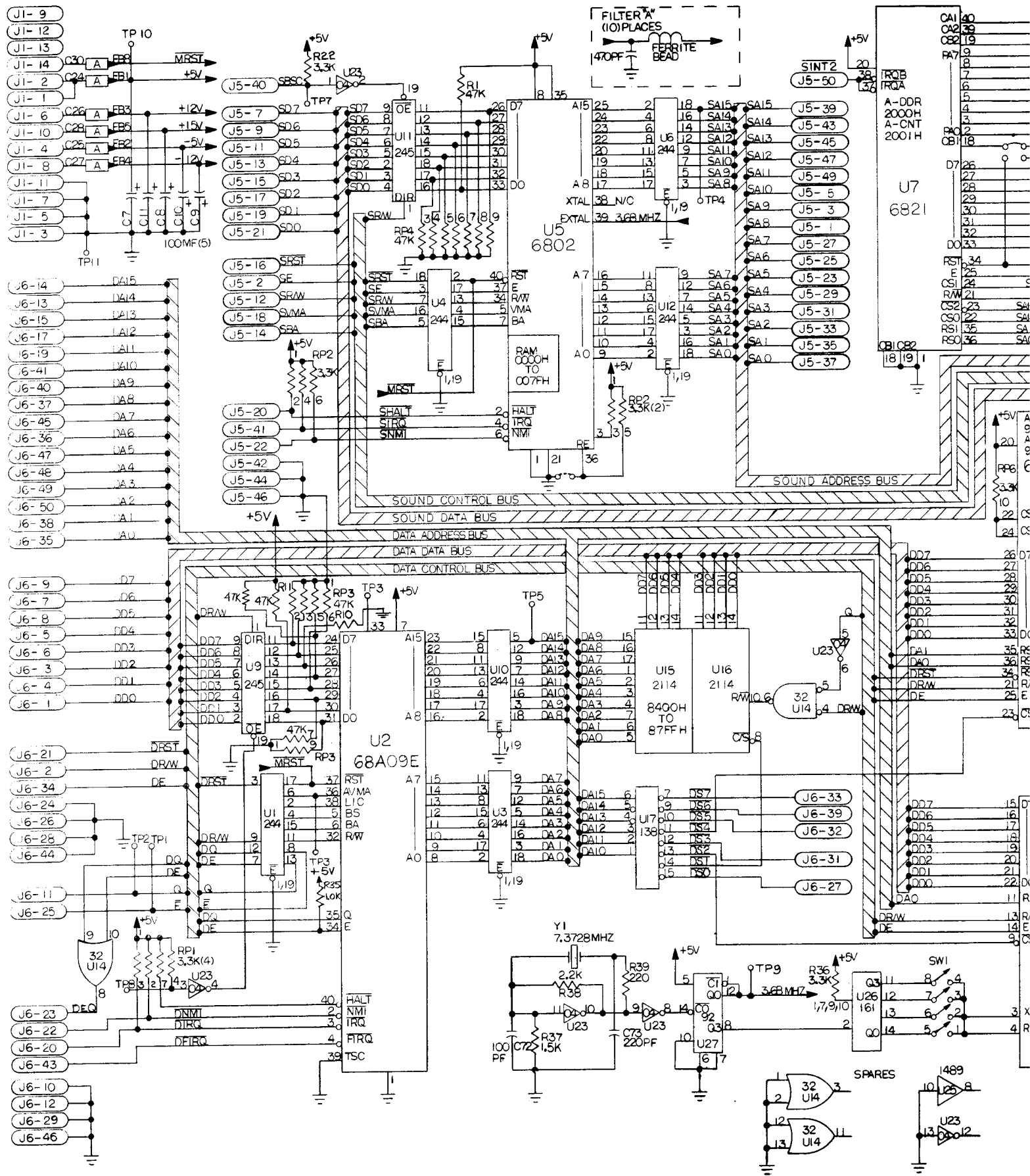
FIGURE 14



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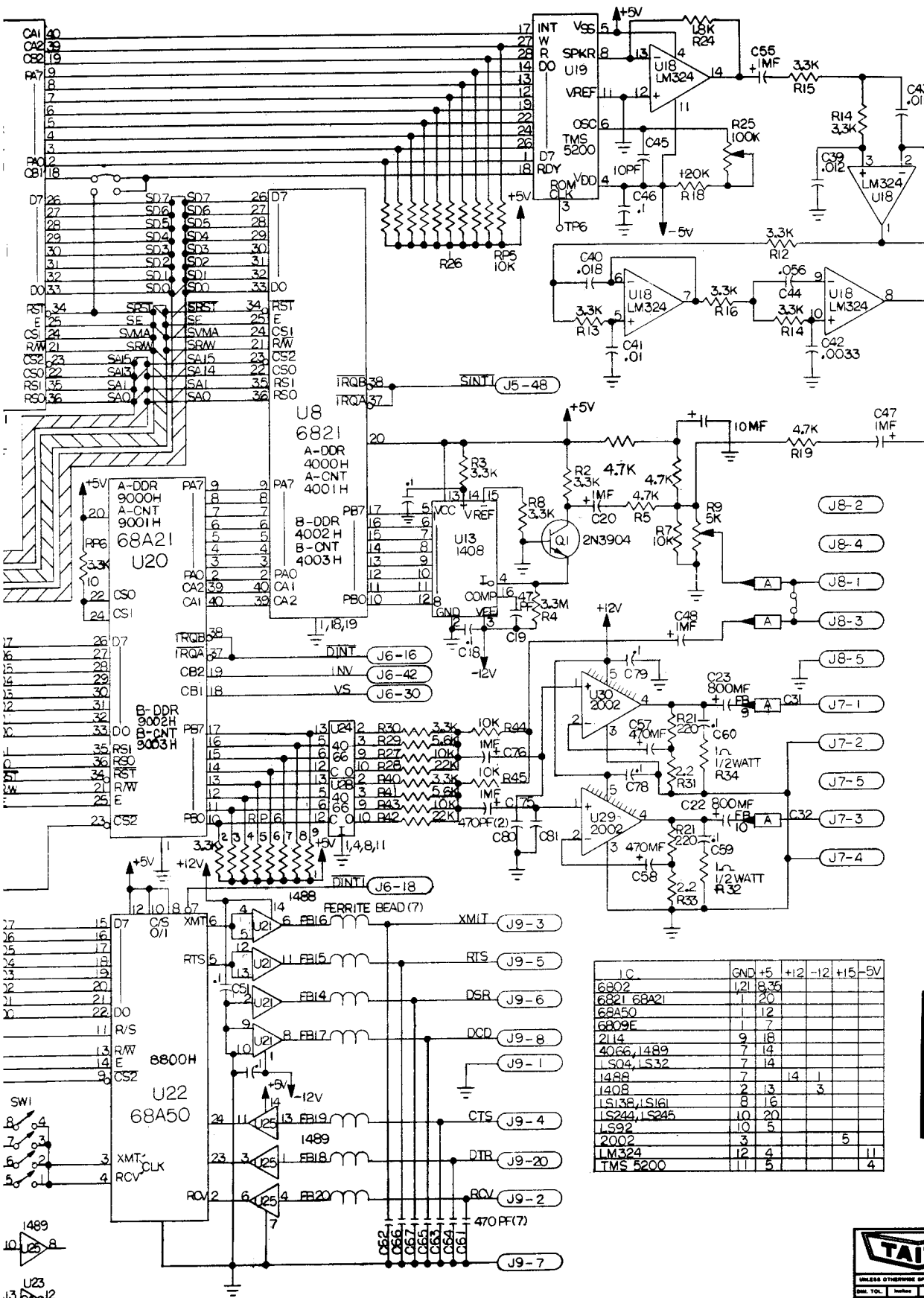
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| DRAWING NUMBER | SIZE | D | 32-00001 |



PROCESSOR SCHEMATIC

FIGURE 15



| IC | GND | +5 | +12 | -12 | +15 | -5V |
|--------------|-----|-----|-----|-----|-----|-----|
| 6802 | 12 | 18 | 35 | | | |
| 6821 68A21 | 1 | 120 | | | | |
| 68A50 | 1 | 12 | | | | |
| 6809E | 1 | 7 | | | | |
| 2114 | 9 | 18 | | | | |
| 4066, 1489 | 7 | 14 | | | | |
| LS04, LS32 | 7 | 14 | | | | |
| 1488 | 7 | 14 | 1 | | | |
| 1408 | 2 | 13 | | 3 | | |
| LS138, LS161 | 8 | 16 | | | | |
| LS244, LS245 | 10 | 20 | | | | |
| LS92 | 10 | 5 | | | | |
| 2002 | 3 | | | | 5 | |
| LM324 | 12 | 4 | | | | 11 |
| TMS 5200 | 1 | 5 | | | | 4 |

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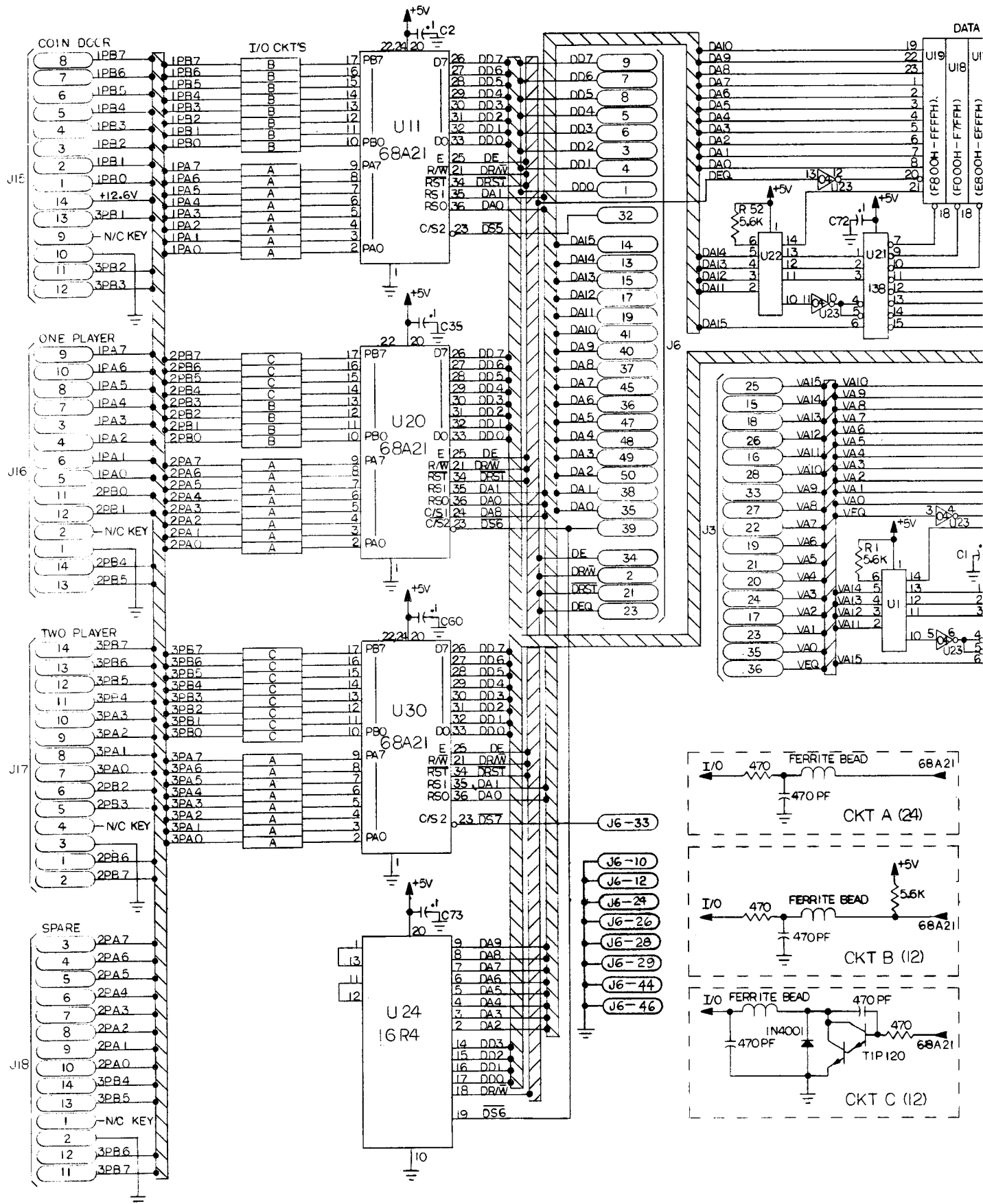
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DATE: **5/81** DRAWING NUMBER: **D 32-00002**

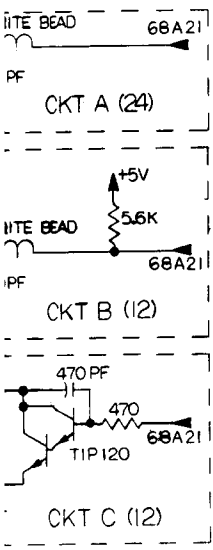
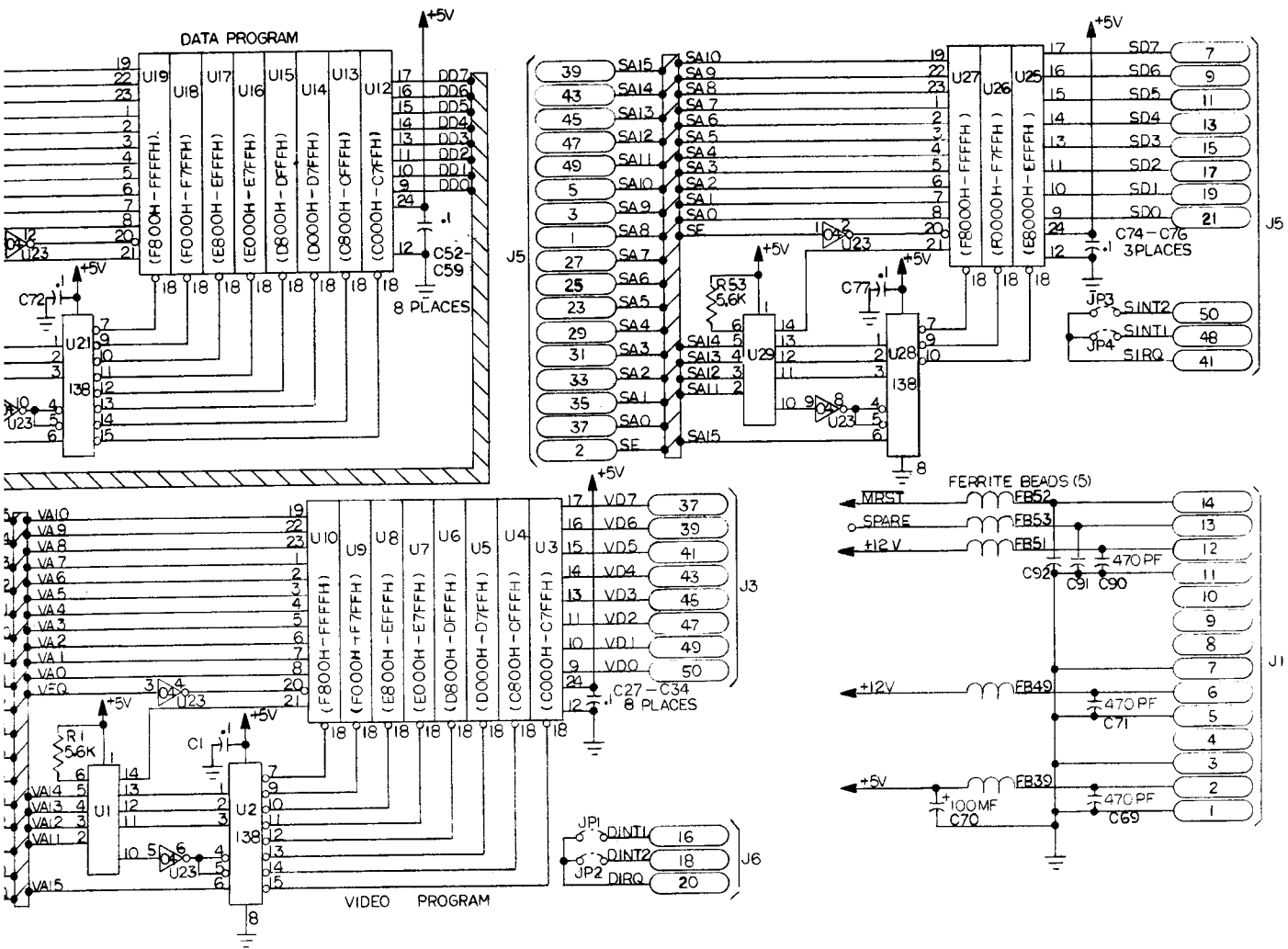
ROM I/O SCHEMATIC

FIGURE 16



I/O SCHEMATIC

FIGURE 16



| (68A21) IC NO. | 68A21 MEMORY MAP | | | |
|----------------|------------------|---------------|----------------|---------------|
| | PORT A DIR REG | CONTROL REG A | PORT B DIR REG | CONTROL REG B |
| U11 | 9400H | 9401H | 9402H | 9403H |
| U20 | 9900H | 9901H | 9902H | 9903H |
| U30 | 9C00H | 9C01H | 9C02H | 9C03H |

| POWER/GROUND TABLE | | | |
|--------------------|-----|----|-----|
| IC | GND | +5 | +12 |
| 68A21 | 1 | 20 | |
| 2716 | 12 | 24 | |
| LS138 | 8 | 16 | |
| LS04 | 7 | 14 | |

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| DATE | APPROVED BY | DATE | SCALE |
| DESCRIPTION | | | |
| ROM / IO | | | |
| DATE | USED ON | SIZE | DRAWING NUMBER |
| | | D | 32DC0003 |
| SHEET | | [or] | |

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- MANDATORY
- ON FAILURE ONLY
- FOR YOUR INFORMATION

81-16

ATTN: SERVICE MANAGERS

GAME: "QIX"

SUBJECT: LOCATION PROGRAMMING FRAME

SOLUTION: NONE

PARTS NEEDED: NONE

DISPOSITION OF OLD PARTS: NONE

PROCEDURE: OPEN THE COIN DOOR AND PULL THE BOTTOM INTERLOCK SWITCH OUT (LEAVE THE TOP INTERLOCK SWITCH ALONE). PUSH THE SELF TEST SWITCH TOWARD "ADVANCE TEST!" THE "LOCATION PROGRAMMING" FRAME SHOULD BE ON THE DISPLAY. THE FIRST LINE SHOULD BE GREEN. IN ORDER TO CHANGE A LINE'S NUMBER, YOU WILL HAVE TO PRESS THE TEST SWITCH TOWARD ADVANCE SUB TEST UNTIL THE LINE YOU WANT TO CHANGE IS GREEN. IN ORDER TO CHANGE THE NUMBER ITSELF, PRESS THE SET SWITCH (SEE FIGURE 1) TOWARD UP OR DOWN DEPENDING IF YOU WANT A HIGHER NUMBER OR A LOWER NUMBER.

THE FIRST LINE IS BACK UP HSTD [0000]. THIS LINE IS FOR THE HIGH SCORE TO DATE. WHEN YOU RESET THE HIGH SCORE TO DATE, YOU WILL SET ALL LINES TO THIS VALUE.

THE NEXT LINE IS FOR MAXIMUM CREDITS. WHEN THE NUMBER OF CREDITS GOES OVER THIS NUMBER, THE COIN LOCKOUT COILS WILL BE DE ENERGIZED SO NO MORE COINS ARE ACCEPTED.

THE NEXT LINE IS THE NUMBER OF TURNS. THIS IS THE NUMBER OF MARKERS GIVEN IN THE GAME.

THE NEXT LINE IS FOR THE TIME LINE. THE TIME LINE IS THE RED LINE ABOVE THE PLAYING FIELD. WHEN THE TIME LINE IS EXHAUSTED, 2 MORE SPARK GO ALONG THE BORDER WHEN THE TIME LINE IS EXHAUSTED AGAIN, THEY TURN BLUE AND WILL CHASE AFTER THE MARKER WHILE IT IS DRAWING. THIS LINE IS FOR HOW MANY SECONDS IT WILL TAKE TO EXHAUST THE TIME LINE.

THE NEXT 4 LINES ARE FOR DIFFICULTY FOR THE FOUR DIFFERENT FRAMES, DIFFICULTY FOR THE FIRST FRAME. THIS WILL ONLY AFFECT THE "QIX" ITSELF. FRAME 1, THE "QIX" IS MORE OR LESS AT A RANDOM PATTERN. FRAME 2, THE "QIX" WILL BE MORE AGGRESSIVE. FRAME 3, THERE IS 2 "QIX" AT A RANDOM PATTERN. FRAME 4, HAS 2 "QIX" IN AN AGGRESSIVE PATTERN. THE NUMBER AT THE END OF EACH DIFFICULTY LINE SHOULD BE BETWEEN 0 AND 3. THE HIGHER THE NUMBER, THE MORE AGGRESSIVE THE "QIX" BECOMES (THE MORE THE "QIX" WILL LOOK AT WHERE THE MARKER IS AT IN THE PLAYFIELD).

THE NEXT LINE IS FOR ATTRACT SOUND. IF THIS LINE IS SET TO 0 THERE WILL BE NO SOUND DURING THE ATTRACT MODE.

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ON SOME GAMES YOU WILL HAVE ANOTHER LINE, IT WOULD SAY TABLE MODE. FOR AN UPRIGHT IT WOULD BE SET TO 0, AND FOR THE COCKTAIL TABLE IT WOULD BE SET AT 1.

THE BOTTOM LINE IS TO BE ABLE TO RESET THIS FRAME TO FACTORY SETTINGS.

THIS "LOCATION PROGRAMMING" FRAME IS VERY GOOD FOR TOURNAMENTS AFTER THE TOURNAMENT YOU CAN USE THE FACTORY RESET FOR YOUR NORMAL PLAY OR HOWEVER YOU WANT TO PUT THE SETTINGS.

Advance Test/Sub-Test
Test Switches

Up/Down Set Switch

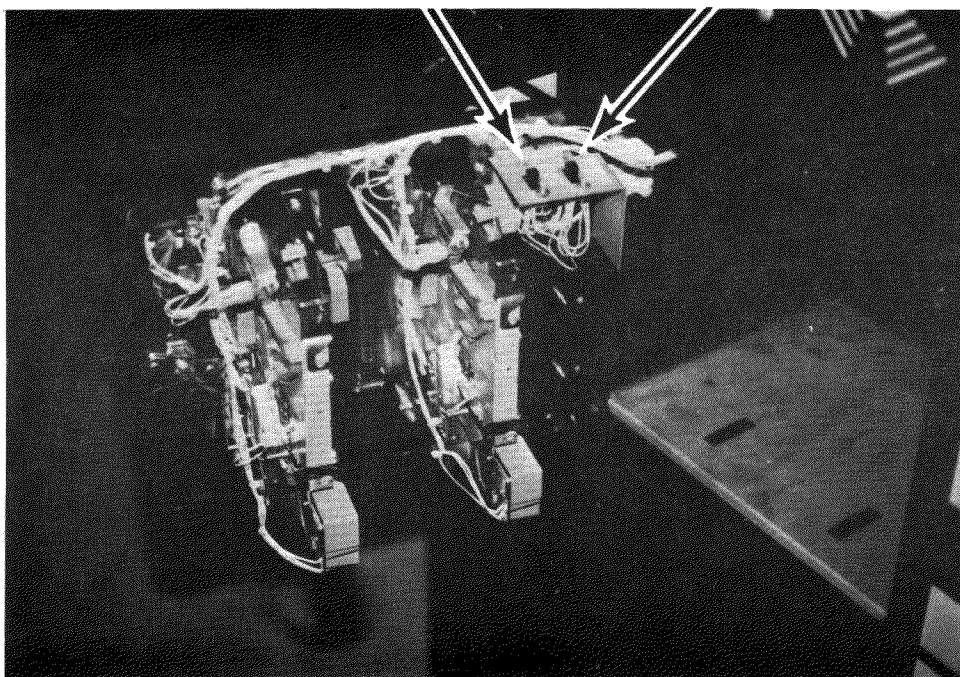


FIGURE 1