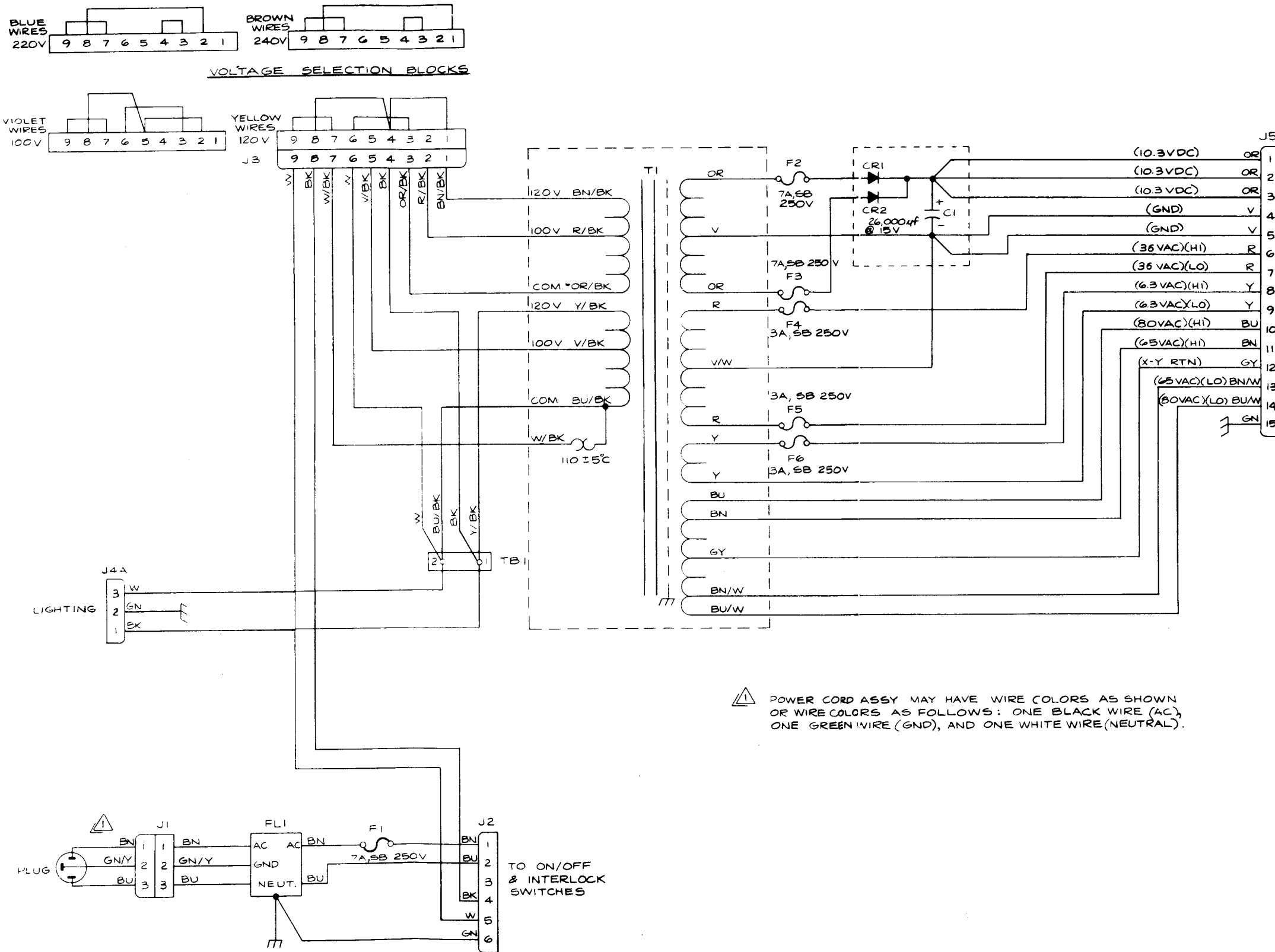


VIDEO POWER SUPPLY WIRING DIAGRAM (034633-01 A)



REGULATOR/AUDIO PCB SCHEMATIC

Regulator/Audio PCB 034485-01 A

The Regulator/Audio PCB has the dual function of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage regulator Q1, source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through feedback inputs +SENSE and -SENSE. The input is taken directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage to the game PCB. This eliminates a reduced voltage due to voltage buildup on the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the voltage on the game PCB. Once adjusted, the voltage at the game PCB will remain constant at this voltage.

Regulator Adjustment

1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND test point of Regulator/Audio PCB and plus lead to +5 V GND test point of game PCB. Note the voltage difference. If greater than +5.5 VDC, if greater, try cleaning the connectors on both the game PCB and the Regulator/Audio PCB.
4. If cleaning PCB edge connectors doesn't drop the voltage difference, connect minus lead of voltmeter to +5 V REG test point on Regulator/Audio PCB and plus lead to +5 V GND test point of game PCB. From this you can see if the harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

Audio Circuit

The audio circuit contains two independent audio amplifiers. Each amplifier consists of a TDA1584 amplifier with a gain of ten. In Asteroids, the audio circuit is permanently on. Therefore, this audio circuit is always on, even when the game is in the attract mode.

The audio circuit is repeated on Sheet 2, Side B, for more information about its operation.

Drawing Package Supplement

to

ASTEROIDS

Operation, Maintenance, and Service Manual

Contents of this Drawing Package

Game Wiring Diagram, Coin Door and Power Supply
Microprocessor
Video Generator
Switch Inputs, Coin Counter, LED and Audio Outputs

Sheet 1, Side A
Sheet 1, Side B
Sheet 2, Side A
Sheet 2, Side B

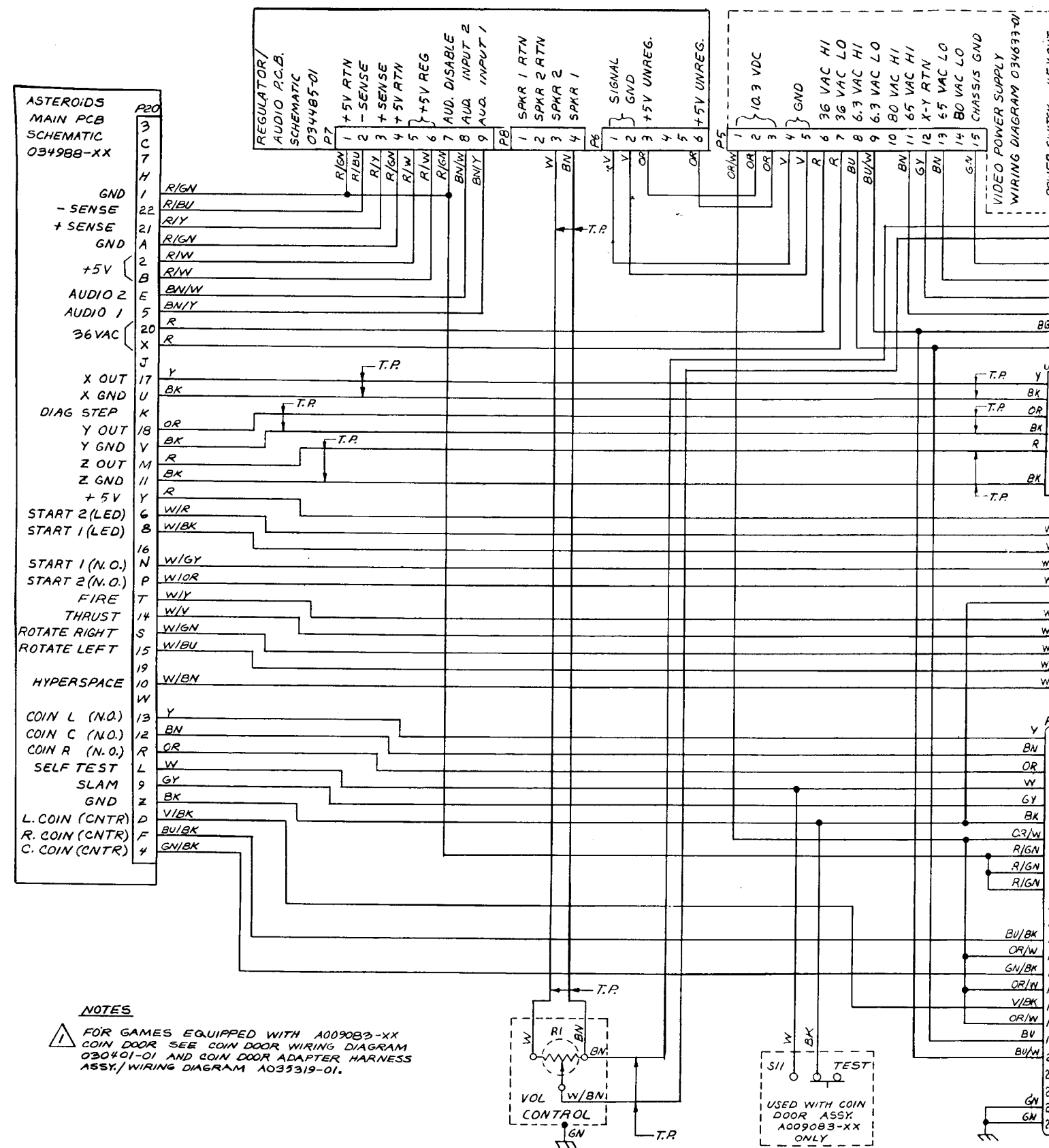
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ASTEROIDS WIRING DIAGRAM (035156-01 B)



SCHEMATIC (034485-01 D)

functions of
the PCB and

Q1, current
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D test points

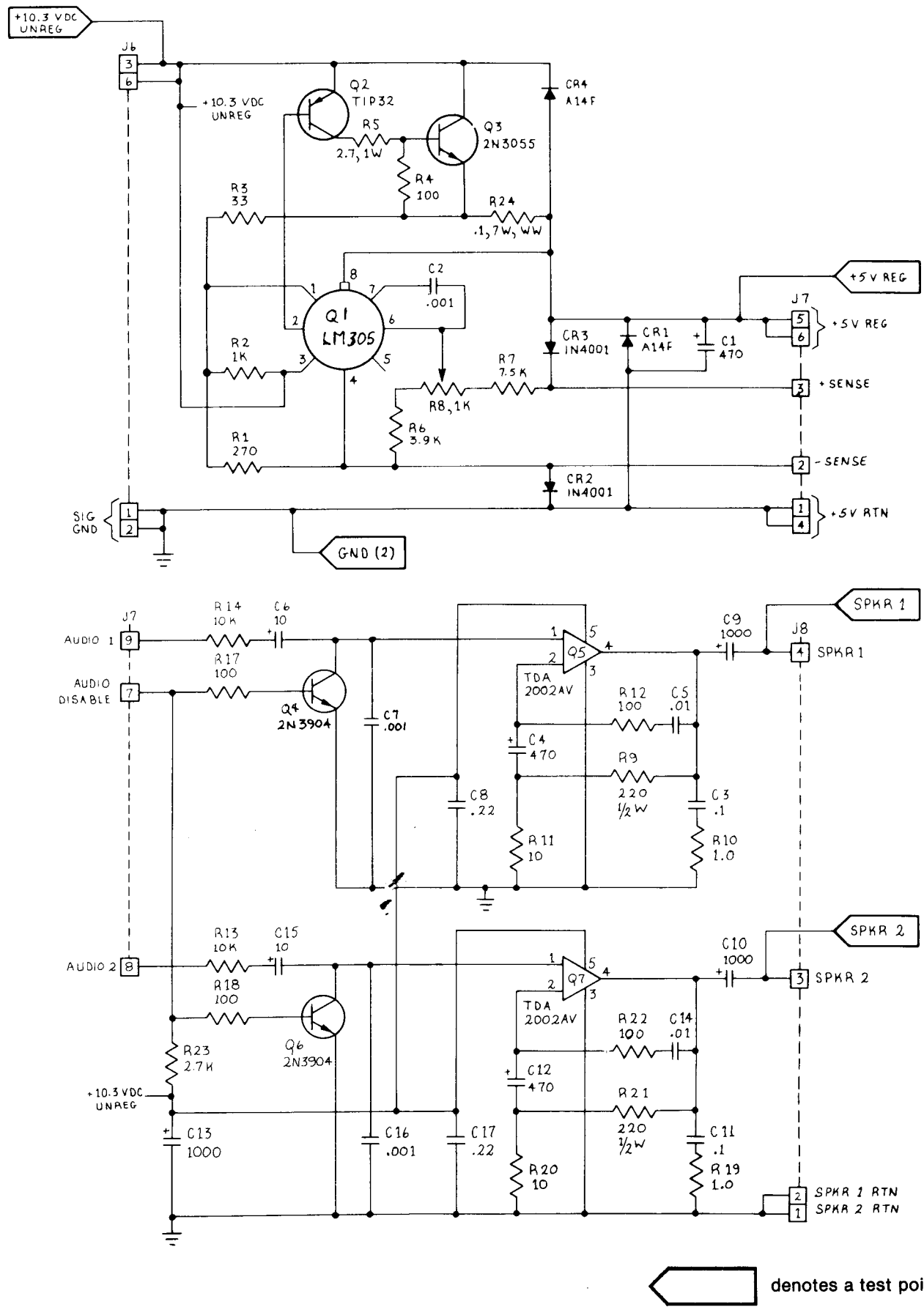
/Audio PCB

and GND on
shall not be
eaning edge
3 and the

't decrease
voltmeter to
plus lead to
voltage. Now
G test point
+5 V test
see which
troubleshoot
connector.

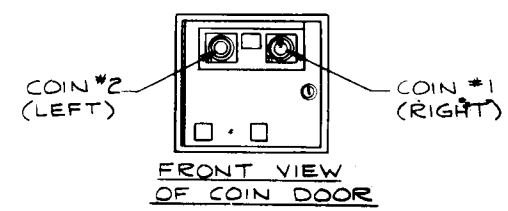
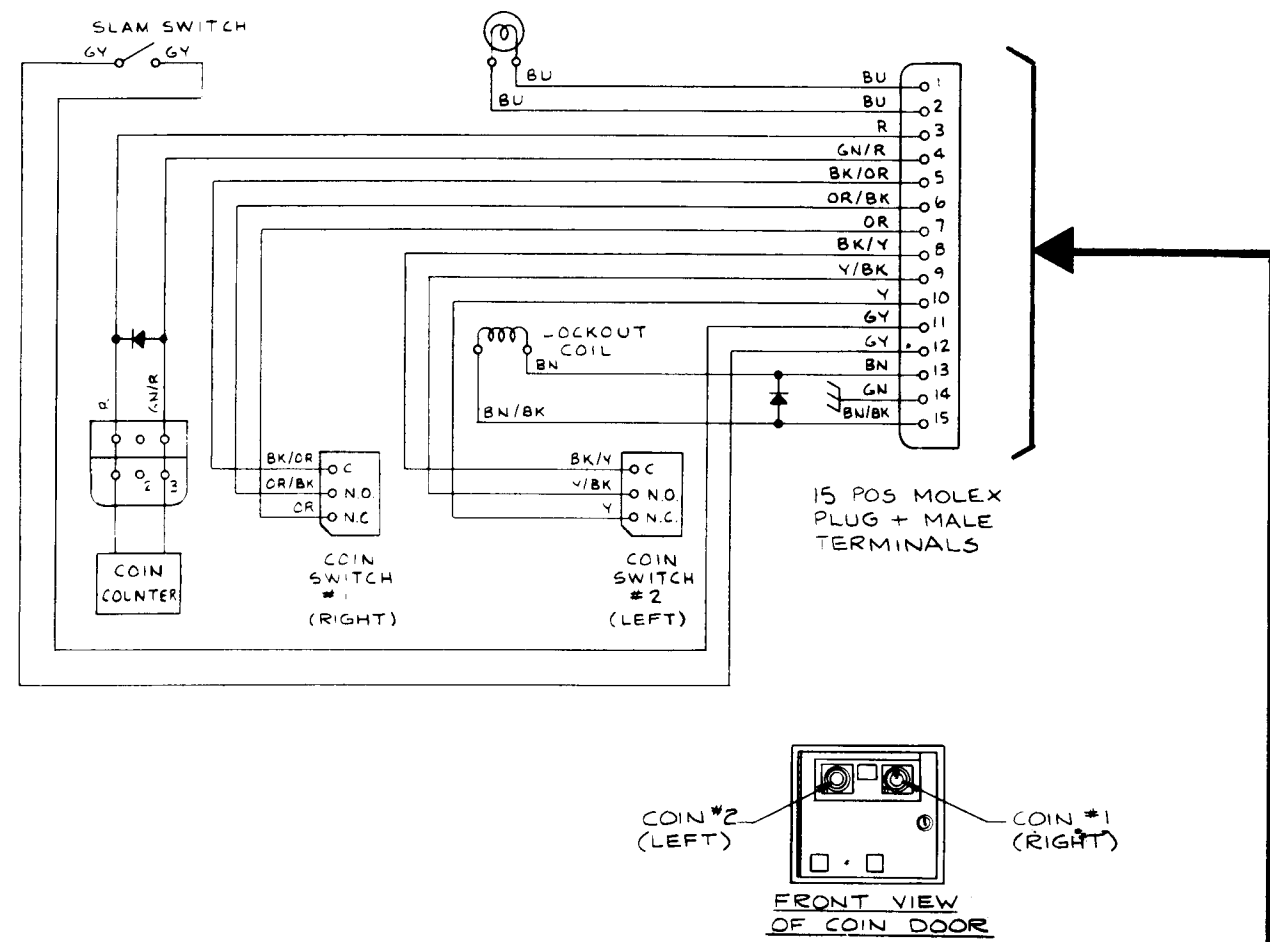
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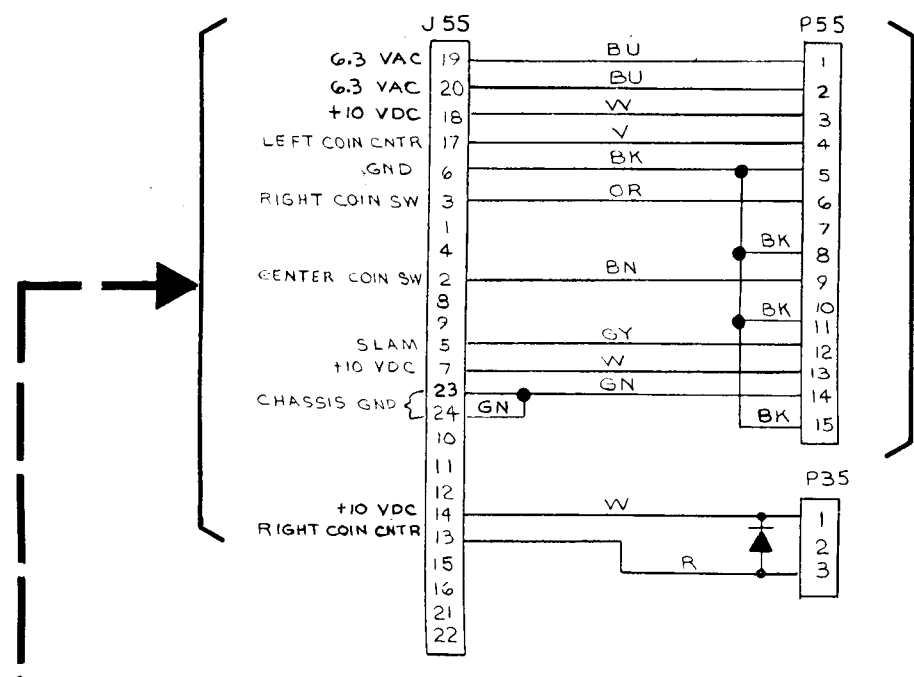


denotes a test point

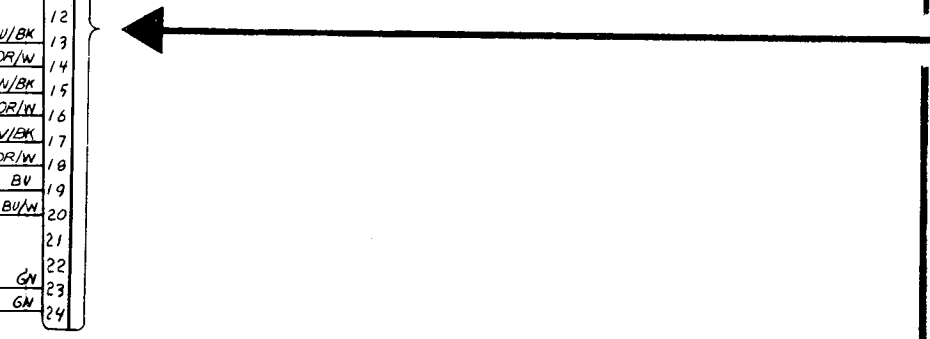
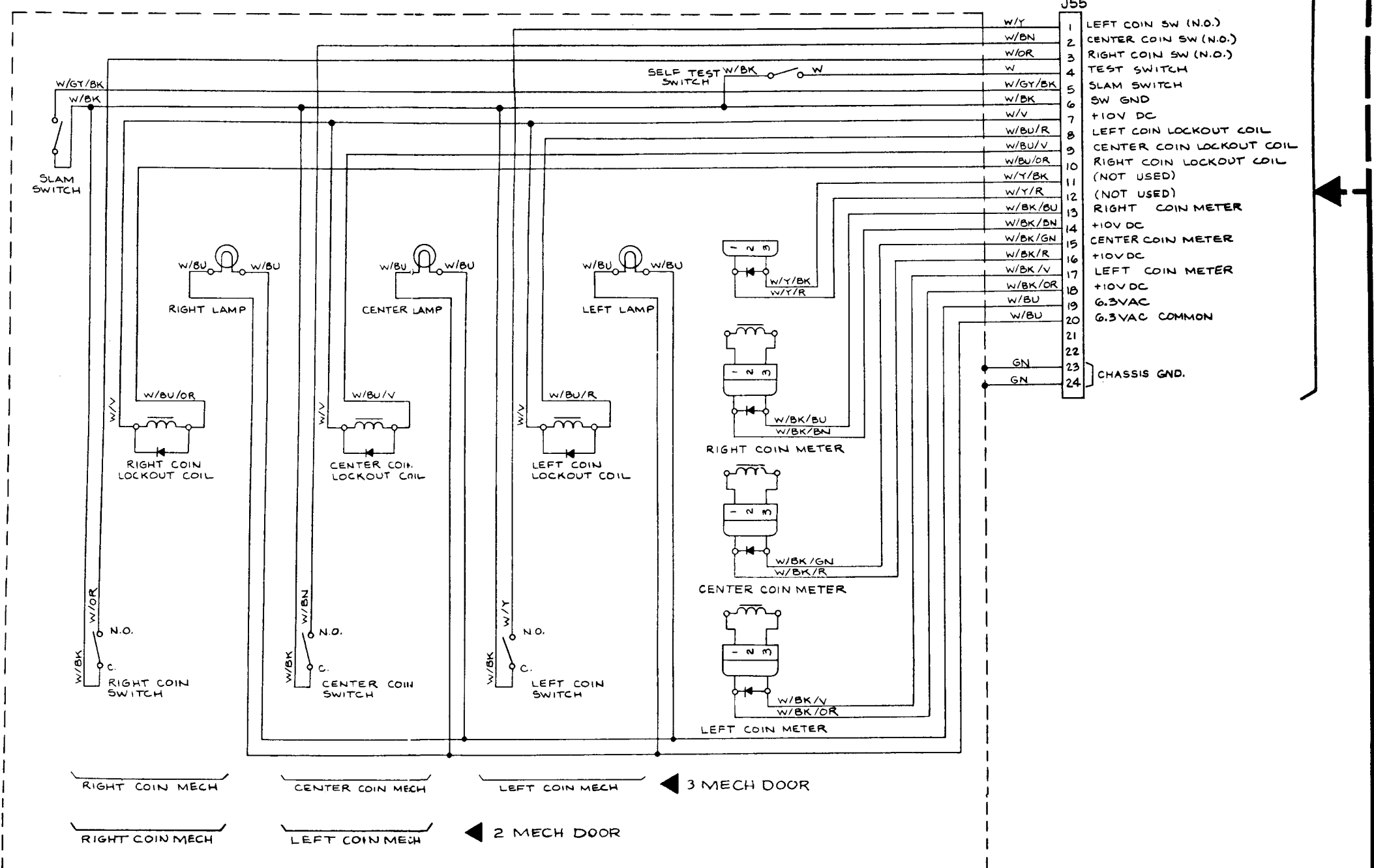
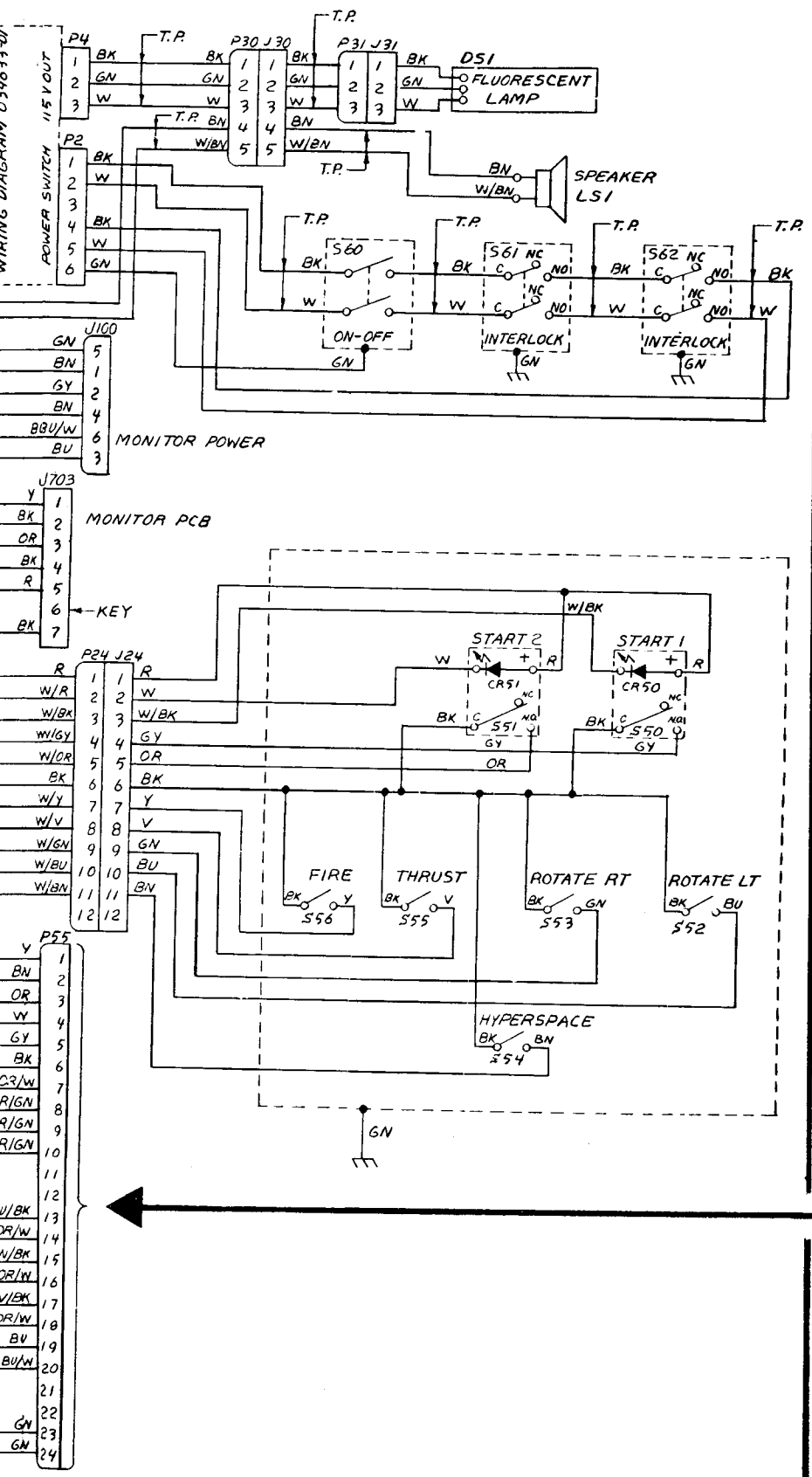
COIN DOOR SCHEMATIC (030401-01 B)



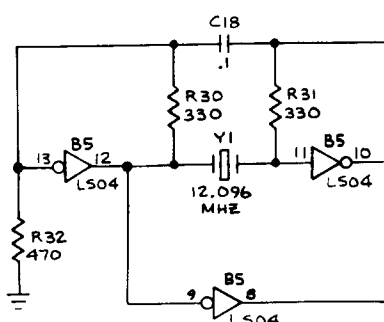
COIN DOOR ADAPTER HARNESS



COIN DOOR SCHEMATIC (034988-01 A)

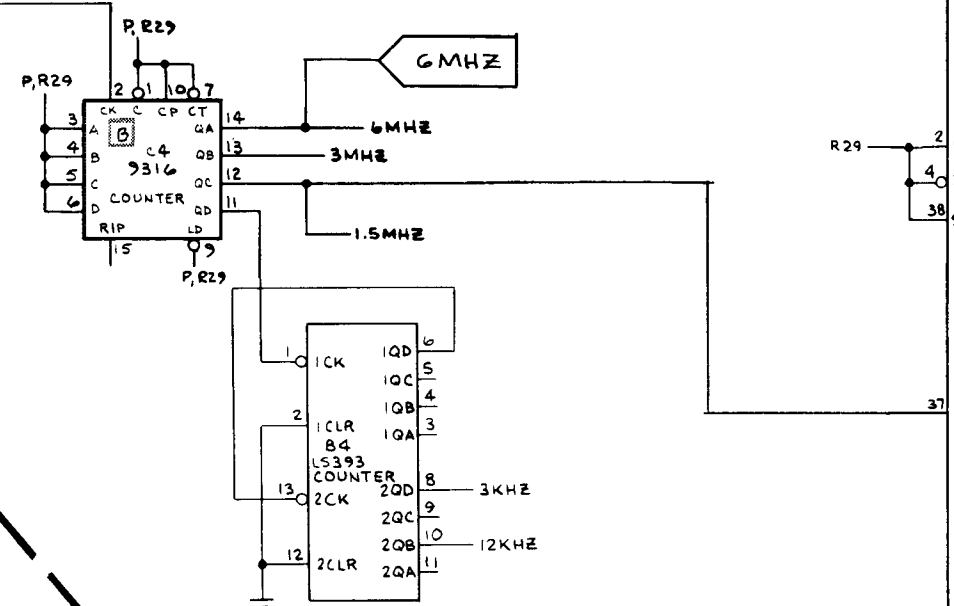


CLOCK CIRCUIT

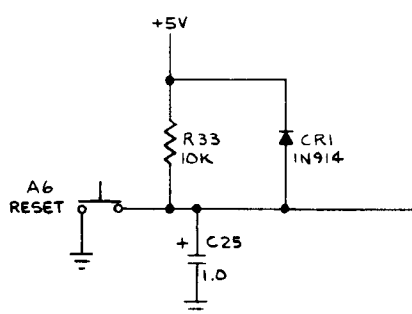


NOTE:
THE MPU IN THIS GAME OPERATES AT A FREQUENCY OF 1.5 MHZ. THEREFORE THE MPU CHIP MUST BE 6502A. THE 6502'S MAXIMUM FREQUENCY IS 1 MHZ AND IS NOT COMPATIBLE WITH THIS GAME.

The clock circuit consists of crystal Y1 and associated inverters and counters C4 and B4. Counters C4 and B4 count the crystal frequency down to the frequencies necessary for the Asteroids game.



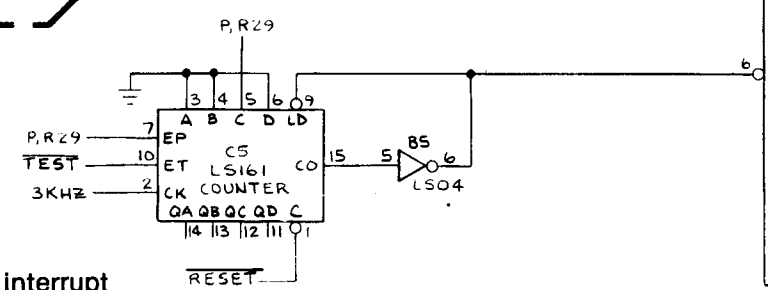
POWER RESET AND WATCHDOG COUNTER



During initial power-up, the delayed charging of capacitor C25 causes a preset of flip-flop D4 and a clear of counter D5. This results in holding RESET input to the MPU low. When the charge of C25 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D5 counts to 128 at 3 KHz rate and RESET is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

If the MPU program is operating properly, the MPU address decoding circuitry will output the WDCLR (Watchdog clear) signal at predetermined intervals. This serves to clear counter D5 before it counts up to the state that will create the RESET condition. If the MPU program strays from its intended sequence and does not output the WDCLR signal, counter D5 will count up to the RESET state and cause the MPU to return to its initialization routine.

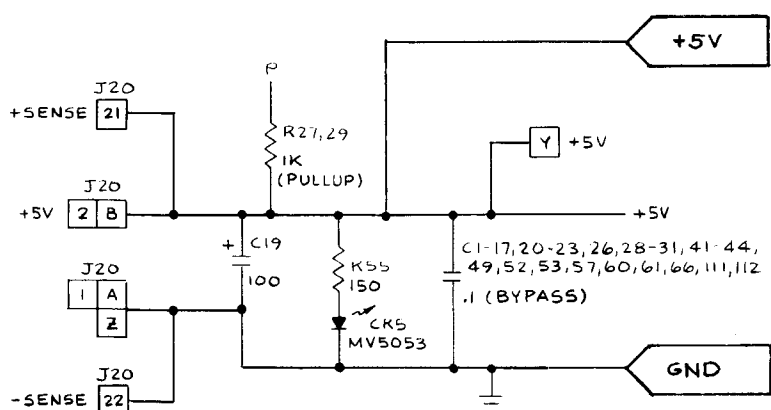
NMI COUNTER



The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter C5. The interrupt occurs when pin 6 of inverter B5 goes low. During power-up, the NMI counter is disabled by RESET. During Self-Test, the NMI is disabled by TEST.

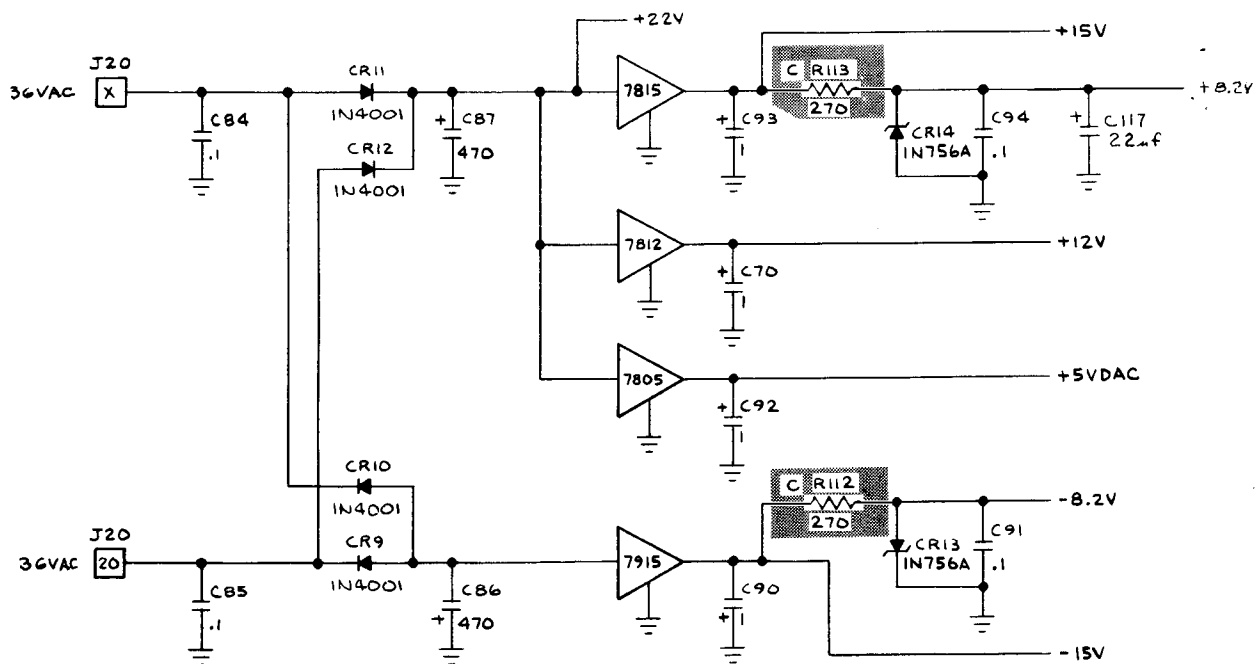
□ denotes change by indicated revision
◁ denotes a test point

POWER INPUT



This circuitry consists of the PCB inputs and outputs for the +5 VDC logic power and outputs for 36 VAC input to the on board regulators. The +5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.

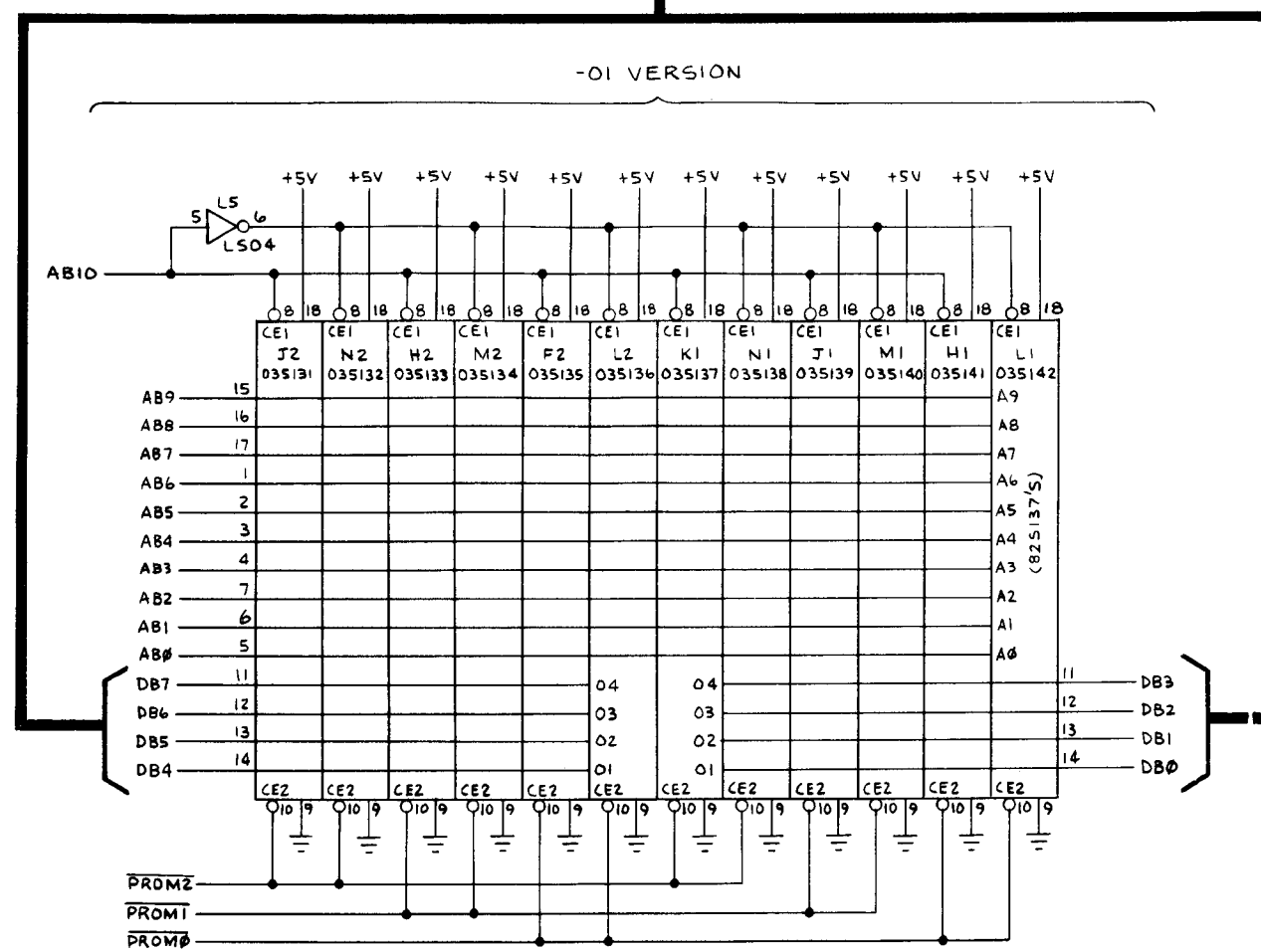
The 36 VAC inputs are received by two full wave rectifiers. Diodes CR9 and CR10 rectify the negative cycle of the input and the 7915 regulates the voltage at -15 VDC. Diodes CR11 and CR12 rectify the positive pulse of the 36 VAC input and the 7815 regulates the voltage at +15 VDC. The 7812 regulates at +12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR14 supplies the +8.2 VDC for the sample and hold circuit. The +22V (unregulated) is used to power operational amplifiers P11 and L8 in the audio output.



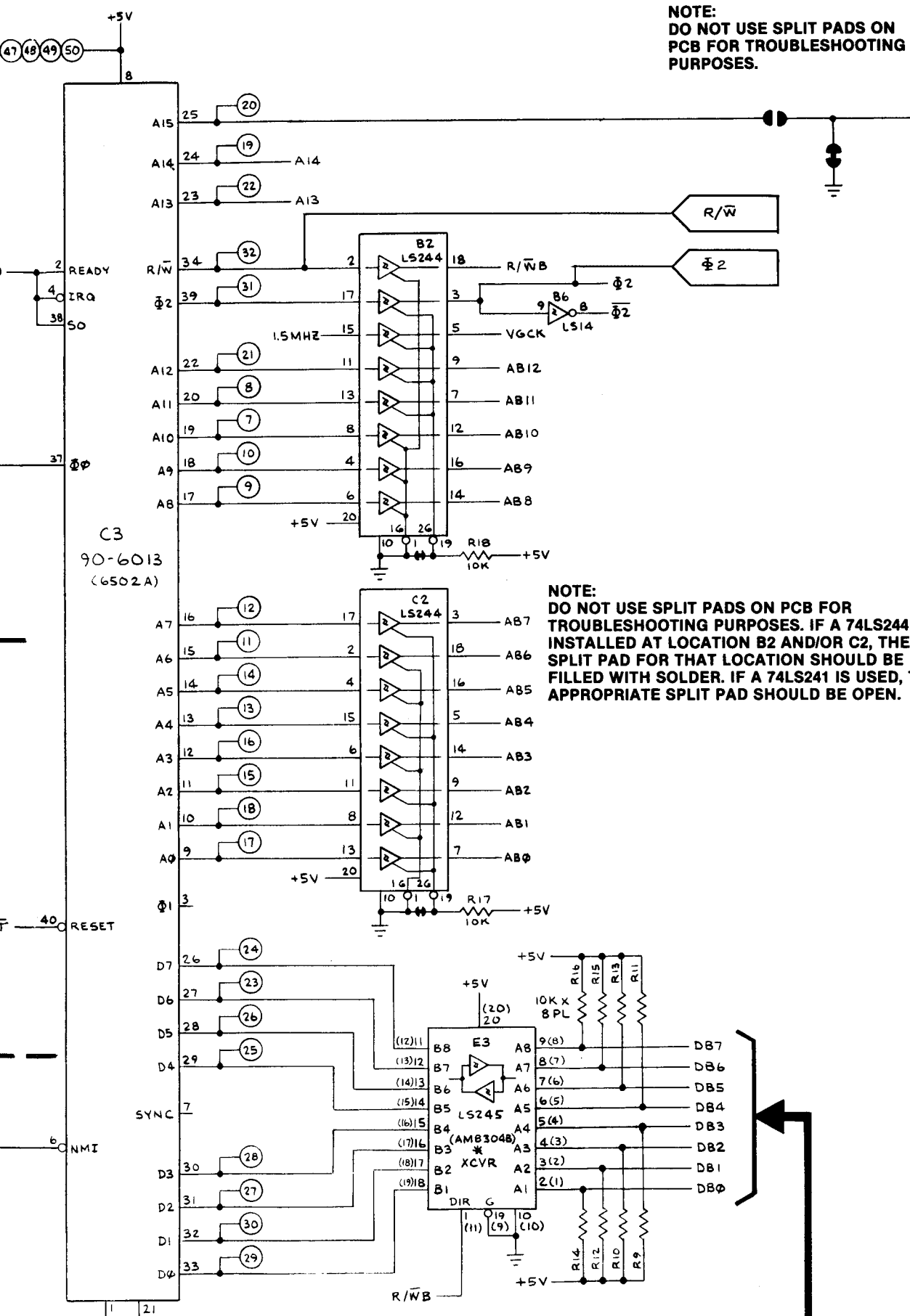
FROM SWITCH INPUTS SHEET 2, SIDE B

ROM/PROM CIRCUITRY

Program Memory for the Asteroids is contained in PROMs for the -01 version ROMs for the -02 version of the PCB equivalent to four PROMs. All PROMs a common enable must be removed with a ROM. For example, remove locations F2, H1, L2 and L1 before ROM at location F1.



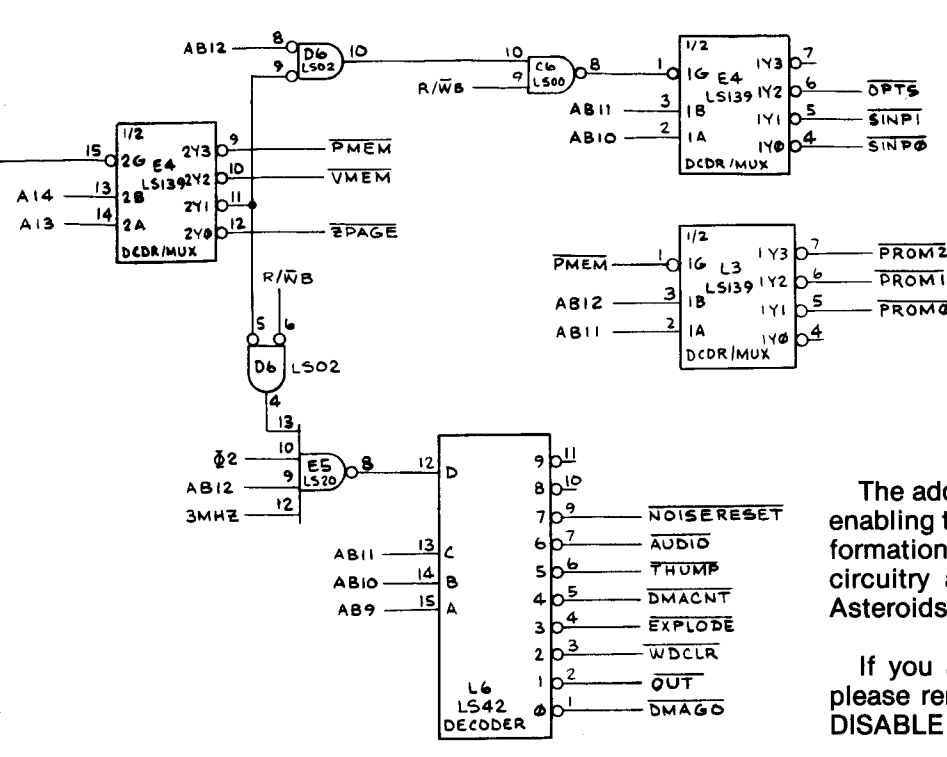
MPU CIRCUITRY



NOTE: DO NOT USE SPLIT PADS ON PCB FOR TROUBLESHOOTING PURPOSES. IF A 74LS244 IS INSTALLED AT LOCATION B2 AND/OR C2, THE SPLIT PAD FOR THAT LOCATION SHOULD BE FILLED WITH SOLDER. IF A 74LS241 IS USED, THE APPROPRIATE SPLIT PAD SHOULD BE OPEN.

NOTE: EITHER A 74LS245 OR AN AM8304B MAY BE USED AT LOCATION E3. PIN NUMBERS NOT ENCLOSED IN PARENTHESIS ARE FOR 74LS245. PIN NUMBERS IN PARENTHESIS ARE FOR AN AM8304B.

ADDRESS DECODING CIRCUITRY



The address decoder performs the function of turning on or enabling the appropriate circuitry at the critical time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Asteroids game.

If you are going to use the Automatic RAM/ROM Tester, please remember to remove MPU C3 and ground the WDOG DISABLE test point.

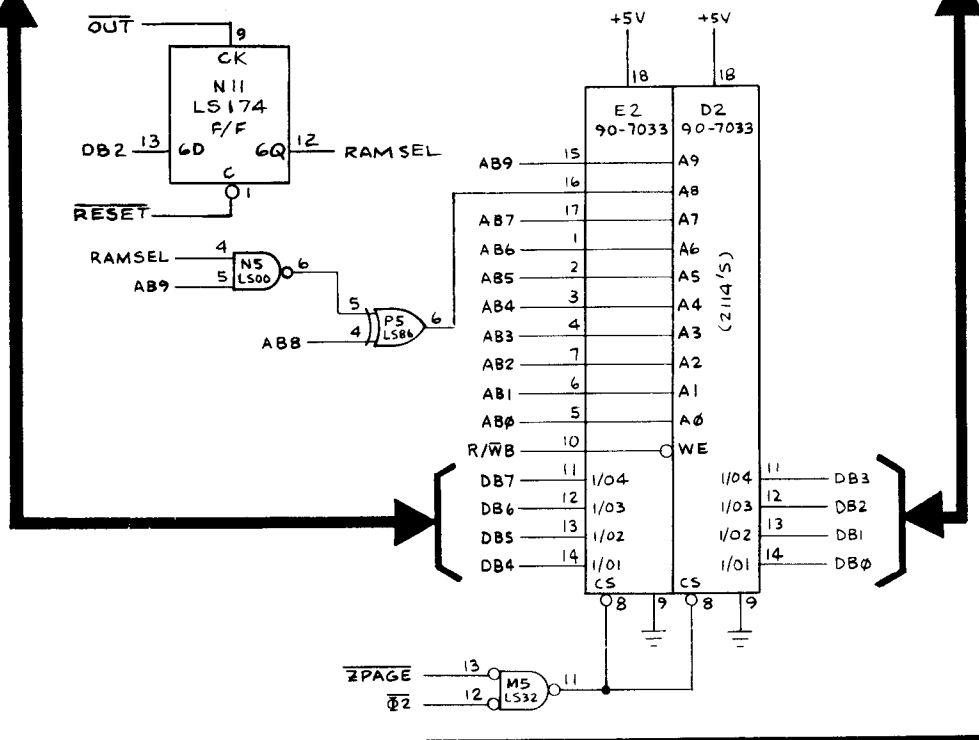
HEXADEDECIMAL	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION		
0000-01FF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	ZERO & ONE PAGE RAM		
0200-02FF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	PLAYER 1 RAM		
0300-03FF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	PLAYER 2 RAM		
2001	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								3 KHz		
2002	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								HALT		
2003	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								HYPERSPACE SW		
2004	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								FIRE SW		
2005	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								DIAG. STEP		
2006	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								SLAM SW		
2007	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								SELF TEST SW		
2400	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								LEFT COIN SW		
2401	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								CENTER COIN SW		
2402	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								RIGHT COIN SW		
2403	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								1 PLYR START SW		
2404	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								2 PLYR START SW		
2405	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								THRUST SW		
2406	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								ROT RIGHT SW		
2407	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D								ROT LEFT SW		
2800	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D									OPT SW (SW8, SW7)	
2801	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D									OPT SW (SW6, SW5)	
2802	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D									OPT SW (SW4, SW3)	
2803	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D									OPT SW (SW2, SW1)	
3000	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W										DMAGO	
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W										2 PLYR START LAMP	
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W										1 PLYR START LAMP	
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W										RAMSEL	
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W										COIN CNTRL LEFT	
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W										COIN CNTRC CENTER	
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W										COIN CNTRR RIGHT	
3600	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W										WDCLR	
3600	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W										EXPLOSION PITCH	
3600	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W										EXPLOSION VOLUME	
3A00	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W										THUMP VOLUME	
3A00	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W										THUMP FREQUENCY	
3C00	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	W											SAUCER SOUND
3C01	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	W											SAUCER FIRE SOUND
3C02	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	W											SAUCER SOUND SELECT
3C03	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	W											SHIP THRUST SOUND
3C04	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	W											SHIP FIRE SOUND
3C05	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	W											LIFE SOUND
3E00	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	W											NOISE RESET
4000-47FF	1	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D		VECTOR RAM	
5000-57FF	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D		VECTOR ROM	
6800-7FFF	1	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D		PROGRAM	

Asteroids game is conversion of the PCB or the PCB. One ROM is all PROMs connected to removed before replacple, remove PROMs at before replacing with

RAM CIRCUITRY

The RAM is the temporary storage space for the MPU and is enabled when ZPAGE (Zero Page enable) is low. When R/WB (from the MPU) is low, the RAM stores the data byte input (DB0 thru DB7) at the location addressed by the MPU address bus (AB0 thru AB7). When R/WB is high, the MPU reads the stored data byte at the addressed location.

The signal RAMSEL, when low, has the effect of swapping pages 2 and 3 within the RAM. This allows greater programming flexibility.



Memory Components and Their Equivalents (Locations Shown in Bold)

-01 P.C. Boards (PROMs)	Alternate -01 P.C. Boards (PROMs)	-02 P.C. Boards (ROMs)
035131-01 J2		
035132-01 N2	035150-01 J2	
035137-01 K1		035143-01 C1
035138-01 N1	035153-01 K1	
035133-01 H2		
035134-01 M2	035151-01 H2	
035139-01 J1		035144-01 D/E1
035140-01 M1	035154-01 J1	
035135-01 F2		
035136-01 L2	035152-01 F2	
035141-01 H1		035145-01 F1
035142-01 L1	035155-01 H1	

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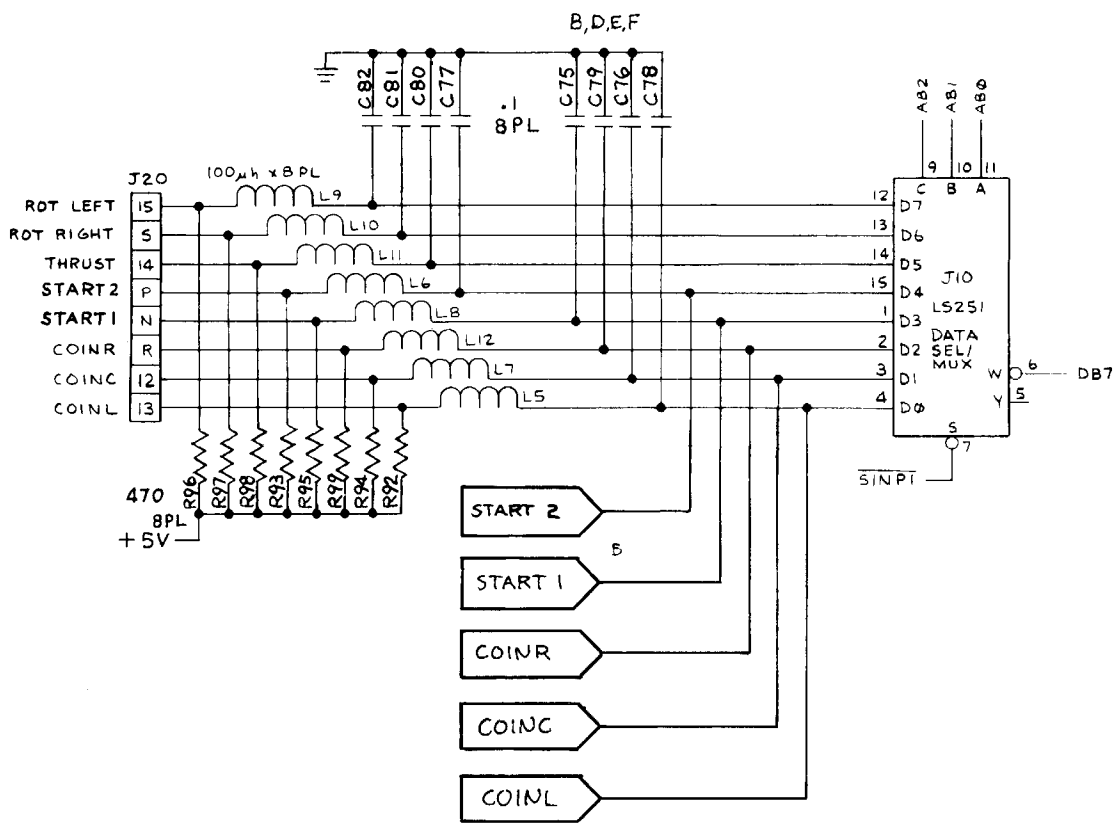
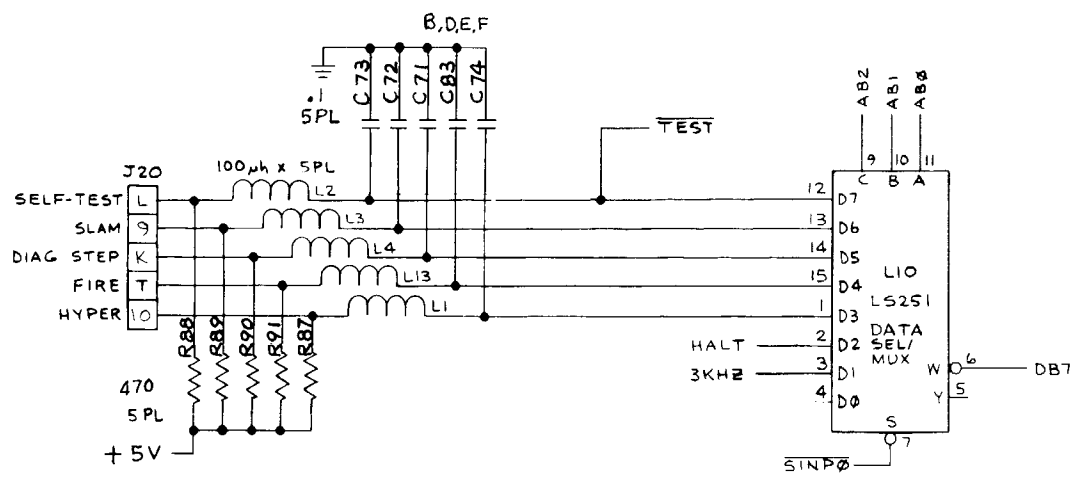


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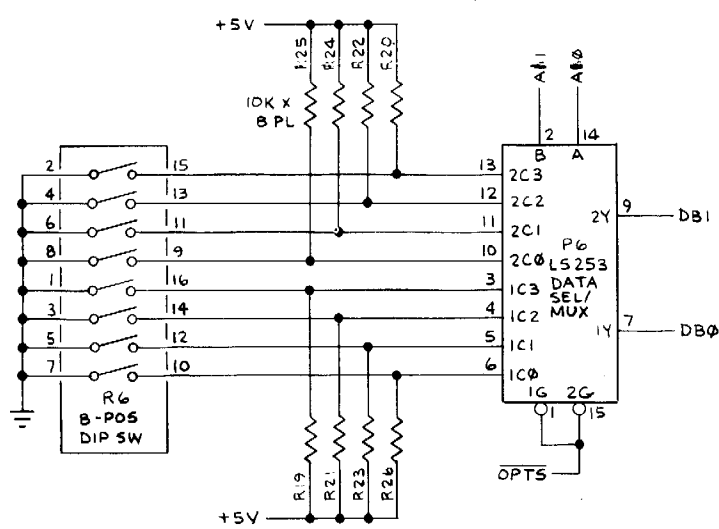
Sheet 1, Side B
ASTEROIDS
 Microprocessor
 Section of 034986-XX **F**

INPUTS

PLAYER INPUT CIRCUITRY



OPTIONS INPUT CIRCUITRY

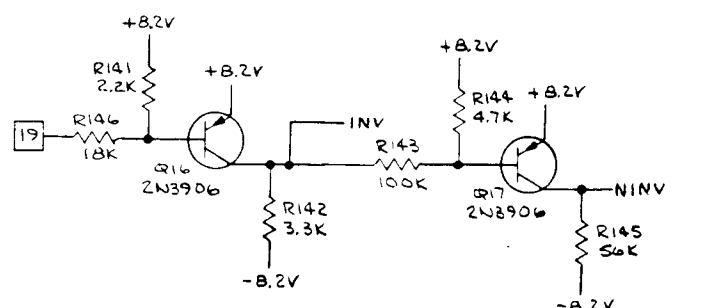


DIAG STEP (diagnostic step), 3 KHZ, SELF-TEST SLAM, HALT, FIRE and HYPER inputs are read by the MPU when SINP0 (switch input zero enable) is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on DB7. Switch inputs are active when pulled to ground. DIAG STEP, 3 KHZ, and SELF-TEST are signals read by the MPU to initiate and control the game's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the antislam switch mounted on the coin door. The MPU reads HALT to determine the state of the vector generator.

The coin door and some control panel switches are read by the MPU when SINP1 (switch input one enable) is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on data line DB7. Switch inputs are "on" when pulled to ground.

The game option switches are read by the MPU when OPTS (option switch enable) is low. Switch toggles to be read are selected by AB0 and AB1 from the MPU. Switch toggles 1, 3, 5, and 7 are read on data line DB0 and toggles 2, 4, 6 and 8 are read on DB1. Toggle inputs are "on" when pulled to ground.

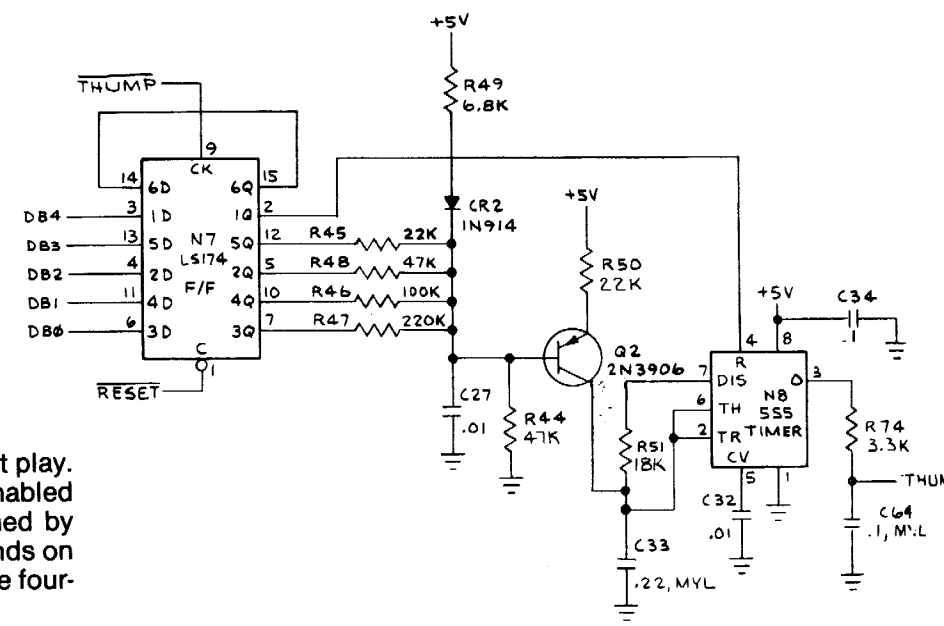
VIDEO INVERTER



The video inverter circuitry is only used in a cocktail game. In an upright game, pin 19 is unconnected and therefore floats. When pin 19 floats, transistor Q16 is turned off and transistor Q17 is turned on. Therefore, INV is -8.2 VDC and NONINV is about +8.2 VDC. The result is a non-inverted X-axis and Y-axis output.

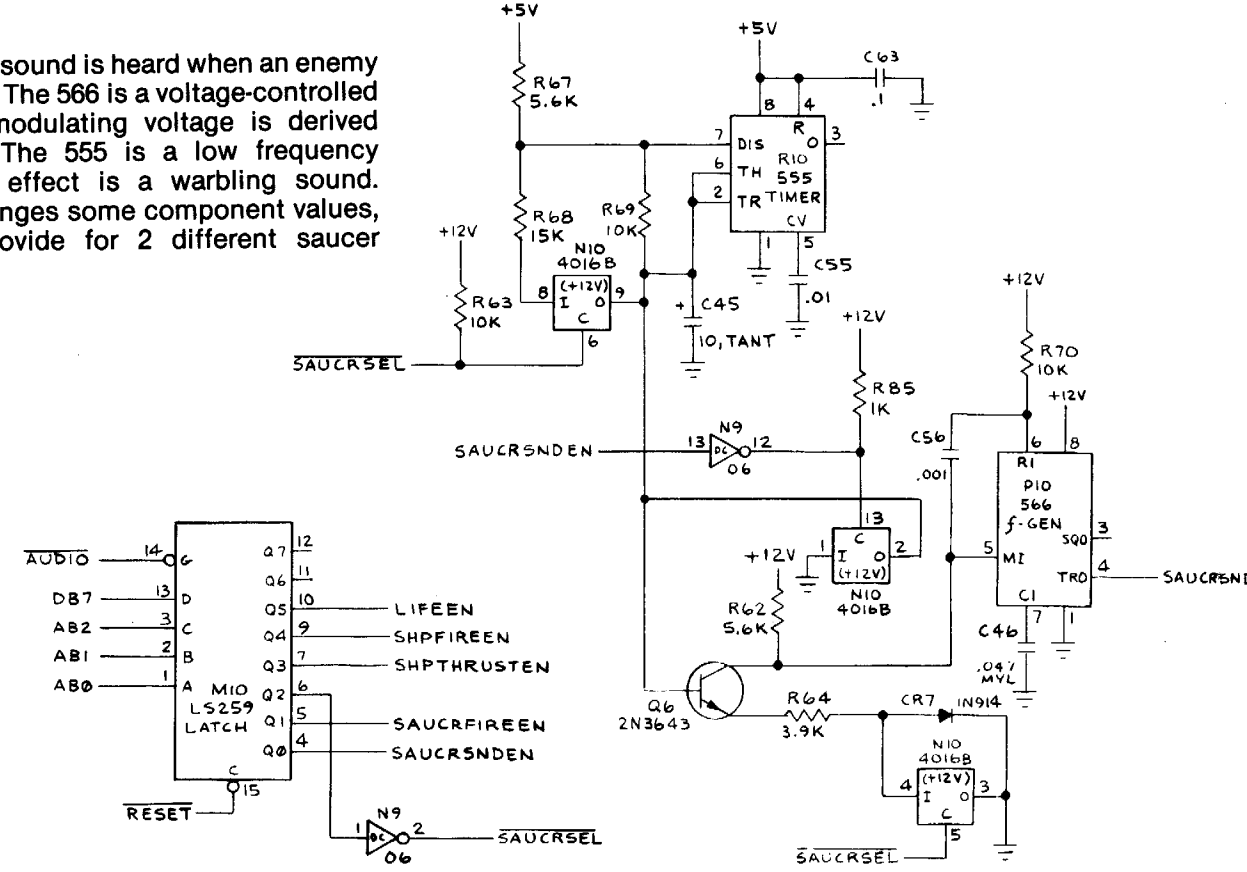
In a cocktail game, the wiring harness shorts connector J20's output pin 7 input pin 19. When the video of player 1 is being displayed, pins 7 and 19 are +5 VDC. This results in a non-inverted video output. When the video for player 2 is being displayed, pins 7 and 19 are grounded. This causes transistor Q16 to be turned on and Q17 to be turned off. Therefore, INV is +8.2 VDC and NONINV is -8.2 VDC. The result is an inverted X-axis and Y-axis output, causing the monitor's display to be upside down.

OUTPUTS



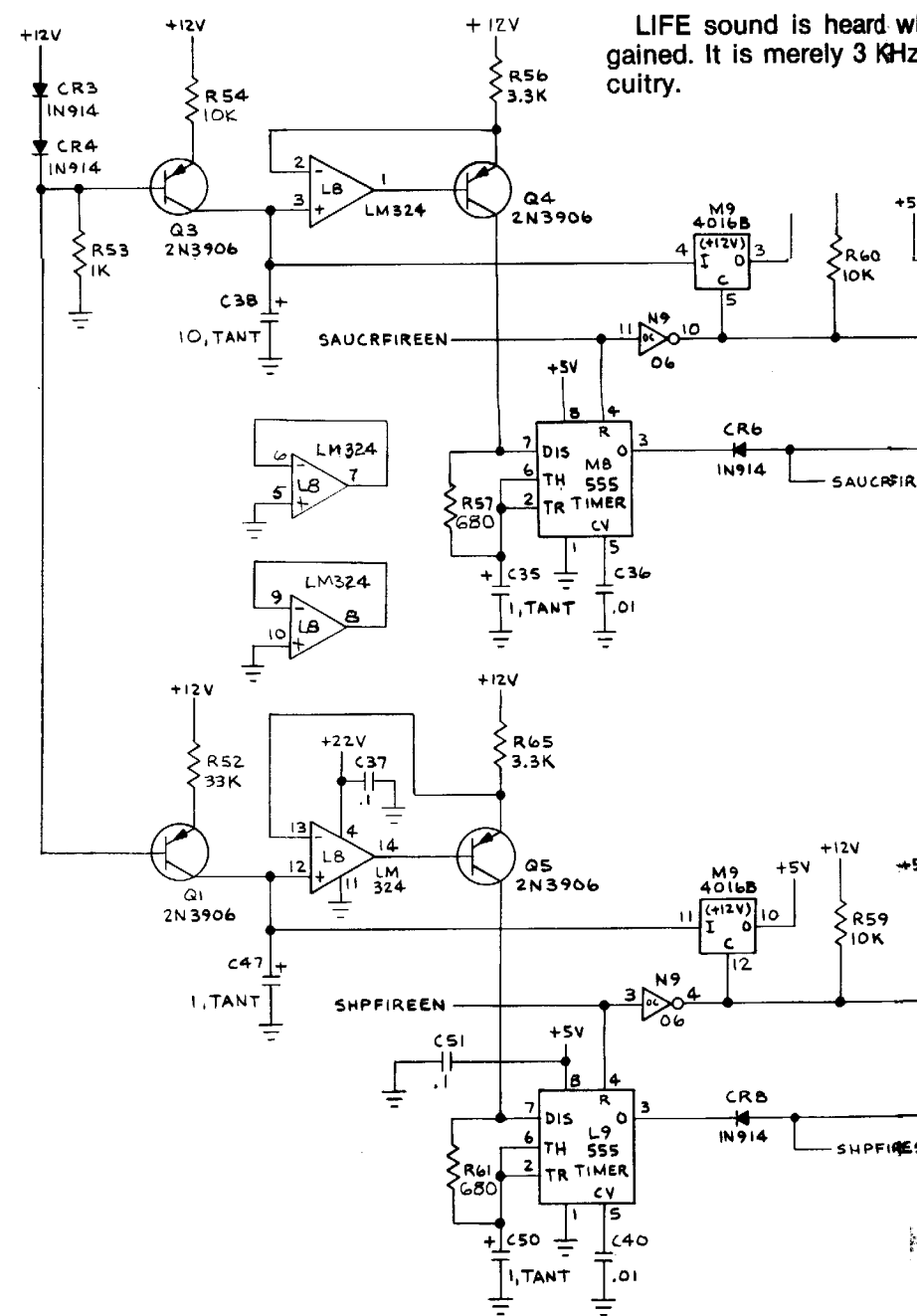
The THUMP sound is heard throughout play. The 555 is connected as an oscillator, enabled by N7 pin 2. The frequency is determined by the current coming out of Q2. This depends on its base voltage, which is derived from the four-bit code in N7.

The SAUCER sound is heard when an enemy saucer appears. The 566 is a voltage-controlled oscillator. Its modulating voltage is derived from the 555. The 555 is a low frequency oscillator. The effect is a warbling sound. SAUCRSEL changes some component values, in order to provide for 2 different saucer sounds.



M10 latches control signals to enable different sounds.

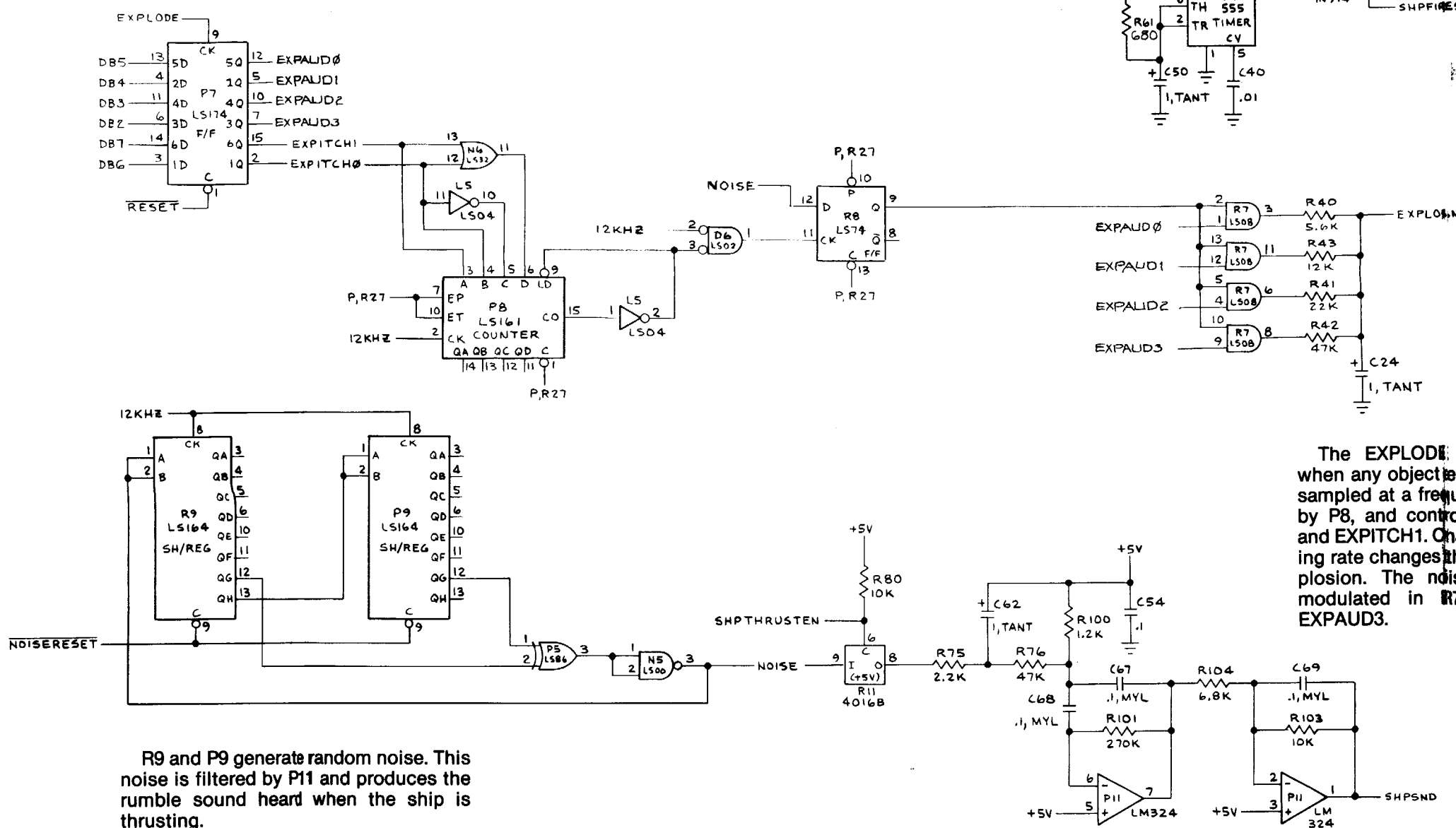
The Fire sounds for the Saucer and the Space Ships are generated by two identical circuits. Each contain a 555 operating as a voltage-controlled oscillator. The Saucer Firesound is initiated by SAUCRFIREEN, and the Space Ship Fire sound is initiated by SHPFIREEN. Each of the 555s is configured in such a way that when they are enabled, they output a signal of a specific frequency and amplitude. This signal begins to decay immediately, both in frequency and amplitude, due to the discharge of the control capacitors (C38 & 39 for Saucer Fire Sound; C47 & 48 for Ship Fire Sound).



LIFE sound is heard when an enemy saucer is gained. It is merely 3 KHZ circuitry.

denotes change by indicated revision

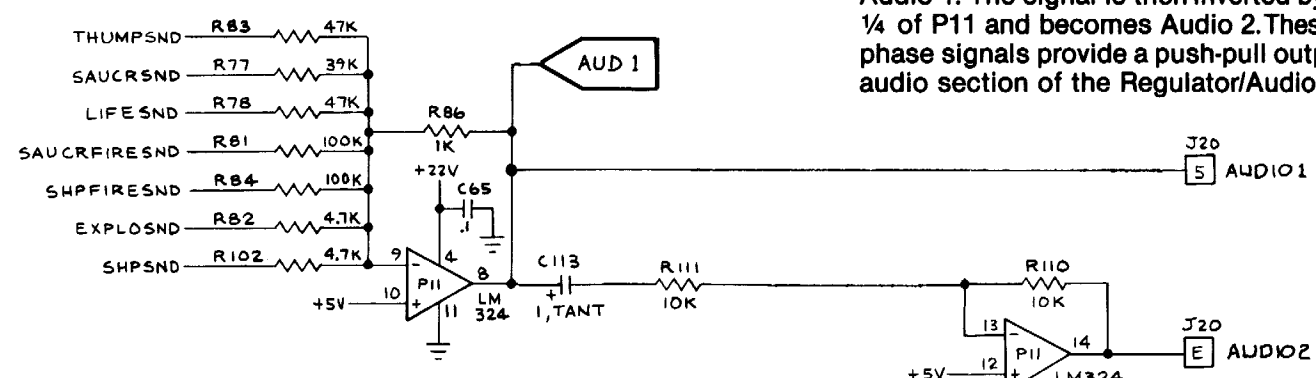
VIDEO INVERTER



R9 and P9 generate random noise. This noise is filtered by P11 and produces the rumble sound heard when the ship is thrusting.

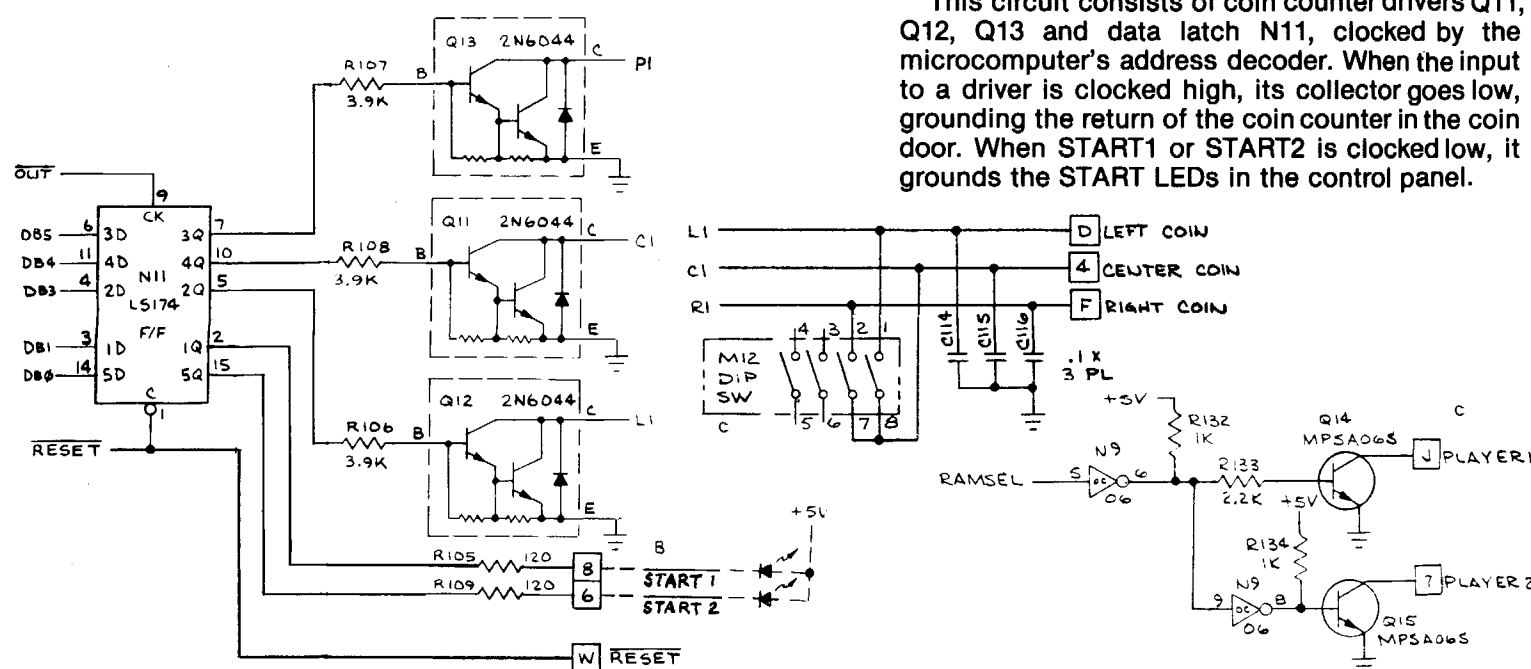
The EXPLODE sound is heard when any object is sampled at a frequency by P8, and controlled by EXPITCH1. Changing rate changes the position. The noise is modulated in EXPALD3.

AUDIO OUTPUT



All sounds are mixed in 1/4 of P11. This is Audio 1. The signal is then inverted by another 1/4 of P11 and becomes Audio 2. These out-of-phase signals provide a push-pull output to the audio section of the Regulator/Audio PCB.

LAMP, LED, AND COIN COUNTER OUTPUT

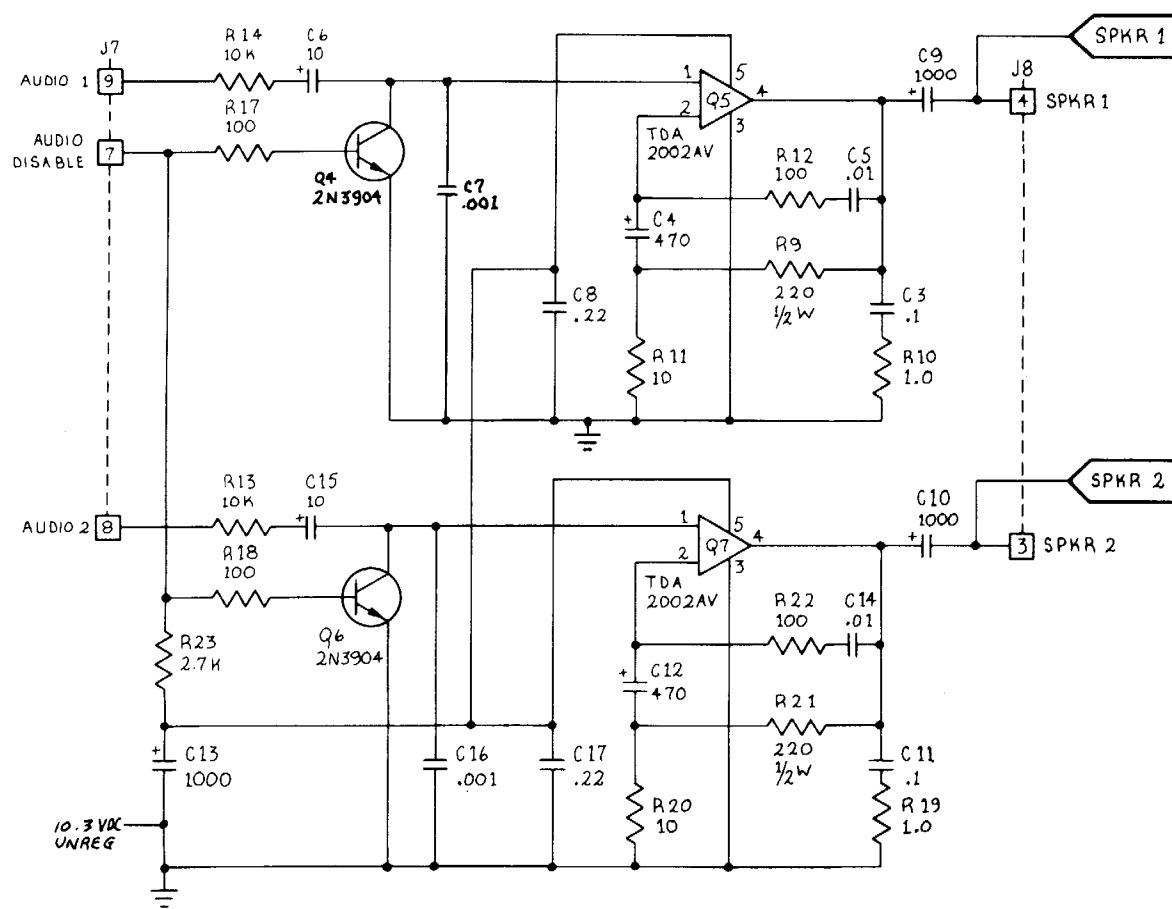


This circuit consists of coin counter drivers Q11, Q12, Q13 and data latch N11, clocked by the microcomputer's address decoder. When the input to a driver is clocked high, its collector goes low, grounding the return of the coin counter in the coin door. When START1 or START2 is clocked low, it grounds the START LEDs in the control panel.

PART OF REGULATOR/AUDIO PCB

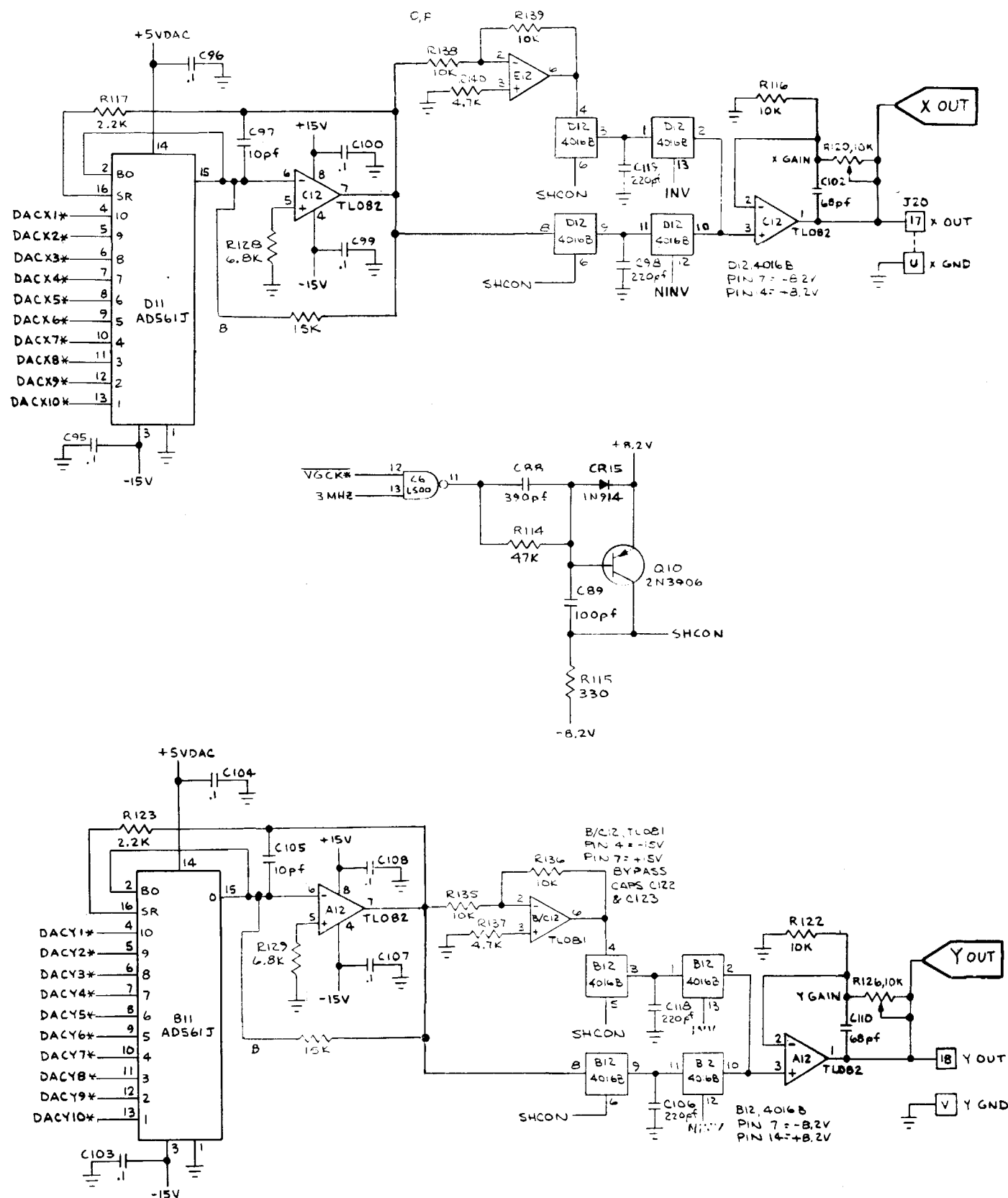
NOTE: AUDIO AMPLIFIER IS PART OF REGULATOR/AUDIO PCB AND IS REPEATED ON SHEET 1, SIDE A.

Audio inputs AUDIO 1 and AUDIO 2 receive out of phase signals for push-pull operation. AUDIO DISABLE is permanently grounded for continuous audio amplification.



denotes a test point

VIDEO OUTPUTS



The video output circuit consists of three individual circuits; X axis, Y axis, and Z axis video output circuits. The X axis and Y axis video output circuits each consist of a digital-to-analog converter (DAC), current-to-voltage converter, two sample and holds, and amplifier. The Z axis video output circuit consists of a shift register and a summer.

X and Y Outputs

The DACs (D11 and B11) each receive binary numbers from the vector generator's position counters outputs. These numbers represent the location of the beam on the monitor. For the non-inverted X axis, the numbers range from 0 to 1023, where 0 is at the far left of the monitor screen, 512 is at the center, and 1023 is at the far right. For the non-inverted Y axis, the numbers range from 128 to 996, where 128 is at the bottom of the monitor screen, 512 is at the center, and 996 is at the top. When the X axis and Y axis are inverted, the monitor picture is turned upside down. This is used for a two-player cocktail game.

The DACs convert these binary number inputs to current outputs. The DACs' current outputs are applied to the pin 6 inputs of current-to-voltage converters C12 and A12.

From the current-to-voltage converters, the signal is fed to two sample-and-hold circuits: One is non-inverted and the other is inverted. The non-inverted sample and hold consists of one stage of analog switch D12 and capacitor C98 for the X axis, and B12 and C106 for the Y axis. The inverting sample and hold consists of inverter E12, one stage of analog switch D12, and capacitor C119 for the X axis and B/C12, B12 and C118 for the Y axis.

The sample and hold circuits are controlled by SHCON (sample and hold control). SHCON is derived by gating 3 MHz from the microcomputer clock circuitry and VGCK* from the vector generator's state generator. The result of these inputs insures that the non-inverted and inverted analog signals that are applied to the analog switches have sufficiently stabilized before being applied to the sample and hold capacitors.

The output swing of SHCON is -8 to +8 VDC. When SHCON is high, the voltage charges or discharges the sample-and-hold capacitors to the X and Y analog voltage value. The voltages are then applied to the inputs of the second analog switch. These switches select either the non-inverted or inverted X-axis and Y-axis outputs. The outputs are then amplified by the second stages of C12 and A12 for an impedance-matched output to the X and Y inputs to the monitor. Since the monitor doesn't have field-adjustable X and Y gains, the gains are adjustable by variable resistors R120 and R126.

Z Output

The Z axis video output receives six inputs. BVLD (beam valid), from the output of the vector generator's position counters, tells the Z axis to draw the line. BLANK (vector line blank), from the vector generator's state machine, tells the Z axis to stop drawing a line. SCALE0 thru SCALE3 (grey level shading scale), from the output of the vector generator's data latch, tells the Z axis the grey level shading of the line that is being drawn on the monitor.

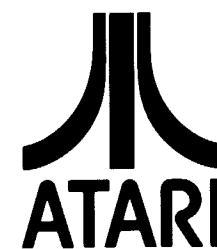
When BVLD and BLANK are both high, a high is clocked through shift register K9 that turns transistor Q3 off. This allows the scale inputs to be passed through transistor Q2. When BLANK goes low, a low is clocked through K9, transistor Q3 turns on, and the signal is grounded at the base of transistor Q2.

The scale inputs at the base of transistor Q1 determine Q1's emitter voltage, during the line draw period. The SCALE0 thru SCALE3 resistors R36 thru R39, resistor R35, and resistor R40 result in a range of about +1.0 VDC when all are low and +4.0 VDC when all are high. The emitter of Q1 follows at about +1.7 to 4.7 VDC, while the emitter of transistor Q2 follows at about +1.0 to 4.0 VDC. This output is applied to the Z input of the monitor. Since there are brightness and contrast controls in the monitor, there are no adjustments in this circuit.

Sheet 2, Side B

ASTEROIDS Switch Inputs, Coin Counter, LED and Audio Outputs Section of 034986-XX F

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