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LIBERATOR™

Operation, Maintenance, and Service Manual

Complete with Illustrated Parts Lists

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Complete with Illustrated Parts Lists

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Notice Regarding Non-ATARI Parts

WARNING

Use of non-ATARI parts or modifications of your ATARI® game circuitry may adversely affect the safety of your game, and may cause injury to you and your players.

You may void the game warranty (printed on the inside back cover of this manual) if you do any of the following:

- substitute non-ATARI parts in the game
- modify or alter any circuits in the game by using kits or parts *not* supplied by Atari.

to licensed communications services is not permitted by the Federal Communications Commission (FCC).

If you suspect interference from an ATARI® game at your location, check the following:

- all green ground wires in the game are properly connected as shown in the the game wiring diagram
- the power cord is properly plugged into a **grounded** 3-wire outlet.

If you are unable to solve the interference problem, please contact ATARI Customer Service. See the inside front cover for service in your area.

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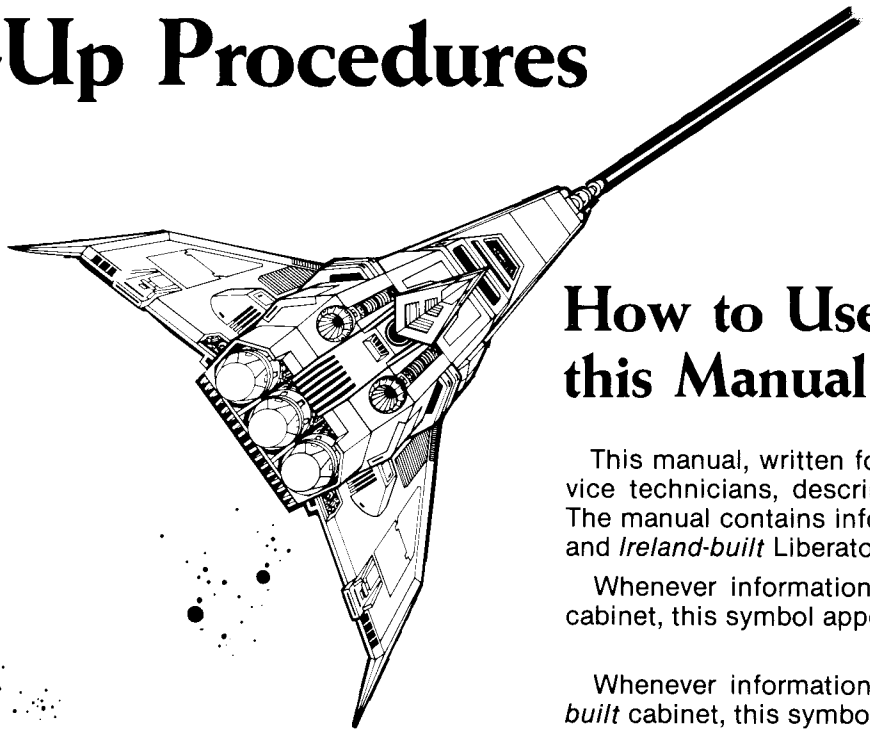


How to Use this Manual

This manual, written for game operators and service technicians, describes the Liberator™ game. The manual contains information about the *Upright* and *Ireland-built* Liberator cabinets.

Whenever information is unique to the *Upright* cabinet, this symbol appears: 1

Whenever information is unique to the *Ireland-built* cabinet, this symbol appears: ♣

Chapter 1 describes new features, game setup, settings of option switches, self-test procedures, and game play.

Chapter 2 contains self-test procedures.

Chapter 3 details maintenance, repair, and parts information.

A ***glossary of terms*** is in the back of this manual for your convenience.

In addition, schematic diagrams of the game circuitry are included with this manual.

Figures 1-1 and 3-1 illustrate the game cabinet. Italicized lettering on these figures refers you to other places in the manual for information about specific cabinet parts.

Chapter 1

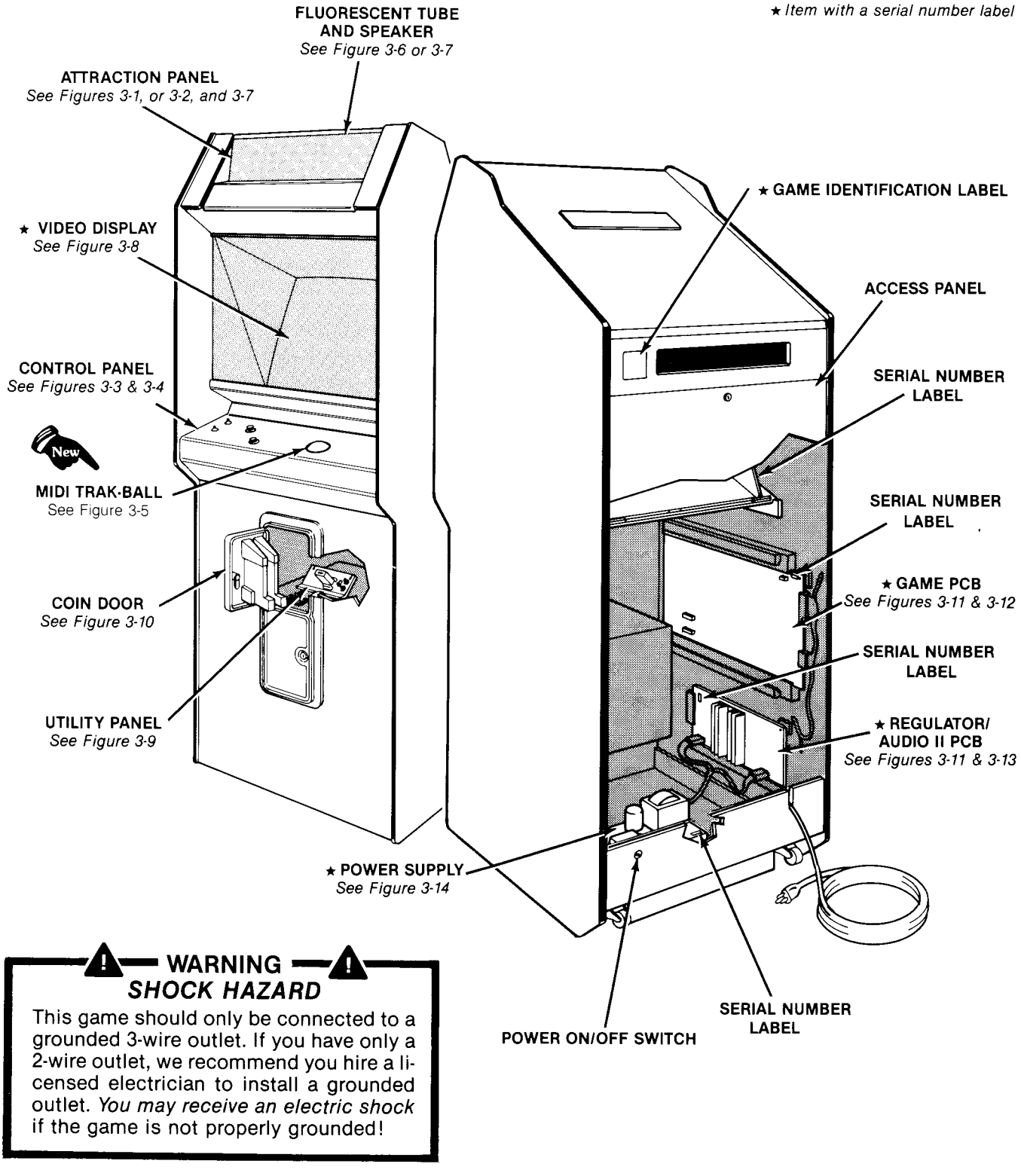


Figure 1-1 Game Overview

A. New Features

The Liberator™ game has four new features. Even if you are familiar with ATARI® games, you should note these important differences:

1. **Shielded Game Speakers.** These 8-ohm, 6-ounce, high-fidelity speakers provide exceptional audio. The speaker magnets are shielded.
2. **Midi Trak-Ball™.** The popular Trak-Ball™ assembly has been enlarged and simplified. The housing for this control is a molded plastic frame with two parts. Smooth action of the Midi Trak-Ball improves player accuracy.
3. **Grey Tinted Glass.** This new shade of tempered glass used in the display shield enhances video colors.
4. **Molded Coin Box.** This game has a sleek, one-piece molded coin box with handles on either end for easy carrying.

New features and all other major parts of the game are illustrated in Figure 1-1. Throughout this manual, wherever one of these new features is mentioned, you will see this symbol:

B. Inspecting the Game

Please inspect your game carefully to ensure that it was delivered to you in good condition.

WARNING

To avoid electrical shock, do not plug in the game until inspection and installation have been completed!

1. Examine the exterior of the game cabinet for dents, chips, or broken parts.
2. Remove the screws that were used as extra security to seal the rear access panel. Unlock and open this panel and the coin door; inspect the interior of the game as follows:
   a. Ensure that all plug-in connectors (on the game harness) are firmly plugged in. Replug any connectors found unplugged. **Do not force connectors together.** The connectors are keyed so they only fit in the proper orientation. **A reversed edge connector may damage a PCB** and will void your warranty.
   b. Ensure that all plug-in integrated circuits on the PCB are firmly plugged into their sockets.
   c. Remove the tie-wrap that secures the coiled power cord inside the cabinet. Inspect the power cord for any cuts or dents in the insulation. Repair or replace it as required. Place the square black plastic strain-relief plate in the wood slot at the bottom of the rear panel opening.
   d. Note the game serial number printed on a label on the back of the cabinet. Verify that the same serial number is also on the Liberator game PCB, Regulator/Audio II PCB, power supply, and video display. See *Figure 1-1* for locations of the serial-numbered components. Please mention this serial number whenever you call your distributor for service.
   e. Inspect major subassemblies, such as the power supply, control panel, and video display. Make sure that they are mounted securely.

WARNING

To avoid electrical shock, do not touch internal parts of the display with your hands or with metal objects held in your hands!

C. Space and Power Requirements

1. Installation Requirements

Power	200 W
Temperature	0 to +38°C (+32 to +100°F)
Humidity	Not over 95% relative
	Upright Cabinet
Space Required	62 x 78 cm (25¼ x 30½ in.)
Game Height	184 cm (72 ½ in.)
	Ireland-Built Cabinet
Space Required	60 x 68 cm (24 x 27 in.)
Game Height	170 cm (67 in.)

2. Selecting the Voltage Plug

The power supply used in this game operates on the line voltage of almost any country in the world. The power supply comes with either one, two, or three separate voltage-selection plugs. Plug voltages and wire colors are 100 VAC (violet wire color), 120 VAC (yellow wire color), 220 VAC (blue wire color), and 240 VAC (brown wire color).

Before plugging in your game, check your line voltage. Next, check the wire color on the voltage selection plug that is plugged into your power supply. Make sure the voltage selection plug is correct for the voltage of your location (see *Figure 3-14*).

D. Locating the Switches

1. On/Off Switch

The on/off switch is located on the back of the cabinet on the lower left side (see *Figure 1-2*).

2. Utility Panel Switches

The utility panel includes the volume control, self-test switch, coin counter(s), and auxiliary coin switch (used to credit the game without activating the coin counter). The utility panel is located inside the upper coin door (see *Figure 1-2*).

3. Option Switches

Option switches are located on the game PCB (see *Figure 1-2*).

a. Game-price options are at PCB location A4.
b. Game-play options are at PCB location D4.
c. Coin-counter options are at PCB location T12.

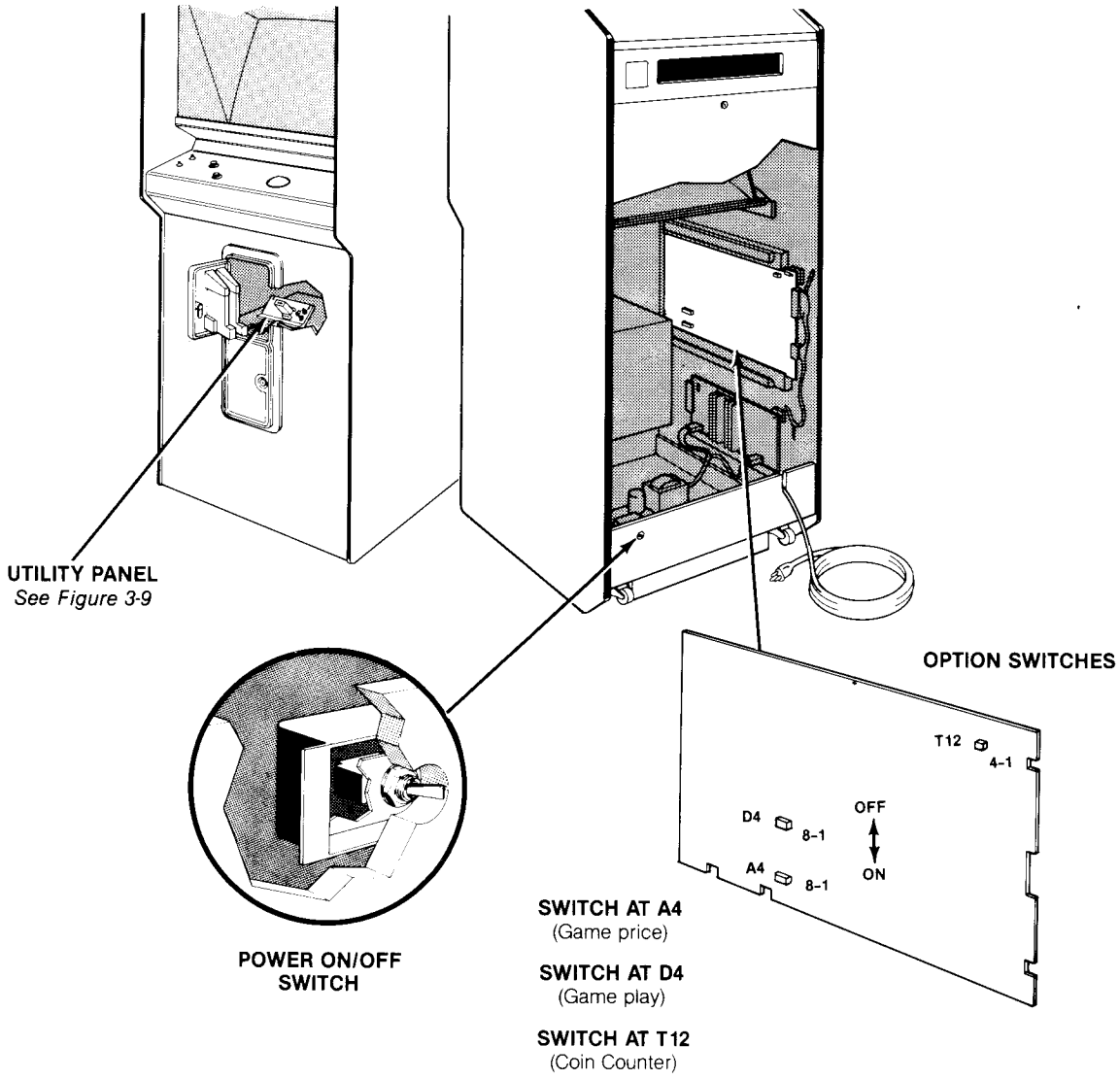


Figure 1-2 Location of Game Switches

E. Setting the Option Switches

Settings of the game option switches are explained in Tables 1-1 and 1-2. Options preset at the factory are shown by the ◄ symbols. However, you may change the settings according to your individual needs.

To verify option switch settings, first toggle the on/off switch to the *off* position and then to the *on* position. Next, set the self-test switch to the *on* position, and verify the settings on the self-test screen. Then set the self-test switch to the *off* position.

Table 1-1 contains the switch settings for options relating to game price, coin mechanism multipliers, and bonus play. The switches are on the game PCB at location A4.

The *multipliers* (toggles 4-6) determine the value of the coin mechanisms to the game's logic. A *coin mechanism* is a device on the inside of the coin door that inspects the coin to determine if the correct coin has been inserted. After this inspection, the mechanism either accepts or rejects the coin. The coin door has two mechanisms.

The basic unit of measurement is a coin worth $.25 or 1 DM, which equals a multiplier of x1. For example, if you have a 2 DM/1 DM coin door, you may want to set the left multiplier at x2 and the right multiplier at x1.

You may offer *bonus play* for certain combinations of coins inserted. For example, with the game set at $.25 per play, players who deposit four successive $.25 coins before pressing the start switch can receive a bonus play. The bonus feature encourages players to insert more money than just the minimum $.25 required for one game.

Switch 1 of the 4-toggle switch at **PCB location T12** should be set in the *on* position. For the *Ireland-built* cabinet, this ensures that a coin inserted in either coin mechanism will be counted. Switches 2, 3, and 4 are not used.

Table 1-1 Switch Settings for Price Options

Settings of 8-Toggle Switch on Liberator PCB *(at A4)*								
8	7	6	5	4	3	2	1	Option
Off	Off							Free play
On	Off							1 coin for 2 credits
Off	On							1 coin for 1 credit ◄
On	On							2 coins for 1 credit
		Off	Off					Right coin mechanism x 1 ◄
		On	Off					Right coin mechanism x 4
		Off	On					Right coin mechanism x 5
		On	On					Right coin mechanism x 6
				Off				Left coin mechanism x 1 ◄
				On				Left coin mechanism x 2
					Off	Off	Off	No bonus coins ◄
					Off	On	Off	For every 4 coins inserted, logic adds 1 more coin
					On	On	Off	For every 4 coins inserted, logic adds 2 more coins
					Off	Off	On	For every 5 coins inserted, logic adds 1 more coin
					On	Off	On	For every 3 coins inserted, logic adds 1 more coin
					Off	On	On	No bonus coins
					On	On	On	No bonus coins

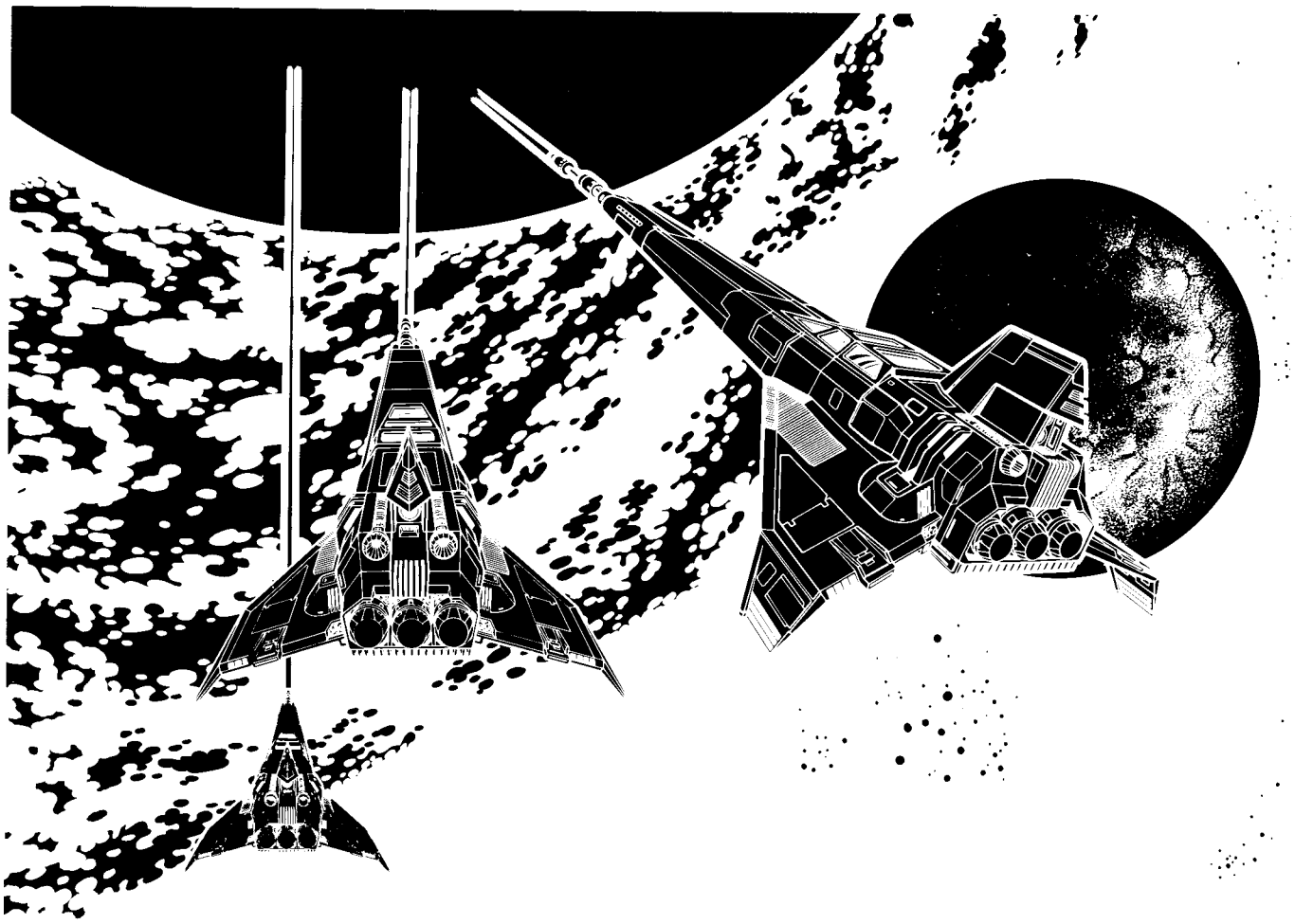
◄ *Manufacturer's recommended settings*

Table 1-2 contains the switch settings for options relating to number of ships per game, bonus levels, and game difficulty. The switches are on the game PCB at location D4.

Table 1-2 Switch Settings for Play Options

Settings of 8-Toggle Switch on Liberator PCB *(at D4)*								
8	7	6	5	4	3	2	1	Option
Off	Off							4 ships per game ◄
On	Off							5 ships per game
Off	On							6 ships per game
On	On							8 ships per game
		Off	Off			*Not used*	*Not used*	Bonus ship every 15,000 points
		On	Off					Bonus ship every 20,000 points ◄
		Off	On					Bonus ship every 25,000 points
		On	On					Bonus ship every 30,000 points
				On	Off			Easy game play
				Off	Off			Normal game play ◄
				Off	On			Hard game play

◄ *Manufacturer's recommended settings*



F. Performing the Initial Self-Test

This game will test itself and provide data to show that the game's circuitry and controls are operating properly. The data is provided on the video display and speaker. No additional equipment is necessary.

Wait at least 10 seconds after playing a game before switching to the Self-Test Mode. Otherwise, you may erase the top three scores in the high-score table or distort the statistics. All credits will be cancelled when you switch to self-test.

Refer to Figure 1-2 for the location of the self-test switch and option switches. Set the self-test switch to the *on* position (see *Figure 1-3*) to see the Self-Test Display in the Self-Test Mode. To exit the Self-Test Mode, set the self-test switch to the *off* position.

The complete self-test procedure is explained in *Chapter 2, B. Self-Test Procedure.*

We suggest you perform the self-test procedure when you first set up the game, any time you collect money from the game, when you change game options, or when you suspect game failure.

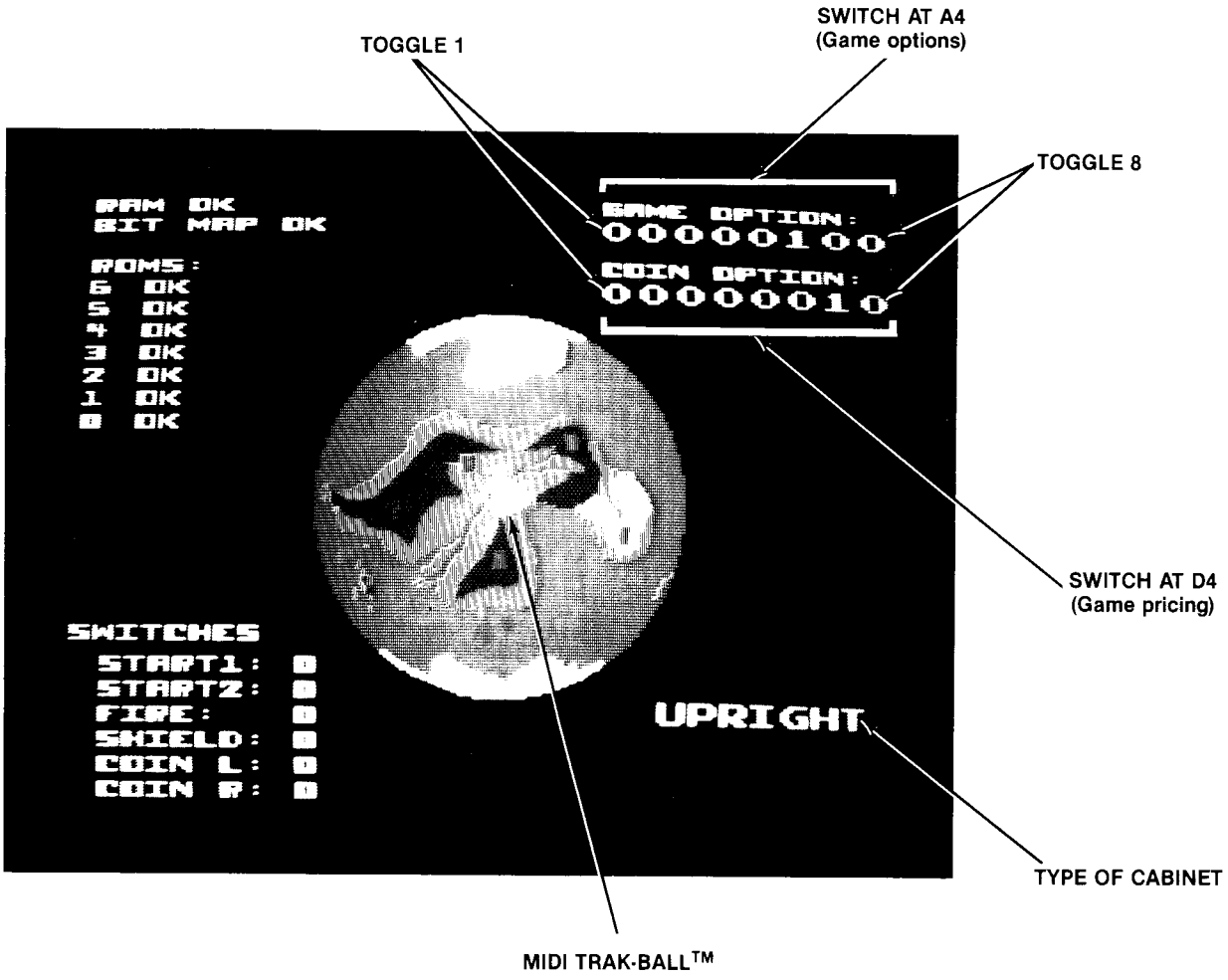


Figure 1-3 Self-Test Display

Table 1-3 Self-Test Procedure

Instruction	Test Passes
1. Switch the self-test switch to the *on* position.*	The screen goes blank for a few seconds while a continuous low-to-high tone sounds. This tone means the VBLANK and timing circuits are working correctly. If there is no tone, refer to *Chapter 2, Self-Test Procedure.* The self-test display appears. RAMs, ROMs, and the bit map are tested. If the screen is different from the self-test display, or if there are sounds, refer to *Chapter 2, Self-Test Procedure.*
2. Press the control panel pushbuttons and the left and right coin switches. Roll the Midi Trak-Ball™.	As you press the pushbuttons or switches, you will hear a tone, the screen will change color, and the corresponding *0* will change to *1*. Pressing any pushbutton or switch will change the color of the screen and will change the appearance of the planet alternately from Earth to Jupiter. The (Midi Trak-Ball) cursor moves freely. If the test fails, refer to *Chapter 2, Self-Test Procedure.*
3. Press the auxiliary coin switch on the utility panel.	The screen displays the game bookkeeping statistics as follows: • Average of the total game scores • Average cumulative game time • Number of one-player games played • Number of two-player games played If the test fails, refer to *Chapter 2, Self-Test Procedure.*
4. Press the auxiliary coin switch.	The screen displays the following color bar pattern: • Three shades of blue (light to dark) • Seven shades of green (light to dark) • Seven shades of red (light to dark) • Alternate white and black squares If the test fails, refer to *Chapter 2, Self-Test Procedure.*
5. Press the auxiliary coin switch.	A grid pattern framed in red and green appears on the screen. The corners of the green frame must be visible at all times; the corners of the red frame may or may not be visible. The corners of the display should cut across the blue boxes located in the corners of the convergence display between the red and green frames. If the test fails, refer to *Chapter 2, Self Test Procedure, Screen 4.*

**All credits are cancelled when you switch to self-test.*

G. Game Play

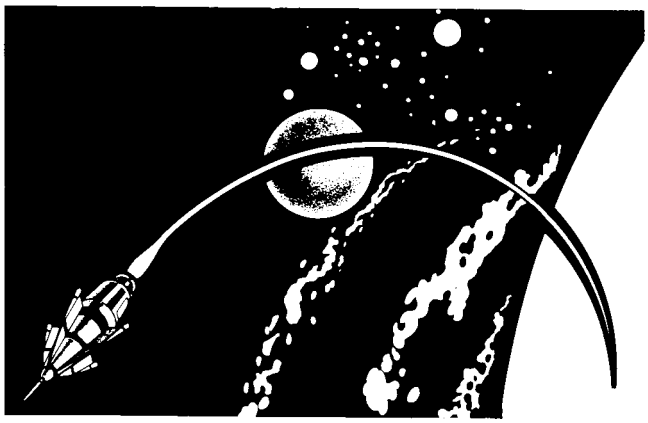
Liberator™ is a one- or two-player game with a color raster-scan video display. The game action takes place in various star systems in outer space. There are missile bases on planets and enemy spaceships that the player tries to destroy. The object of the game is to find and destroy the enemy missile bases.

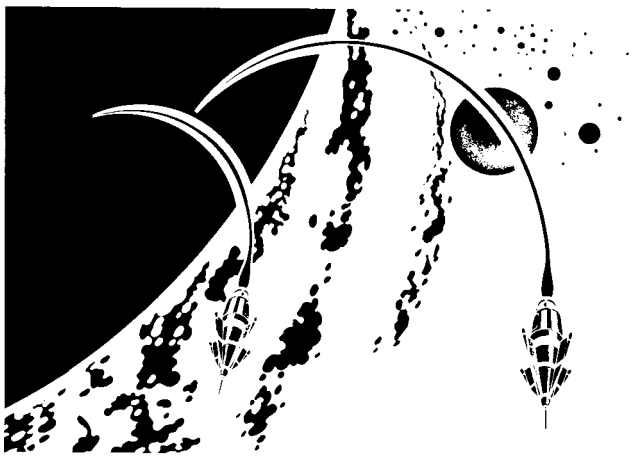
The player controls a fleet of four spaceships, each located in a corner of the screen. Each ship has a weapon that shoots a laser beam. A fleet of four spaceships may have as many as 12 shots on the screen at one time. The player uses the Midi Trak-Ball™ to control a cursor (⊕ mark) that appears on the screen. The ⊕ marks where a laser shot is to explode. When the player presses the FIRE button, a laser beam is launched from the nearest spaceship to the ⊕. When the beam reaches the ⊕ there is an explosion. Any object within the explosion is destroyed. Nearby objects may also be damaged.

To protect his spaceship, a player may use the SHIELD button. Each ship has four shields at the beginning of a level of play. A hit to a shield destroys that shield and the corresponding shields that protect other spaceships.

When starting a game, a player may select an advanced level of play. When a game ends, the message *FOR ADVANCED GAME HOLD FIRE AND PRESS START* appears. The player presses FIRE to select the level of game play. Levels increase by three, up to Level 22. The player starts the game by pushing a start button.

If a player selects and successfully completes a higher level of game play, he is awarded bonus points. There are 30,000 bonus points and a bonus spaceship (for a maximum of eight regular and bonus ships per player) awarded for completion of each star system. There are three levels of game play within each star system. For example, if a player selects and completes Level 22, he is awarded 210,000 bonus points and has eight ships.





Liberator™ has five possible modes of operation: Demonstration, Attract, Play, High-Score, and Self-Test. Self-Test is a special mode for checking the game switches and computer functions. You may switch to the Self-Test Mode during any mode. All credits will be cancelled. Wait at least ten seconds after a game has been played before switching to Self-Test or switching off power; otherwise, you may erase the highscore table.

1. Demonstration Mode

To switch to the Demonstration Mode, simultaneously press any start button and the auxiliary coin switch (located inside the upper coin door). In this mode your spaceships cannot be destroyed by the enemy. Thus, you can see all the star systems and obstacles in the game. To exit this mode, press the auxiliary coin switch.

2. Attract Mode

The Attract Mode begins when power is applied to the game, after a Play or High-Score Mode, or after Self-Test. The Attract Mode ends when a credit is inserted and a start button is pressed, or when the Self-Test Mode begins.

The screen displays one of five possible pictures in the Attract Mode. The first picture takes place in hyperspace and a message to the player reads: *THE GALAXY HAS BEEN INVADED BY THE EVIL MALAGLON ARMY. COMMANDER CHAMPION OF THE ATARI FORCE HAS CHOSEN YOU TO BECOME THE LIBERATOR. THE PEOPLE OF THE UNIVERSE ARE DEPENDING ON YOU TO FREE THEM FROM THEIR EVIL MASTERS.*

In the second picture, the words *JOIN THE ATARI FORCE IN:* appear at the top of the screen. There is a rotating Earth-like planet in the center of the screen. *LIBERATOR* appears in an orbit around the planet. © *ATARI 1982* appears at the bottom of the screen.

The third picture simulates game play. Two messages appear on the screen— *YOUR MISSION: SHOOT RED FLASHING MISSILE BASES ON PLANET* and *PROTECT SHIPS FROM ONCOMING MISSILES.* The number of remaining enemy bases appears at the bottom of the screen.

In the fourth picture, a planet rotates. The messages *ONE OR TWO PLAYERS* and *PRESS START* appear on the screen if the correct number of credits have been inserted.

The High-Score Table appears in the fifth picture. There is a list of the ten highest scores. Opposite each score are the initials of the player who achieved that score.

All pictures in the attract mode display information about the number of coins required to credit the game, and, if applicable, the number of credits shows at the bottom of the screen. The Attract Mode ends when a credit(s) is inserted and the 1- or 2-player button(s) is pressed.

3. Play Mode

The Play Mode begins when the correct amount of credit is inserted and a start button is pressed.

Game play begins in hyperspace of the first star system. Enemy spaceships try to ram and destroy the player's spaceships. The player must destroy these enemy ships using the FIRE button. There is no shield in hyperspace. When the enemy spaceships on the screen are destroyed, *LEVEL 1* and a revolving Earth-like planet appear on the screen.

There are four enemy missile bases on the planet. The base launches missiles toward the player's spaceships. The missiles travel in a curved line. The player must destroy the missiles before they destroy his spaceships. When the missile bases cross an imaginary vertical line in the center of the planet, the bases become satellites. The satellite launches a missile that travels in a straight line toward the player's spaceships.

When all bases are destroyed, the player's remaining spaceships fly to the planet. Bonus points appear at the top of the screen when the ships land on the planet. There are 100 bonus points for each remaining ship. In Level 2 there are 200 bonus points per ship; Level 3 has 300 points; and so on. After Level 7, the bonus is 800 points for each remaining ship. The screen also displays the points at which the next bonus ship will be awarded.

The planets for Levels 2 and 3 contain killer saucers in addition to the missile bases. The saucer flies in space for a period of time and then stops. It emits a sound and begins to increase in size. Then it fires a death ray that cannot be stopped. FIRE and SHIELD offer no protection. The ray destroys the player's ship. The player must destroy the saucer before it increases in size; otherwise, the death ray will destroy his ship.

Game play in the second star system starts in hyperspace with enemy spaceships trying to ram and destroy the player's spaceships. After successfully destroying the enemy ships, Level 4 is displayed with a revolving Earth-like planet. The player has to destroy six missile bases on the revolving planet. Missile bases fire MIRVs, which explode into four smaller missiles when hit. In this system, there are two more planets (Levels 5 and 6) that have killer saucers and missile bases that turn into satellites.

Game play progresses through many star systems. Play in each system begins with enemy spaceships trying to ram the player's spaceships. Next, there are three levels (each with a different planet) within a system. In each new level, the color of the planet changes and the direction of planet rotation reverses. The player score and number of space ships appear at the top of the screen, and the number of missile bases appears at the bottom of the screen. As bases are destroyed, the number decreases to show the remaining bases. Game play proceeds as before, but in each new star system there are more missile bases and different obstacles. (See *Table 1-4* for a list of obstacles in each star system.)

Fireballs appear in the third star system. Fireballs are red and yellow circular shapes that appear to be burning. When shot with the laser beam, the fireball slows down. It takes four shots to destroy a fireball. In the ninth star system a master base appears. It is a white, pulsating base. The base is smart—it can sense when a laser beam is aimed at it. The master base can decrease or increase the speed of the planet or change the direction of planet rotation to avoid being destroyed!

In the eleventh star system, starballs appear. (After the tenth star system, fireballs become starballs.) Starballs are red circular shapes. A starball slows down when it is shot by a laser beam, but speeds up after the hit. It takes four shots to destroy a starball.

After the fourteenth star system, there are one more MIRV and one more starball for each new star system. (See *Table 1-5* for a list of targets and their point values.)

Table 1-4 Liberator™ Game Play

STAR SYSTEM	PLANET	OBSTACLE*
1	Earth-like	4-5 bases Bases become satellites Killer saucer
2	Earth-like	6-7 bases Bases become satellites Killer saucer MIRVs
3	Jupiter-like	8-9 bases Bases become fireballs Killer saucer
4	Jupiter-like	10-11 bases MIRVs Fireballs Killer saucer
5	Earth-like	12-13 bases Faster rotation of planet Satellites Killer saucer
6	Jupiter-like	14-15 missile bases Faster rotation of planet Fireballs
7	Earth-like	16 bases MIRVs Satellites
8	Jupiter-like	16 bases Faster rotation of planet MIRVs Fireballs
9	Earth-like	16 bases Master base MIRVs Satellites
10**	Jupiter-like	16 bases Master base MIRVs Fireballs

**Each star system has enemy spaceships, missile bases, and missiles.*

***After Star System 10, fireballs become starballs.*

Table 1-5 Liberator™ Scoring

TARGET	POINT VALUE
Enemy spaceship	50
Missile base	100
Satellite	20
Killer saucer	150
MIRV	10
Fireball	20
Starball	20

4. High-Score Mode

The High-Score Mode begins when a player has earned one of the ten highest scores. The player has one minute to record his initials. A player spins the Midi Trak-Ball™ to locate his initial. He presses FIRE to put his initial into the high-score table.

To reset the high-score table, power the game *off* and then *on*, or switch the self-test switch *on* and *off*. However, this does not erase the top three scores.

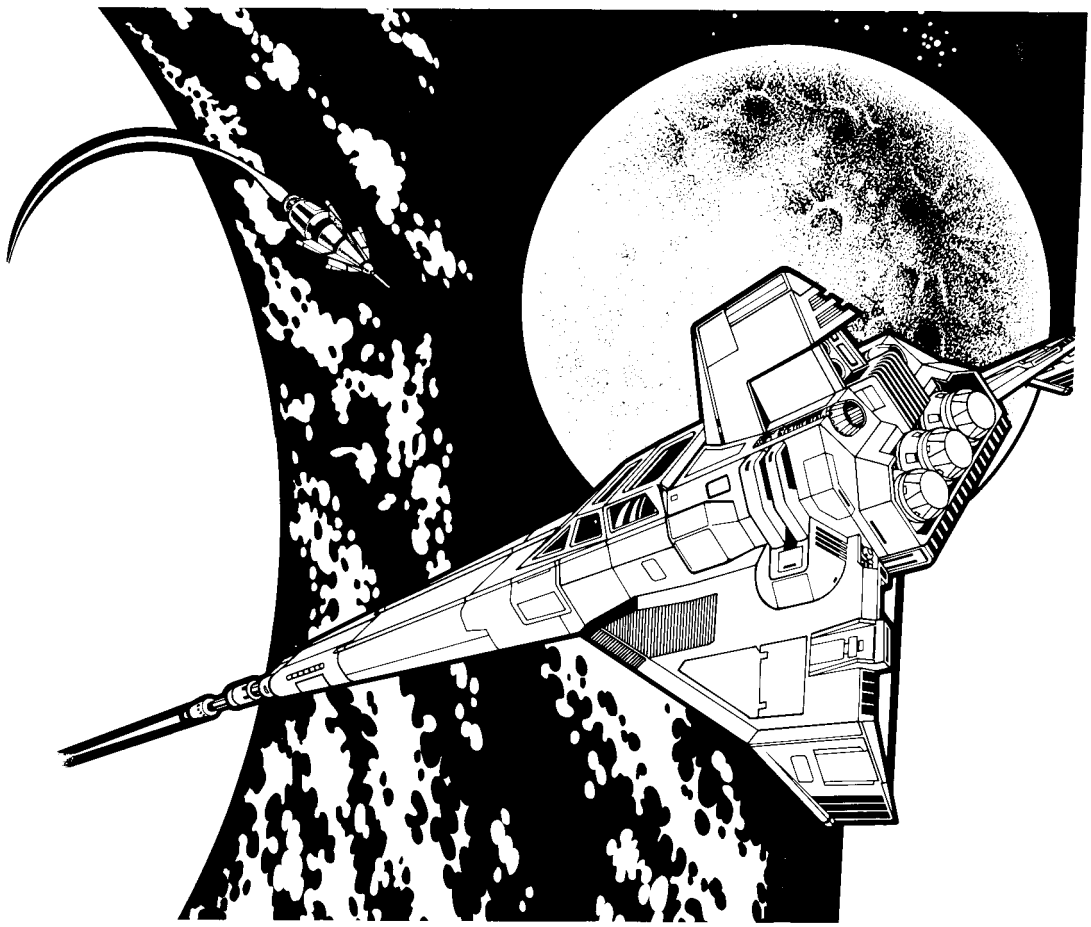
5. Hints for Game Play

- Destroy the enemy missile bases on the planet first, before they launch their missiles!
- Destroy the killer saucer as soon as it begins to grow in size and make a sound.
- Plan your shot so it explodes in front of a moving target.
- Shoot fireballs as soon as possible to slow them down.
- For fast planets, place shots in a long vertical line directly over the planet.

Self-Test Procedure

The following self-test procedures should be performed by a qualified electronic technician.

This game tests itself when the self-test switch is set to the *on* position. If there is a failure, the game produces audiovisual aids to help you find the failing portion of the game. The self-test procedure included in Chapter 1 will help you decide if the game is or is not working properly.



Chapter 2

A. Comments on Troubleshooting

When troubleshooting, first determine the symptom(s) of the failure. After determining the symptom, look over the wiring diagram and determine what assemblies could cause the failure. Could it be caused by the power supply, Regulator/Audio II PCB, or the video display?

The next step is to check all harness wires and connectors to the suspected failing assembly. If you find no harness or connector problem, substitute an assembly known to be good for the suspected failing assembly. If the game functions properly, you have successfully isolated the failure. If it doesn't, repeat the procedure with another assembly.

When you have isolated the failing assembly, you must troubleshoot that assembly and make the necessary repairs. If the video display fails, we suggest that a qualified video-display technician perform the troubleshooting and repair.

Be sure to refer to *The Book—A Guide to Electronic Game Operation and Servicing*, published by Atari, Inc., whenever you need help with the techniques, tools, and terminology associated with coin-operated electronic games.

To effectively troubleshoot a game PCB, learn as much as you can about the PCB. The diagrams in the *Schematic Package* (included with the game) show the functions of the circuitry. Again, while troubleshooting the PCB, first determine the symptom of the failure, then locate the suspected area on the schematic diagram.

A **Glossary of Game PCB Signal Names** is included in the *Schematic Package*. Each signal description states if the signal is generated by hardware or software, where it is generated, where it goes, and what it does. We suggest you use this glossary to become more familiar with the operation of the game PCB.

B. Performing the Self-Test

The following self-test procedures should only be performed by a qualified electronic technician.

This game will test itself and provide data to show that the game's circuitry and controls are operating properly. The data is provided on the video display and speaker. No additional equipment is necessary.

To switch to the Self-Test Mode, set the self-test switch, located on the utility panel, to the *on* position. Press the auxiliary coin switch, located on the utility panel next to the self-test switch, to progress through tests 1 through 4.

SCREEN 1—Test Passes:

If the test passes, the screen goes blank for a few seconds before displaying the picture below. Upright games should display the message *UPRIGHT* in the lower right corner of the screen; cocktail games should display *COCKTAIL* in the same location. You will hear a continuous low-to-high tone while the screen is blank. See *Chapter 1, Section F, Performing the Initial Self-Test* for a complete description of this picture.

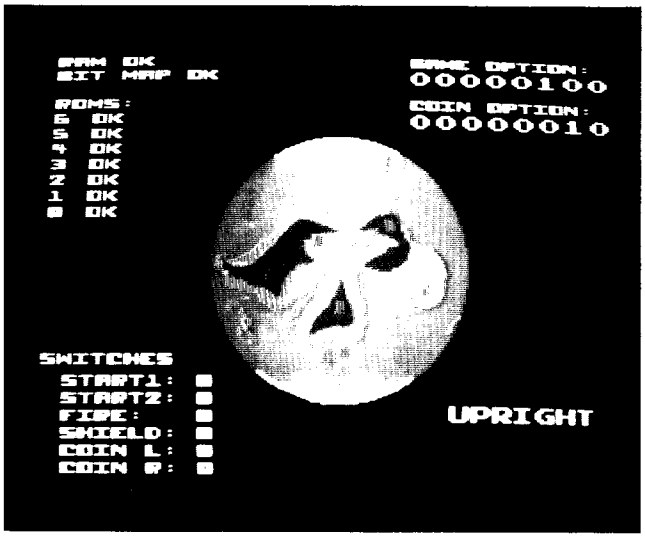


Figure 2-1 Self-Test Screen 1—Test Passes

NOTE

This procedure does not test the coin door lockout coils and coin counter. If the lockout coils do not function when the game is on, suspect the lockout coil wiring or the + 10-volt power supply. Troubleshoot using the game harness schematics. If the coin counter fails, make sure coin-counter switch 1 at T12 on the game PCB is correctly set in the *on* position. If the coin counter still fails, suspect latch T11 on the game PCB. Refer to the game schematics to troubleshoot any further problems with the coin counter.

SCREEN 1—Test Fails:

RAM failure is indicated by a blank or "garbage"-filled screen and a repeating series of eight tones. A low tone indicates a good RAM; a high tone indicates a failed RAM. The tone number and matching RAM location are listed in Table 2-1.

Table 2-1 Failing RAM Location

Tone Number	Failed RAM Location on Game PCB
1st	J10
2nd	M10
3rd	S10
4th	F10
5th	L10
6th	P10
7th	T10
8th	E10

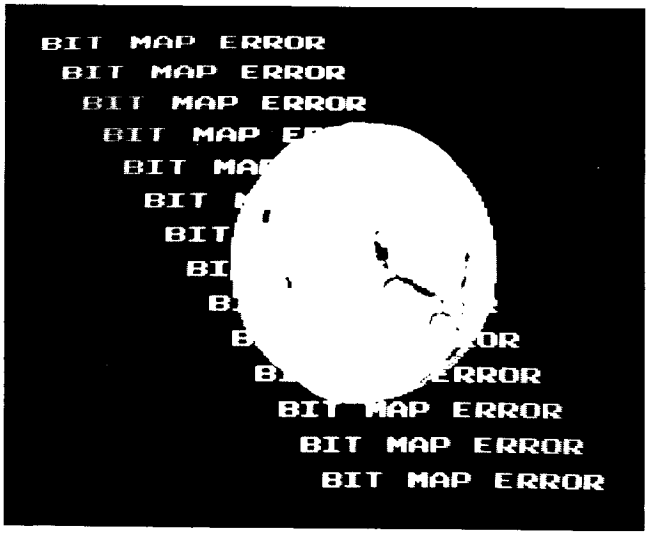


Figure 2-2 Self-Test Screen 1— Test Fails

BIT MAP RAM failure is indicated by *BIT MAP ERROR* displayed on the top center of the screen plus a repeating series of four tones (see *Figure 2-2*). A low tone indicates a good RAM; a high tone indicates a failed RAM. Bit-map tone numbers with corresponding RAM locations are listed in Table 2-2.

Table 2-2 Failing Bit Map RAM Location

Tone Number	Failed Bit Map RAM Location on Game PCB
1st	K10
2nd	N10
3rd	R10
4th	H10

ROM failure is indicated by *BAD* message and the ROM checksum displayed opposite the number of the failed ROM. (Ignore the checksum.) The failed ROM and its location are listed in Table 2-3.

Table 2-3 Failing ROM Location

Screen Display	Failed ROM Location on Game PCB
6 *	T1
5 *	R/S1
4 *	P1
3	N1
2	L/M1
1	K1
0	J1

*This ROM contains the Self-Test program. If this ROM fails, the screen will be blank or will display "garbage."

SWITCH failure is indicated by the corresponding *0* not changing to a *1* on the screen when the switch is pressed. Troubleshoot using the information in *Chapter 3, Section B,* and the game schematics.

SOUND failure is indicated by the absence of any sound when any of the control panel pushbuttons or game switches are pressed. Inspect the volume controls on the utility panel, or troubleshoot using the game schematics.

MIDI TRAK-BALL™ failure is indicated by no movement or jerky movement of the cursor when the Midi Trak-Ball is rolled. If the cursor fails to move, or if movement is reversed or jerky, inspect the Midi Trak-Ball connections (see *Chapter 3, Section B*).

PLANET failure is indicated in several ways:

- If the planet fails to appear, fails to rotate, or if the missile bases fail to flash, refer to the schematics.
- If the Earth-like planet fails to appear, suspect ROMs M/N8 or T8.
- If the Jupiter-like planet fails to appear, suspect ROMs P8 or R/S8.
- If either planet has horizontal bars of color, suspect ROM S7.
- If either planet has vertically jumping blocks of color, suspect ROM T7.
- If horizontal segments of either planet are uneven during rotation, suspect ROMs N6 and P6.

To see the remaining self-test screens (2, 3, and 4), press the auxiliary coin switch on the utility panel to advance to each screen.

SCREEN 2:

EAROM or CUSTOM I/O CHIP failure is indicated by *CLEARING ENTIRE EAROM* message in the top center of the screen (see *Figure 2-3*). If the program confirms a failed ROM after clearing, *EAROM BAD* message appears in the top center of the screen. If replacing the EAROM does not correct the failure, refer to the schematics.

To erase average game score and time, press both FIRE and 1-player start pushbuttons at the same time. Release the pushbuttons. **Wait** until the purple message *CLEARING BOOKKEEPING DATA* disappears before continuing with other tests.

To erase the entire EAROM, press all four player pushbuttons at the same time. Release the pushbuttons. **Wait** until the purple message *CLEARING ENTIRE EAROM* disappears before continuing with other tests.

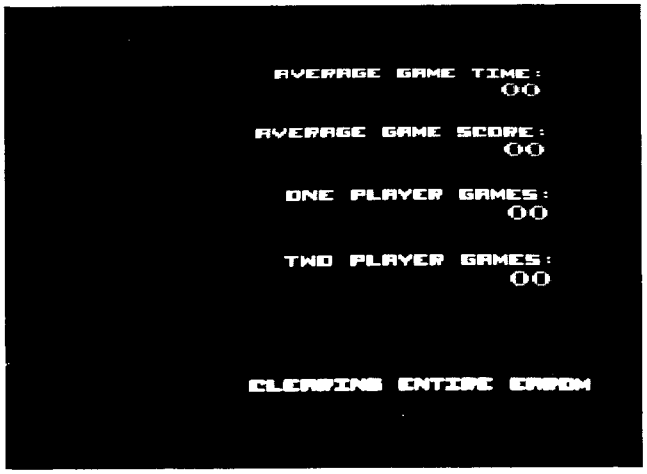


Figure 2-3 Self-Test Screen 2

SCREEN 3:

This screen shows the intensities of red, green, and blue (see *Figure 2-4*). Refer to the color-raster display manual for the next two adjustments. Adjust the levels of each color so that the darkest intensity is just slightly visible from black. Use this pattern for tracking adjustments.

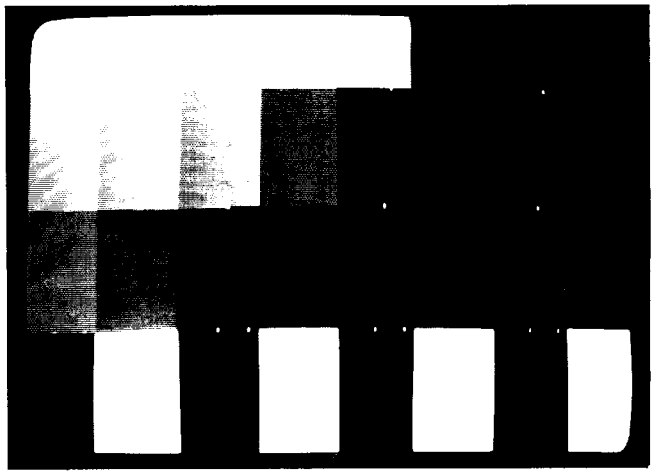


Figure 2-4 Self-Test Screen 3

SCREEN 4:

A grid pattern framed in red and green appears on the screen (see *Figure 2-5*). The corners of the green frame must be visible at all times; the corners of the red frame may or may not be visible. The corners of the display should cut across the blue boxes located in the corners of the convergence display between the red and green frames (refer to the color-raster display manual).

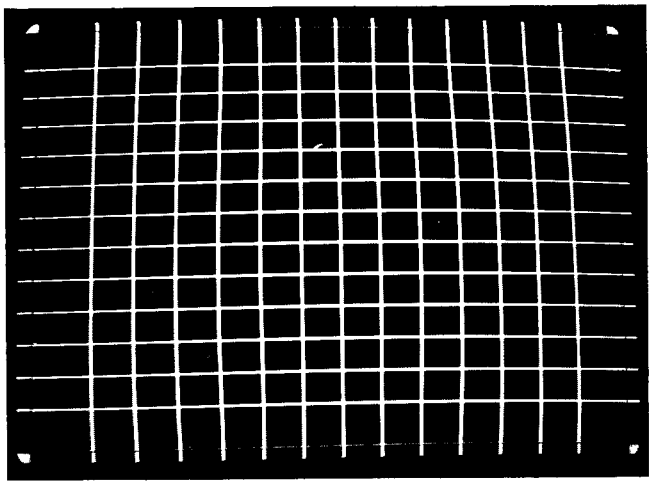
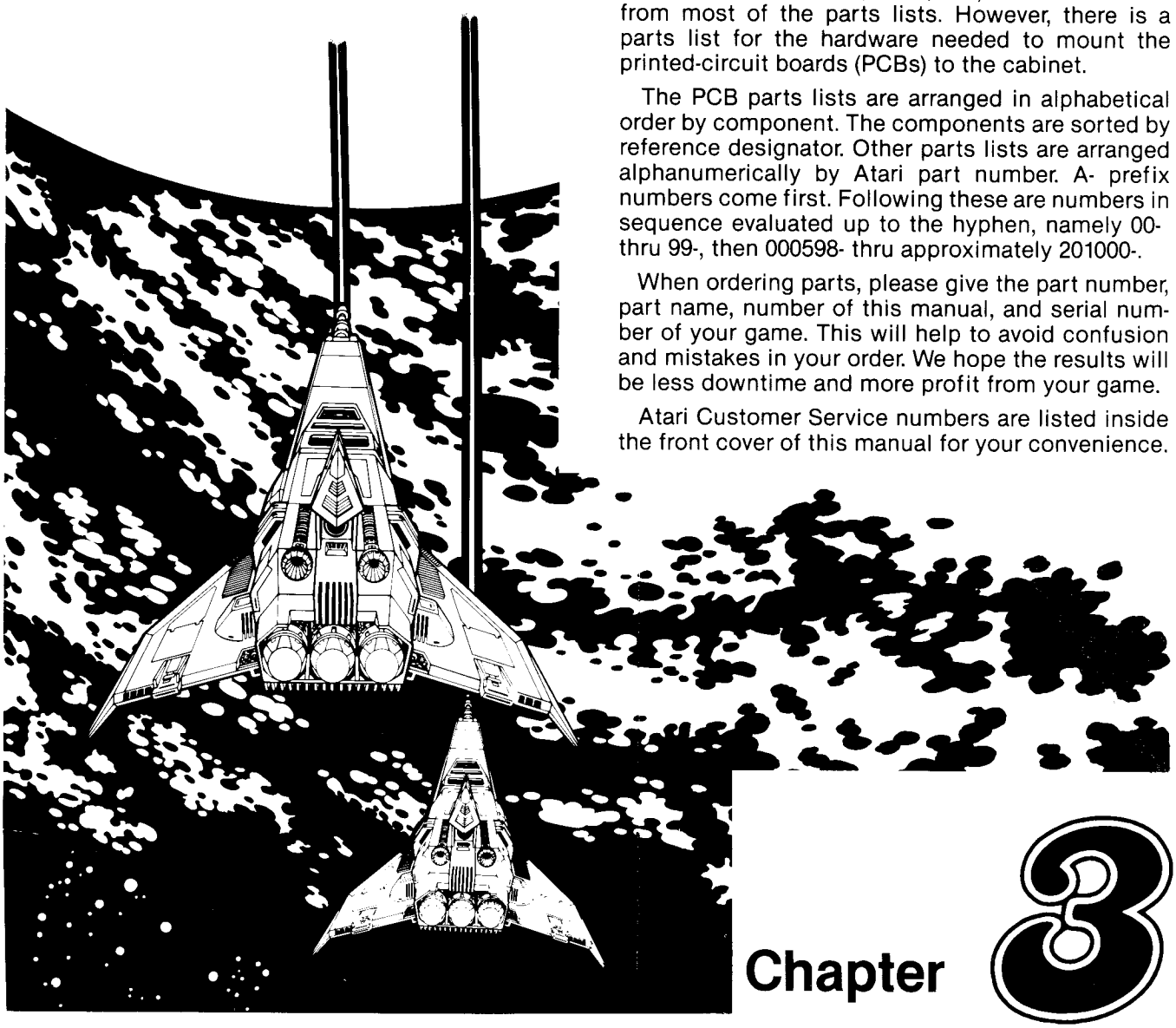


Figure 2-5 Self-Test Screen 4

Maintenance, Repair, and Parts



This chapter details maintenance and repair information and provides information you need to order parts for your Liberator™ game. **Common hardware** (screws, nuts, washers, bolts, etc.) has been deleted from most of the parts lists. However, there is a parts list for the hardware needed to mount the printed-circuit boards (PCBs) to the cabinet.

The PCB parts lists are arranged in alphabetical order by component. The components are sorted by reference designator. Other parts lists are arranged alphanumerically by Atari part number. A- prefix numbers come first. Following these are numbers in sequence evaluated up to the hyphen, namely 00- thru 99-, then 000598- thru approximately 201000-.

When ordering parts, please give the part number, part name, number of this manual, and serial number of your game. This will help to avoid confusion and mistakes in your order. We hope the results will be less downtime and more profit from your game.

Atari Customer Service numbers are listed inside the front cover of this manual for your convenience.

Chapter 3

A. Cabinet-Mounted Assemblies

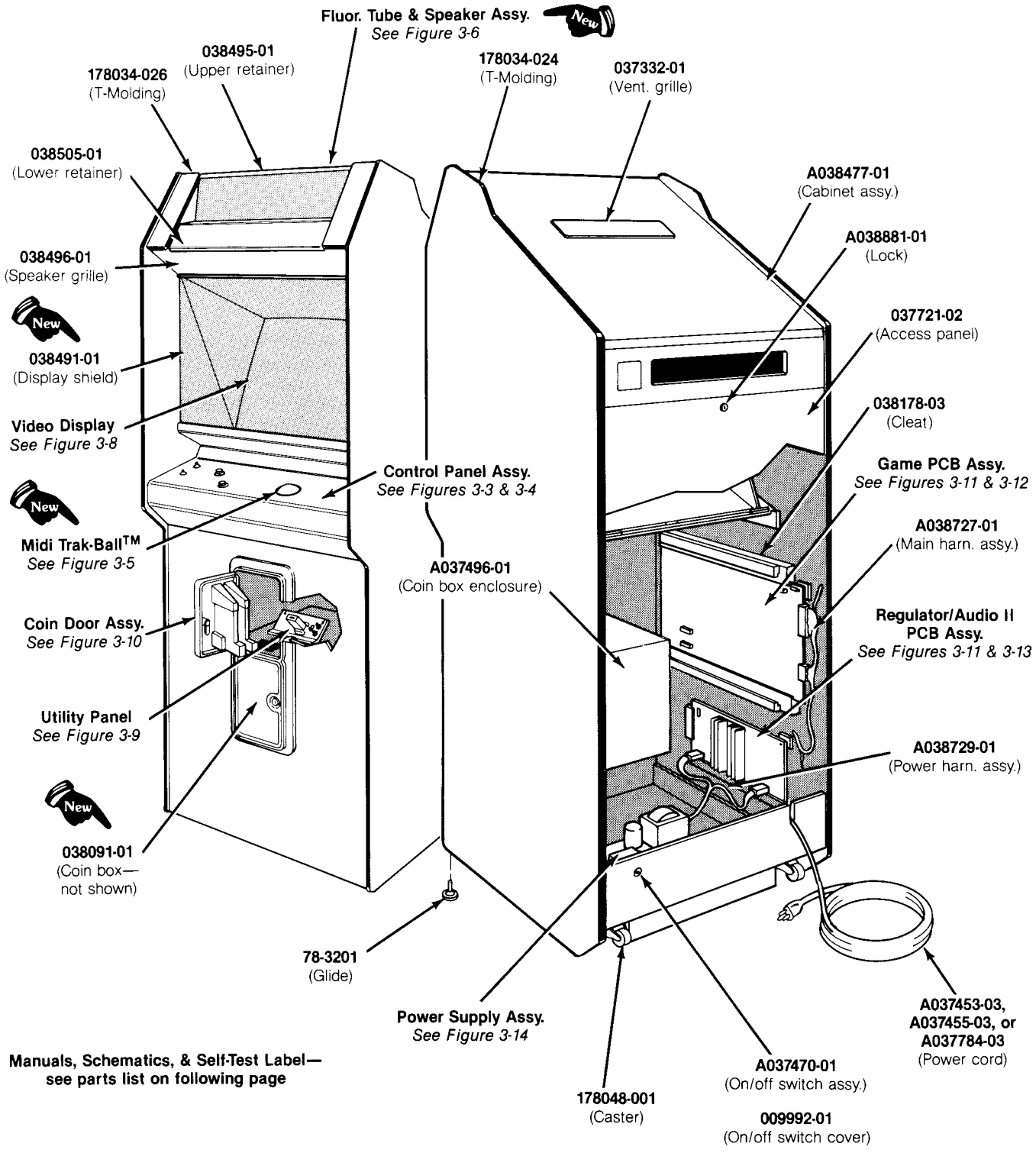


Figure 3-1 Cabinet-Mounted Assemblies
Upright Cabinet A038476-01 A

Cabinet-Mounted Assemblies
Upright Cabinet
Parts List

Part No.	*Description*
A037453-03	Strain-Relief Power Cord *(U.S. and Canada)*
A037455-03	Strain-Relief Power Cord *(Australia and New Zealand)*
A037470-01	Power On/Off Switch/Mounting Plate Assembly
A037496-01	Metal Coin Box Enclosure
A037784-03	Strain-Relief Power Cord *(United Kingdom, Ireland, Lebanon, Saudi Arabia, India, Hong Kong, Singapore, Egypt, Nigeria, Republic of South Africa, Zimbabwe)*
A038477-01	Cabinet Assembly *(includes glides and PCB retainers, but not the rear access panel)*
A038727-01	Main Harness Assembly
A038729-01	Power Harness Assembly
A038881-01	Lock Assembly *(for rear access panel) Acceptable substitute is part no. A038881-03*
	The following six items are the technical information supplements to this game:
SP-209	Liberator Schematic Package
ST-209-01	Liberator Label with Self-Test Procedure and Option Switch Settings
TM-160	Service Manual for 19-Inch Electrohome Color Raster-Scan Display *(use with part no. 92-049)*
TM-201	Service Manual for 19-Inch Wells-Gardner Color Raster-Scan Display *(use with part no. 92-055)*
TM-209	Liberator Operation, Maintenance, and Service Manual
TM-220	Service Manual for 19-Inch Matsushita Color Raster-Scan Display *(use with part no. 139003-1004)*
78-3201	Adjustable Glide
009992-01	On/Off Switch Cover
037332-01	Ventilation Grille
037721-02	Rear Access Panel *(does not include lock)*
038091-01	Molded Coin Box *(not shown)*
038178-03	Dual-slotted PCB cleat
038491-01	Video Display Shield
038495-01	Upper Retainer
038496-01	Speaker Grille
038505-01	Lower Retainer
178013-001	Spring Draw Latch *(not shown)*
178034-024	¾-Inch Black Plastic T-Molding
178034-026	13/16-Inch Black Plastic T-Molding
178048-001	2-Inch Rigid Caster

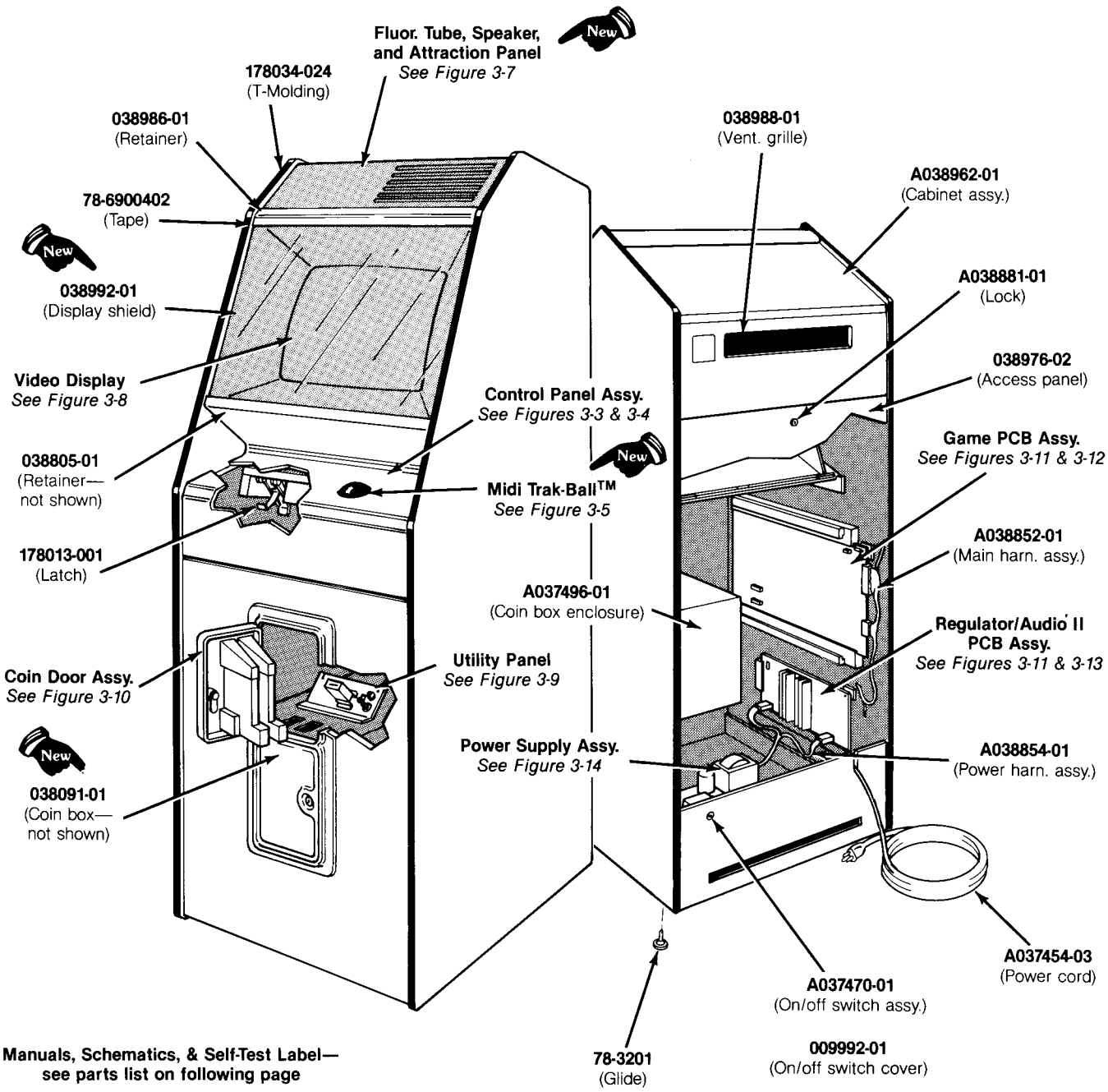


Figure 3-2 Cabinet-Mounted Assemblies
Ireland-Built Cabinet A038961-01 & -02 A

Cabinet-Mounted Assemblies
Ireland-Built Cabinet
Parts List

Part No.	*Description*
A037454-03	Strain-Relief Power Cord *(Austria, Belgium, Chile, Denmark, Finland, France, Germany, Greece, Indonesia, Italy, Netherlands, Norway, Spain, Sweden, and Uruguay)*
A037470-01	Power On/Off Switch/Mounting Plate Assembly
A037496-01	Metal Coin Box Enclosure
A038852-01	Main Harness Assembly
A038854-01	Power Harness Assembly
A038881-01	Lock Assembly *(for rear access panel)*
A038962-01	Cabinet Assembly *(includes glides and PCB retainers, but not the rear access panel)*
	The following six items are the technical information supplements to this game:
SP-209	Liberator Schematic Package
ST-209-01	Liberator Label with Self-Test Procedure and Option Switch Settings
TM-160	Service Manual for 19-Inch Electrohome Color Raster-Scan Display *(use with part no. 92-049)*
TM-201	Service Manual for 19-Inch Wells-Gardner Color Raster-Scan Display *(use with part no. 92-055)*
TM-209	Liberator Operation, Maintenance, and Service Manual
TM-220	Service Manual for 19-Inch Matsushita Color Raster-Scan Display *(use with part no. 139003-1004)*
78-3201	Adjustable Glide
78-6900402	Vinyl Foam Single-Coated Adhesive Tape, ¼-Inch Wide x ⅛-Inch Thick
009992-01	On/Off Switch Cover
038091-01	Molded Coin Box *(not shown)*
038805-01	Display Shield Retainer *(not shown)*
038976-02	Rear Access Panel *(does not include lock)*
038986-01	Attraction Panel Retainer
038988-01	Ventilation Grille
038992-01	Display Shield
178013-002	Spring Draw Latch
178034-024	¾-Inch Black Plastic T-Molding

B. The Control Panel

WARNING

Before you remove or repair any switch on the control panel, **switch the game to *off*.**

Opening the Control Panel:

1. Unlock and open the coin door (see *Figure 3-3*). Reach up through the opening to the top of the control panel and release the spring-draw latches. For the *Ireland-Built* cabinet, remove the two button-head screws that secure the panel to the lower retainer.
2. Close the coin door.
3. Lift the control panel at the top edge and tilt it toward you. The control panel on the *Upright* cabinet has foam tape on the inside edges. Make sure the tape is in good condition.

Repairing the Leaf Switches:

1. Adjust the leaf switches for a narrow gap. When a switch button is pressed, the resulting wiping action of the cross-bar contacts provides a self-cleaning feature. **Do not burnish the contacts.** To clean them, use electrical contact cleaner.
2. To remove a leaf switch, disconnect the wires and remove the screw with a Phillips-head screwdriver.
3. To remove the switch button, turn the nut with a wrench in a counterclockwise direction from inside the control panel. The ring on the outside of the control panel should not spin.
4. Replace the switch, reconnect the harness wires as shown in the *Schematic Package, Game Wiring Diagram.* Make sure the colored wires are routed to their matching colored tabs on the switch.

Repairing the LED Start Switches:

These switches have a very low failure rate. If you suspect switch failure, test it using the following directions.

Testing the LED Switch:

1. Disconnect the wires from the switch.
2. Attach the leads of an ohmmeter to the normally open and common contacts.
3. Check the contacts (push and release the switch button) for closed and open continuity.
4. If the contacts do not operate sharply or always remain closed or open, replace the switch.

Replacing the LED Switch:

1. Disconnect the wires from the switch.
2. Turn the switch counterclockwise while holding the black cone shaped bushing on the outside of the control panel.
3. Install a new switch using the reverse procedure.
4. Reconnect the wires as shown in *Figure 3-3.*

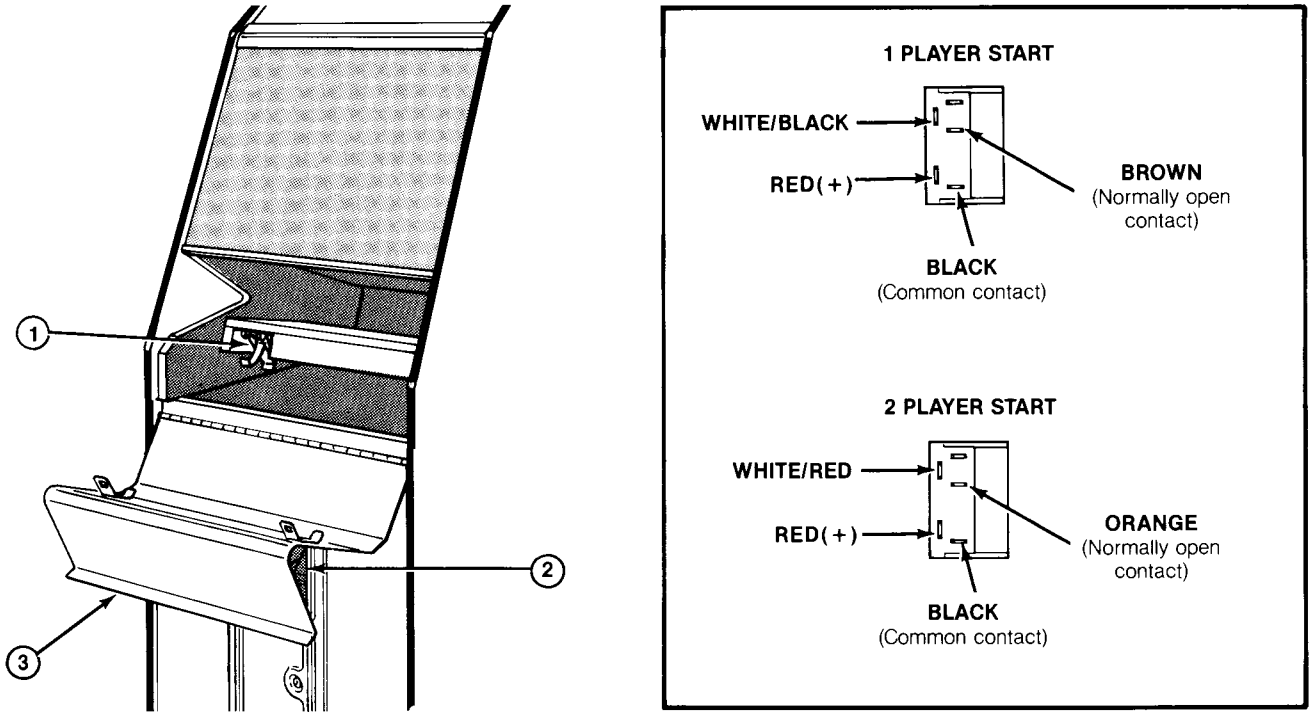


Figure 3-3 Control Panel

WARNING

Players may receive an electric shock if this control panel is not properly grounded! After servicing any parts on the panel, make sure that the ground wire is firmly attached to the metal tab on the inside of the control panel.

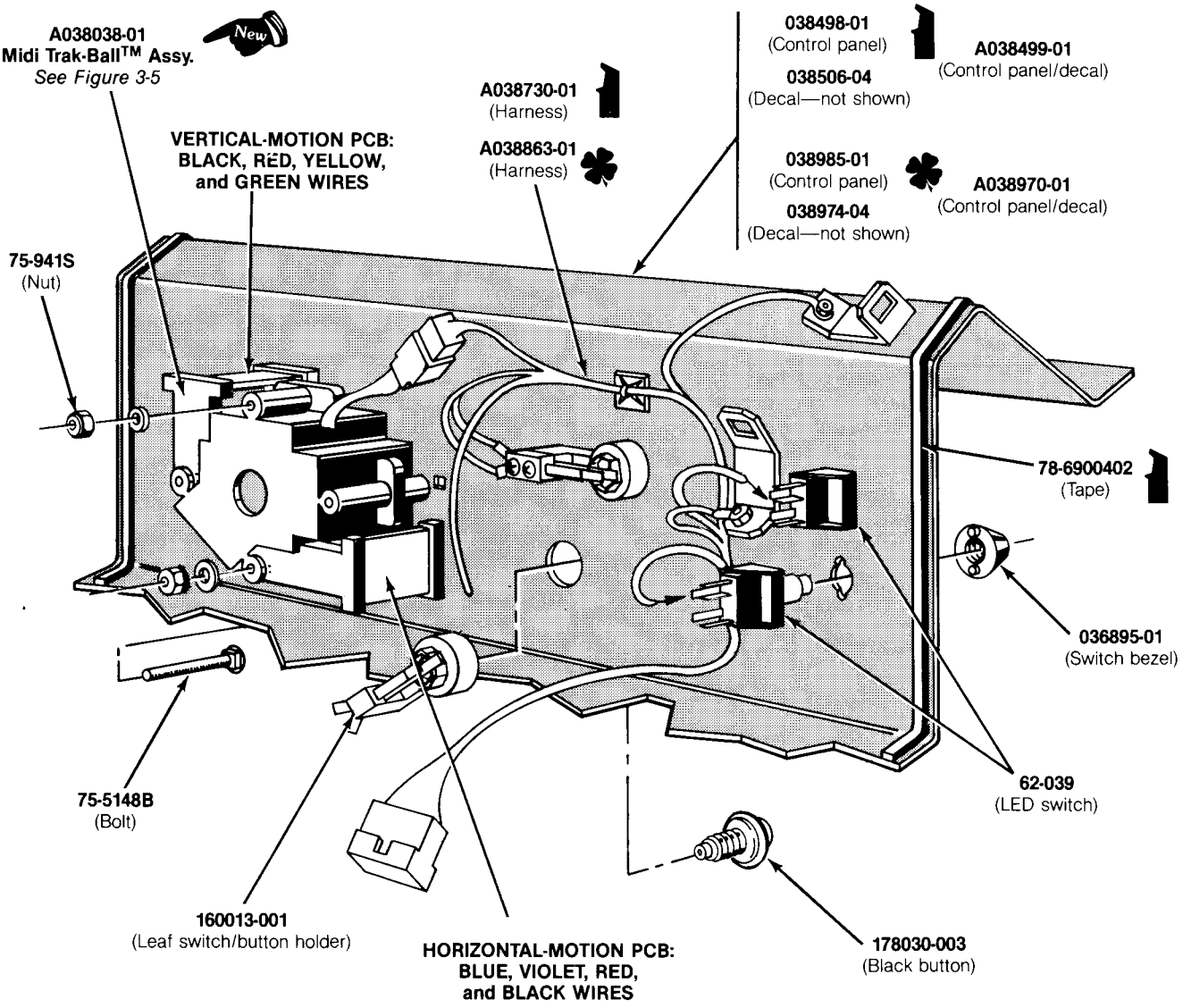


Figure 3-4 Control Panel Assembly
Upright Cabinet A038500-01 A
Ireland-Built Cabinet A038969-01 A

Control Panel Assembly
Parts List

Part No.	*Description*
	Upright Cabinet
A038499-01	Control Panel with Decal
A038730-01	Control Panel Harness Assembly
78-6900402	Vinyl Foam Single-Coated Adhesive Tape, ¼-Inch Wide x ⅛-Inch Thick *(24 in. required)*
038498-01	Control Panel
038506-04	Control Panel Decal
	Ireland-Built Cabinet
A038863-01	Control Panel Harness Assembly
A038970-01	Control Panel with Decal
038974-04	Control Panel Decal
038985-01	Control Panel
	Upright and Ireland-Built Cabinets
A038038-01	Midi Trak-Ball™ Assembly
62-039	SPDT Momentary Pushbutton Start Switch with Red Light-Emitting Diode
75-941S	#10-24 Self-Locking Nut
75-5148B	#10-24 Black Carriage Bolt
036895-01	Black Molded Switch Bezel
160013-001	Leaf Switch and Button Holder *(leaf switch only is part no. 160012-001)*
178030-003	Black Pushbutton Assembly

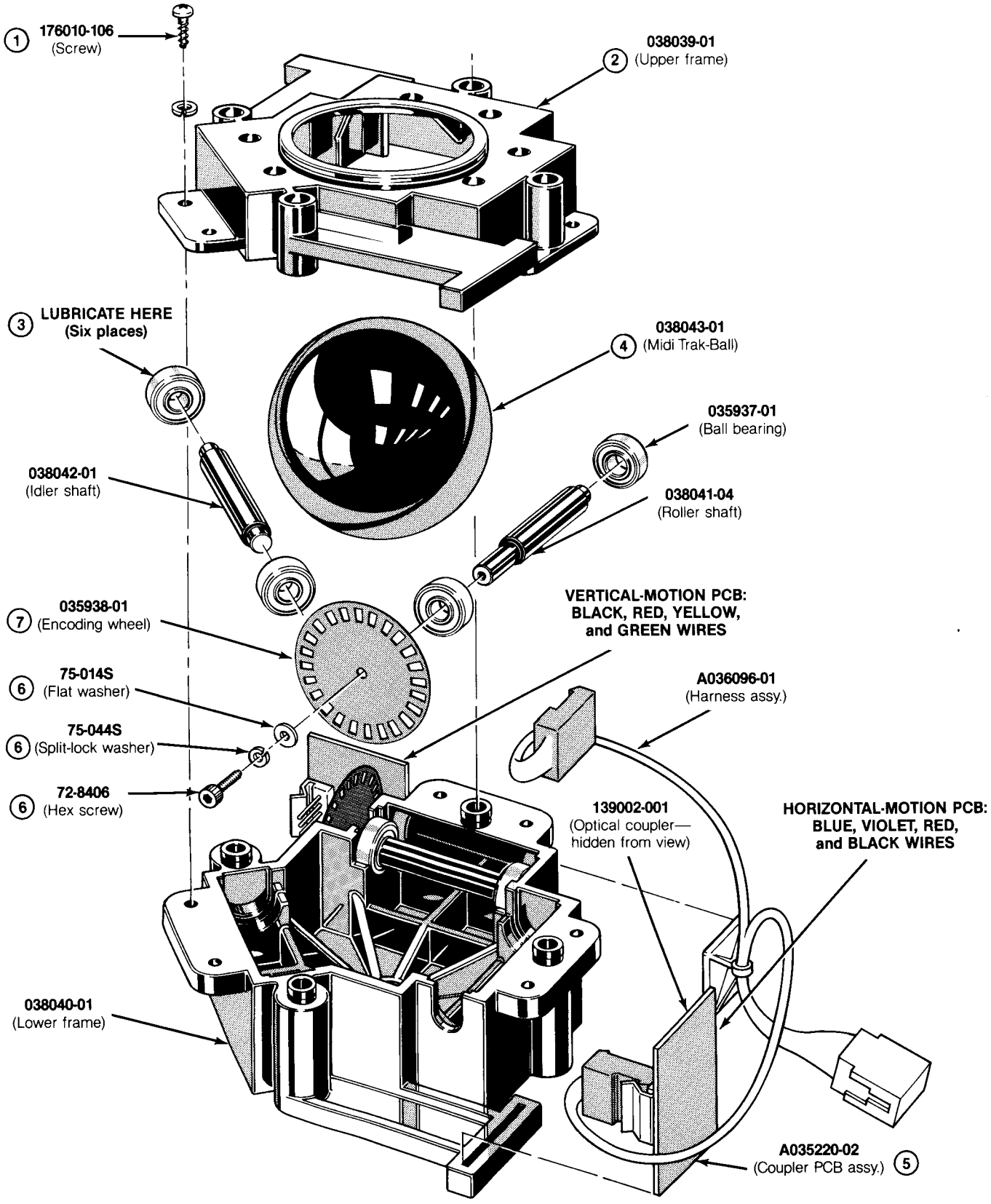


Figure 3-5 Midi Trak-Ball™ Assembly A038038-01 A

WARNING

Prior to removing or repairing the Midi Trak-Ball, **switch the game to *off*.**

Lubricating the Midi Trak-Ball™:

1. Remove the entire Midi Trak-Ball assembly from the control panel (see *Figure 3-4*). Remove the six screws that secure the upper and lower frames together (see *Figure 3-5*).
2. Lift off the top frame.
3. Lubricate each of the six ball bearings with two drops of 3 in-One® oil. Lubricate approximately every three months or 6,000 credits (credits are counted on the coin counter).

Removing the Midi Trak-Ball, Coupler PCB and Encoding Wheel:

4. Follow steps 1 through 3. Then remove the Midi Trak-Ball.
5. Lift the PCB out of its slot. Carefully disconnect the red connector and remove the PCB.
6. Remove the socket-head screw, flat washer, and split-lock washer that secure the encoding wheel.
7. Remove the encoding wheel.
8. Reassemble and reinstall in reverse order.

NOTE

When you replace the PCB, make sure that the metal encoding wheel is not bent or damaged. It should turn freely between the two halves of the radial optical coupler.

Adjusting the Midi Trak-Ball control:

9. When you tighten the encoding wheel, rotate the socket-head screw on the end of the roller shaft until a hole in the shaft is visible through the hole in the top of the frame.
10. Insert a $\frac{3}{10}$-inch diameter pin or screwdriver through the hole in the shaft.
11. Tighten the socket-head screw with an Allen wrench.

Circled numbers match numbered instructions. Disassemble in the order indicated.

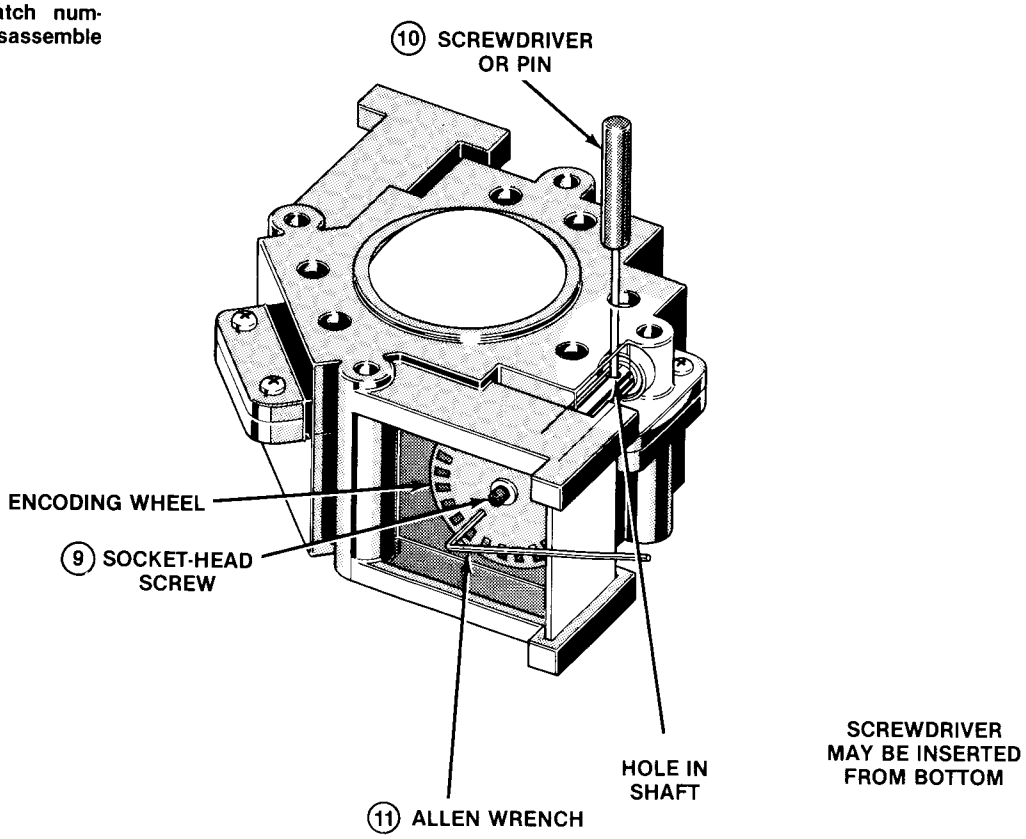
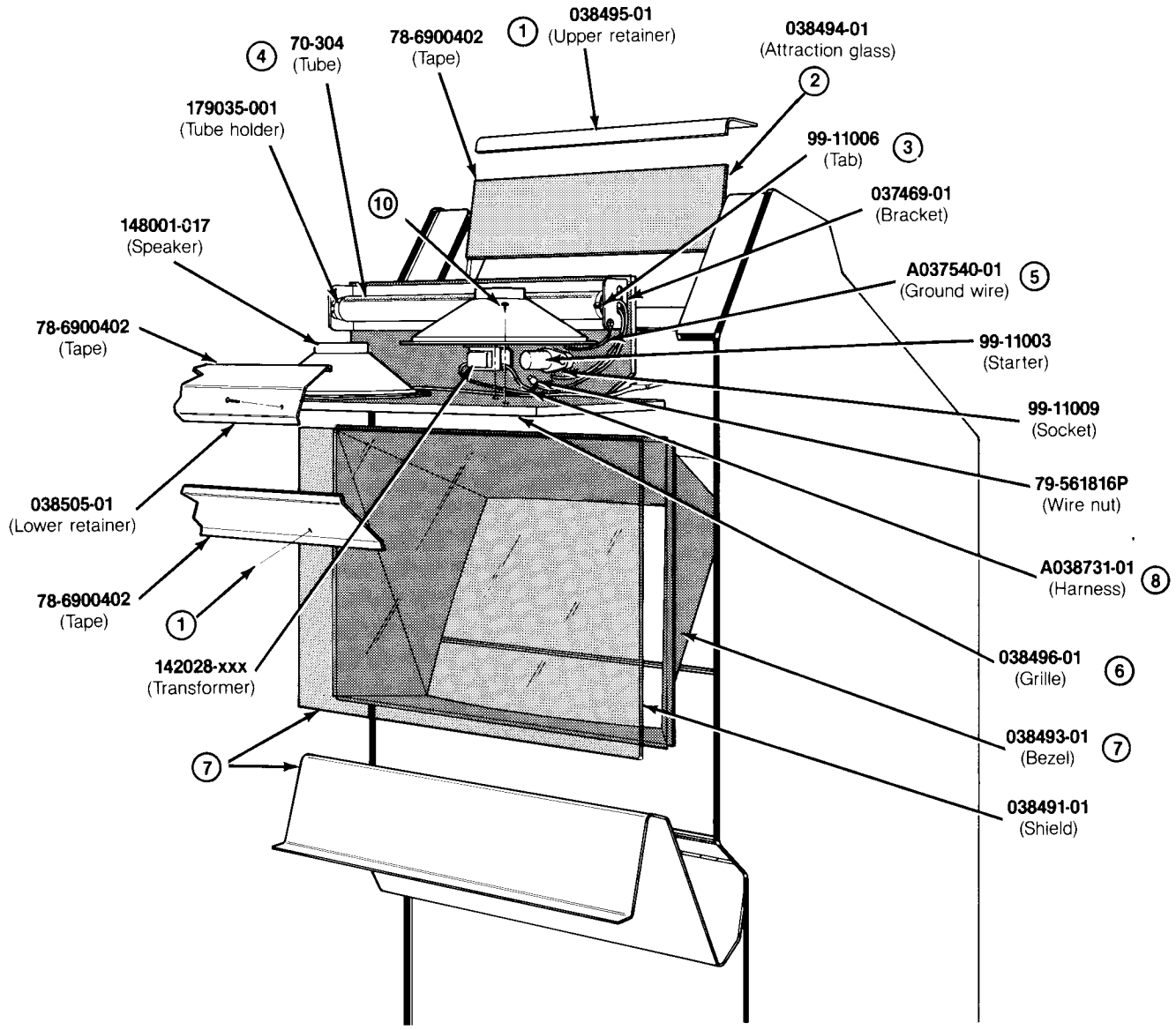


Figure 3-5 Midi Trak-Ball Assembly, continued

Midi Trak-Ball™ Assembly
Parts List

Part No.	*Description*
A035220-02	Coupler PCB Assembly *(includes Radial Optical Coupler)*
A036096-01	Harness Assembly
72-8406	#4-40 x ⅜-Inch, Hex Socket-Head Steel Machine Screw
75-014S	#4 Flat SAE-Standard, Zinc-Plated Steel Washer
75-044S	#4 Split-Lock, Zinc-Plated Steel Washer
034168-01	Label with Lubrication Instructions *(not shown)*
035937-01	Ball Bearing *(6 per assembly)*
035938-01	Etched Encoding Wheel
038039-01	Upper Black Plastic Frame
038040-01	Lower Black Plastic Frame
038041-01	Roller Shaft
038042-01	Idler Shaft
038043-01	Midi Trak-Ball *(3-inch diameter)*
139002-001	Radial Optical Coupler *(located on the Coupler PCB Assembly)*
176010-106	#8 x ⅜-Inch Cross-Recessed, Pan-Head, Zinc-Plated Steel Screw

C. Fluorescent Tube and Speaker



Circled numbers match numbered instructions. Disassemble in the order indicated.

NOTE

To make sure that the fluorescent tube starts, check that the ground wire is firmly attached to both the ballast transformer and the steel lamp bracket.

Figure 3-6 Fluorescent Tube and Speaker Upright Cabinet A038504-01 & -02 A

WARNING

Before you remove or repair the fluorescent tube or speaker, **switch the the game to *off.***

If you drop a fluorescent tube and it breaks, *it will implode!* Shattered glass can fly six feet or more from the implosion. Use care when replacing any fluorescent tube.

Upright Cabinet

Replacing the Fluorescent Tube:

1. Remove the three screws and lock washers that secure the upper attraction-panel retainer to the cabinet. *Loosen* the two screws that secure the lower retainer to the cabinet.
2. Lift the attraction glass up and out of the lower retainer.
3. Remove the cardboard locking tab at each end of the tube. Slightly rotate the tube up or down and carefully remove it from the lampholders.
4. Replace it with a new tube. Do not snap in the tube vigorously—*you may break it, causing an implosion!* Replace the locking tabs.
5. Check that the green ground wire is securely attached to the large metal bracket and the ballast transformer on the wood panel. If the tube is not grounded, it may not start.

Upright Cabinet

Replacing the Speakers:

6. Perform steps 1 and 2. Remove the speaker grille.
7. Open the control panel, and remove the display glass and display bezel.
8. Disconnect the 5-pin fluorescent tube and speaker harness connector.
9. Remove three screws that secure the tube and speaker board to the cabinet. Hold the board **securely** with one hand and remove the fourth screw. Remove the board.
10. Disconnect the two plug-in connectors on the speaker. Note that the white wire (+) connects on the side marked with a painted dot. Remove the screws that attach the speaker to the board. Replace the speaker and reinstall the tube and speaker board. Be sure that the tube and speaker board is flush with the upper front panel when you secure the board to the cabinet. Reassemble in reverse order.

Fluorescent Tube and Speaker Upright Cabinet Parts List

Part No.	*Description*
A037540-01	Ground Wire with Ring Lug
A038731-01	Tube and Speaker Harness Assembly
70-304	18-Inch, 15 W, Cool White Fluorescent Tube
78-6900402	Vinyl Foam Single-Coated Adhesive Tape, ¼-Inch Wide x ⅛-Inch Thick
79-561816P	Spring-Connector Wire Nut for 16- to 18-Gauge Wires
99-11003	Fluorescent Tube Starter
99-11006	Fluorescent Tube Locking Tab *(tab consists of two pieces)*
99-11009	Starter Socket
037469-01	Steel Tube Bracket
038491-01	Video Display Shield
038493-01	Video Display Bezel
038494-01	Attraction Glass with Graphics
038495-01	Upper Attraction Glass Retainer
038496-01	Speaker Grille
038505-01	Lower Attraction Glass Retainer
148001-017	6 x 9-Inch Oval, 8 Ω, 6-Ounce, Shielded High-Fidelity Speaker
142028-001	60 Hz, 118 V, Ballast Transformer *(used on A038504-01 assembly)*
142028-002	50 Hz, 118 V, Ballast Transformer *(used on A038504-02 assembly)*
179035-001	2-Pin Fluorescent Tube Holder

WARNING

Before you remove or repair the fluorescent tube or speaker, **switch the the game to *off*.**

If you drop a fluorescent tube and it breaks, *it will implode!* Shattered glass can fly six feet or more from the implosion. Use care when replacing any fluorescent tube.

Ireland-Built Cabinet

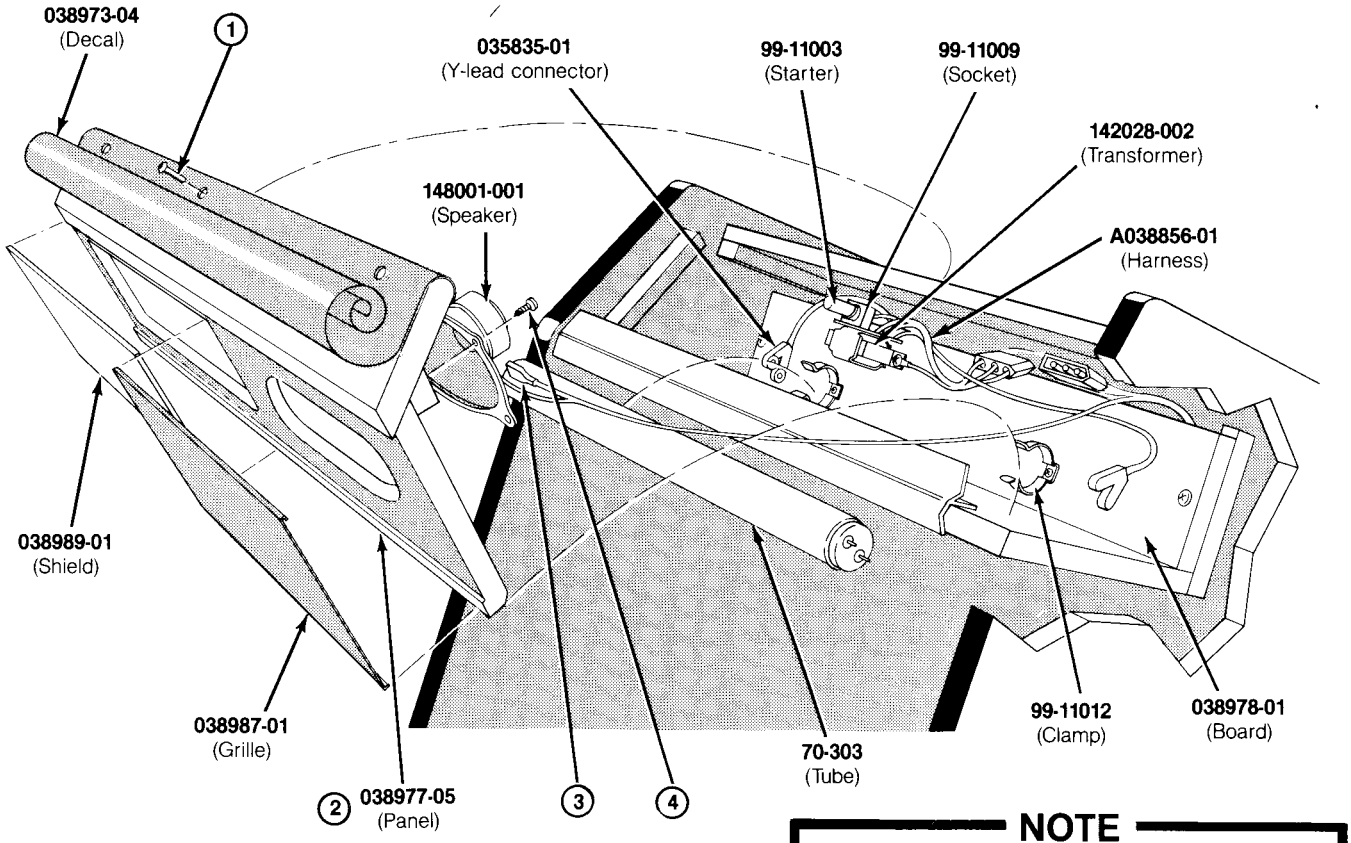
Replacing the Speaker:

1. Remove the three screws that secure the top of the attraction panel to the cabinet.
2. Grasp the panel at the top edge and pull it forward (be careful not to damage the speaker that is attached under the grille). Lift the panel up and out of the cabinet. Lay the panel on the top of the cabinet.
3. Disconnect the two speaker connectors. Note that the white wire (+) connects on the side of the speaker marked with a painted dot.
4. Remove the screws that attach the speaker to the board. Replace the speaker. Reassemble in reverse order.

Ireland-Built Cabinet

Replacing the Fluorescent Tube:

5. Perform steps 1 and 2. Remove the Y-lead connectors at each end of the tube.
6. Replace with a new tube. Do not snap in the tube vigorously—*you may break it, causing an implosion!* Replace the Y-lead connectors.
7. Reassemble in reverse order.



Circled numbers match numbered instructions. Disassemble in the order indicated.

NOTE

To make sure that the fluorescent tube starts, check that the ground wire is firmly attached to the ballast transformer.

Figure 3-7 Fluorescent Tube, Speaker, and Attraction Panel Ireland-Built Cabinet

Fluorescent Tube, Speaker, and Attraction Panel
Ireland-Built Cabinet
Parts List

Part No.	*Description*
A038856-01	Tube and Speaker Harness Assembly
70-303	18-Inch, 15-W, Cool White Fluorescent Tube
99-11003	Fluorescent Tube Starter
99-11009	Starter Socket
99-11012	1 ⅛-Inch Fluorescent Tube Clamp
035835-01	12-Inch Y-Lead Connector
038973-04	Attraction Panel Decal
038977-05	Speaker/Attraction Panel
038978-01	Fluorescent Tube Board
038987-01	Speaker/Attraction Panel Grille
038989-01	Attraction Panel Shield *(does not include decal)*
142028-002	50 Hz, 118 V, Ballast Transformer
148001-001	6 x 9-Inch Oval, 4 Ω, 6-Ounce, Shielded High-Fidelity Speaker

D. Video Display

WARNING

SHOCK HAZARD

The following procedure should only be performed by a *qualified service technician.* Before removing or repairing the video display, **switch the game to *off.*** As an extra precaution, we highly recommend you **discharge the high voltage** from the picture tube.

High voltages may exist in any video display, even with power disconnected. Use extreme caution and do not touch electrical parts of the display yoke area with your hands or with metal objects in your hands!

IMPLOSION HAZARD

If you drop the display and the picture tube breaks, *it will implode!* Shattered glass and the yoke can fly six feet or more from the implosion. Use care when replacing any display.

Upright Cabinet

Removing the Video Display:

1. From the back of the cabinet, open the rear access panel. Unplug the display harness connectors and disconnect the ground wire (see *Figure 3-8*). Remove the hardware that secures the display chassis to the wood display shelf.
2. From the front of the cabinet, loosen the screws on the lower retainer. Remove the three screws that secure the speaker grille to the cabinet and remove the grille (see *Figure 3-6*).
3. Open the control panel and remove the display shield (see *Figure 3-6*).
4. Remove the cardboard bezel.
5. Carefully remove the display through the front of the cabinet. Place it on a soft mat in a protected location. After servicing the display, reinstall it in reverse order.

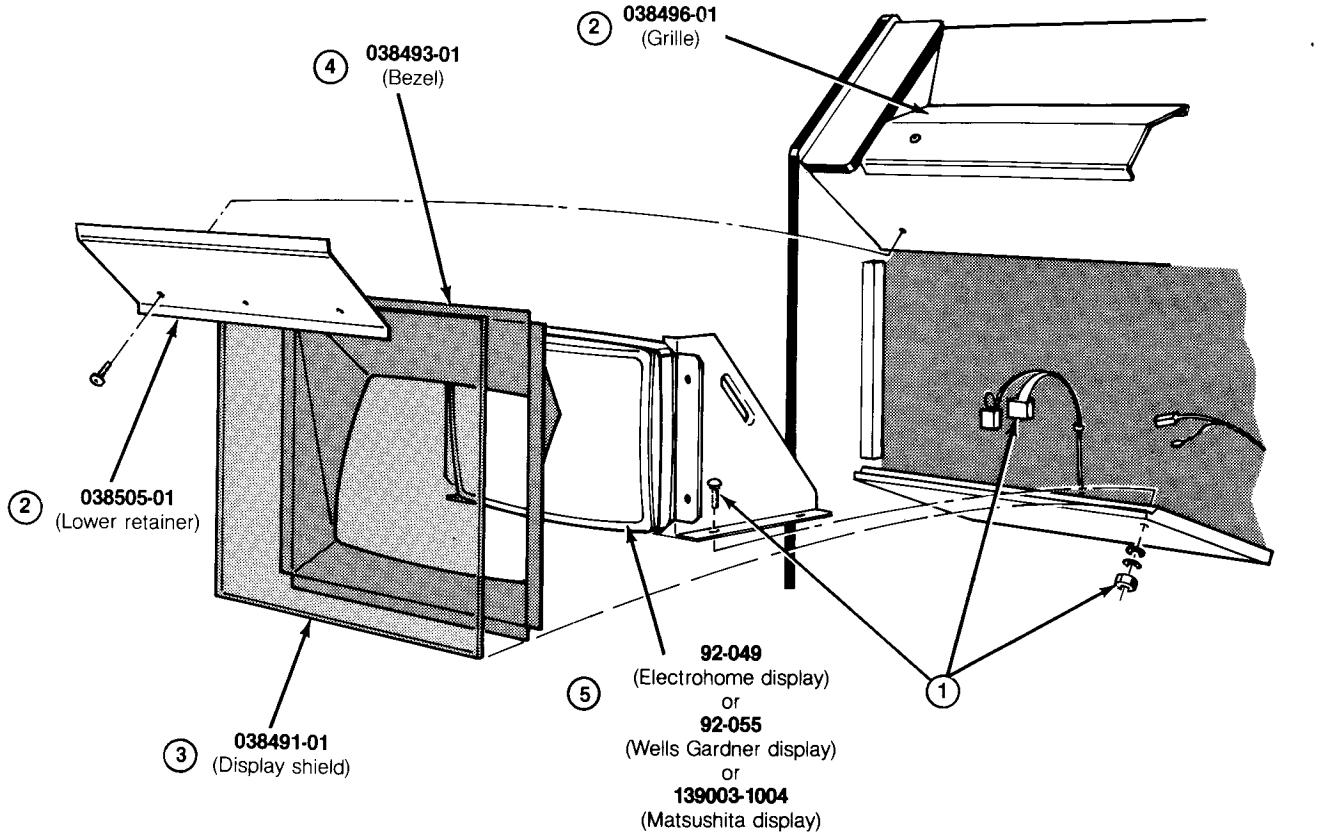


Figure 3-8 Video Display
Upright Cabinet

WARNING

SHOCK HAZARD

The following procedure should only be performed by a *qualified service technician.* Before removing or repairing the video display, **switch the game to *off.*** As an extra precaution, we highly recommend you **discharge the high voltage** from the picture tube.

High voltages may exist in any video display, even with power disconnected. Use extreme caution and do not touch electrical parts of the display yoke area with your hands or with metal objects in your hands!

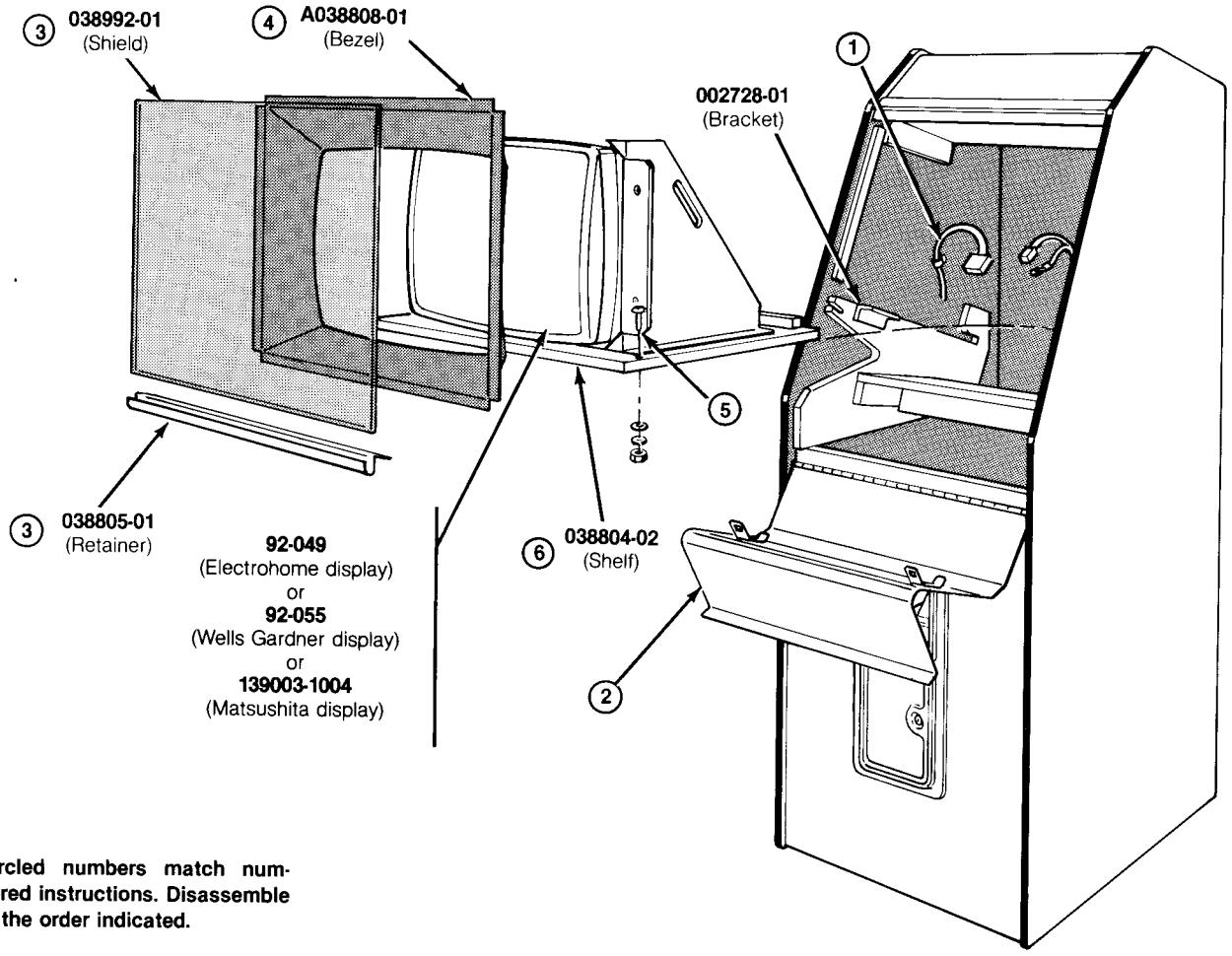
IMPLOSION HAZARD

If you drop the display and the picture tube breaks, *it will implode!* Shattered glass and the yoke can fly six feet or more from the implosion. Use care when replacing any display.

Ireland-Built Cabinet

Removing the Video Display:

1. From the back of the cabinet, open the rear access panel. Unplug the display harness connectors and disconnect the ground wire (see *Figure 3-8*).
2. From the front of the cabinet, open the control panel (see *Figure 3-3*).
3. Grasp the metal retainer that holds the bottom of the video display shield and slide the retainer and the shield down and out of the cabinet.
4. Remove the cardboard bezel.
5. The wood display shelf is secured to the cabinet with two metal brackets. Remove the two sets of hardware that secure the shelf to these brackets.
6. Carefully pull the wood display shelf and display out through the front of the cabinet. Place the display in a protected location. After servicing the display, reinstall it in reverse order.



Circled numbers match numbered instructions. Disassemble in the order indicated.

Figure 3-8 Video Display, continued
Ireland-Built Cabinet

Video Display
Upright and Ireland-Built Cabinets
Parts List

Part No.	*Description*
	For Upright Cabinet
038493-01	Display Bezel
038491-01	Display Shield
038496-01	Speaker Grille
038505-01	Lower Retainer
	For Ireland-Built Cabinet
A038808-01	Display Bezel
002728-01	Display Shelf Bracket
038804-02	Display Shelf
038805-01	Display Shield Retainer
038992-01	Display Shield
	For Upright and Ireland-Built Cabinets
92-049	19-Inch Electrohome Color Raster-Scan Display *Alternate displays are:* *92-055—19-Inch Wells-Gardner Color Raster-Scan Display* *139003-1004—19-Inch Matsushita Color Raster-Scan Display*

E. Utility Panel

WARNING

Before removing or repairing the utility panel, **switch the game to *off*.**

Players may receive an electric shock if the utility panel is not properly grounded! After servicing any parts on the panel, make sure that the ground wire is firmly attached to the metal screw on the back of the coin counter.

NOTE

Only the Ireland-Built cabinet has two coin counters.

The utility panel is located inside the upper coin door. This panel includes the volume control, self-test switch, auxiliary coin switch, and the coin counter(s). The coin switch is used to credit the game without activating the coin counter.

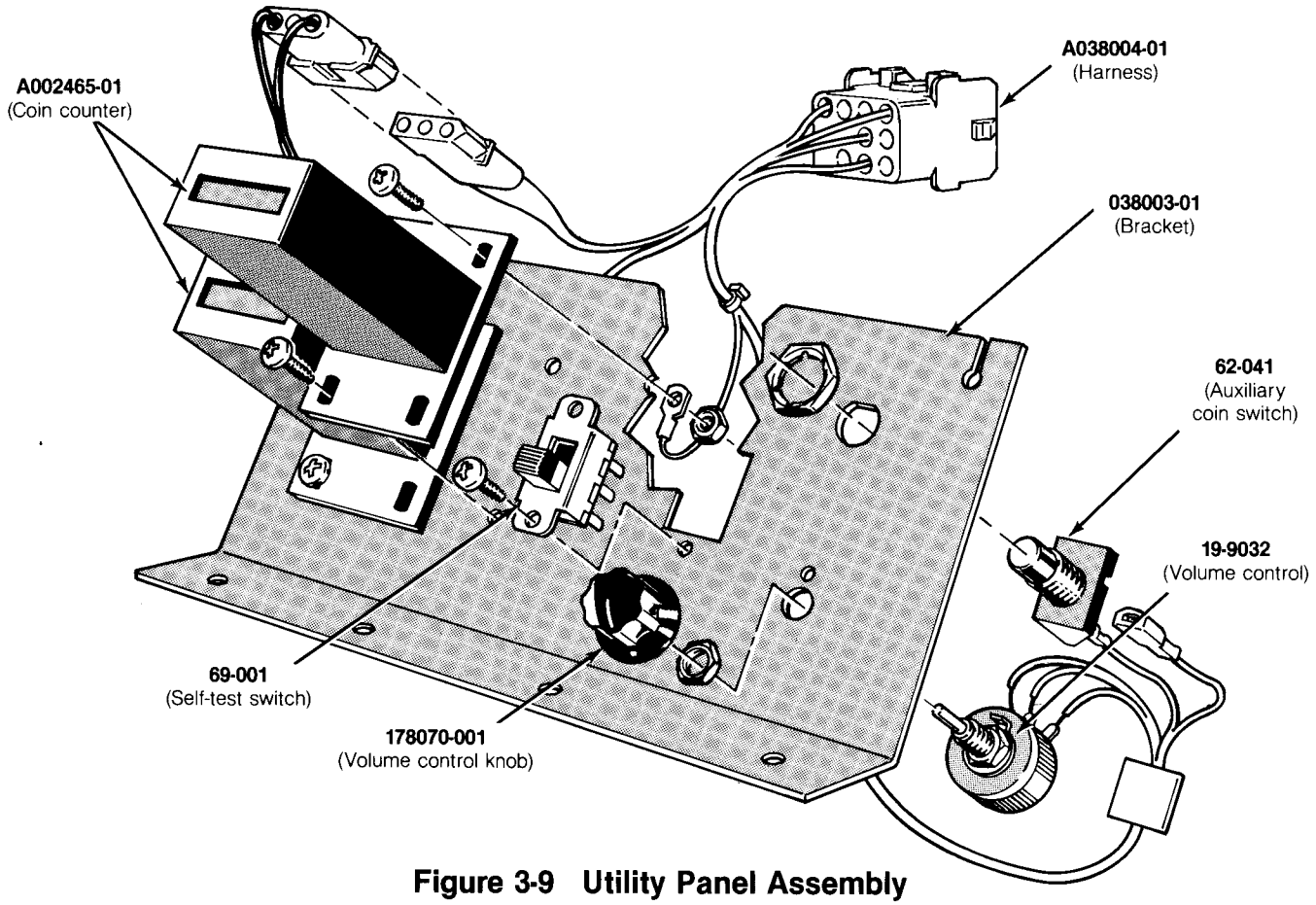


Figure 3-9 Utility Panel Assembly

Parts List

Part No.	*Description*
A002465-01	6 V Coin Counter
A038004-01	Utility Panel Harness
19-9032	Volume Control
62-041	SPDT Momentary-Contact Pushbutton Auxiliary Coin Switch with Black Cap
69-001	DPDT Self-Test Switch
038003-01	Utility Panel Bracket
178070-001	Volume Control Knob

F. Coin Door

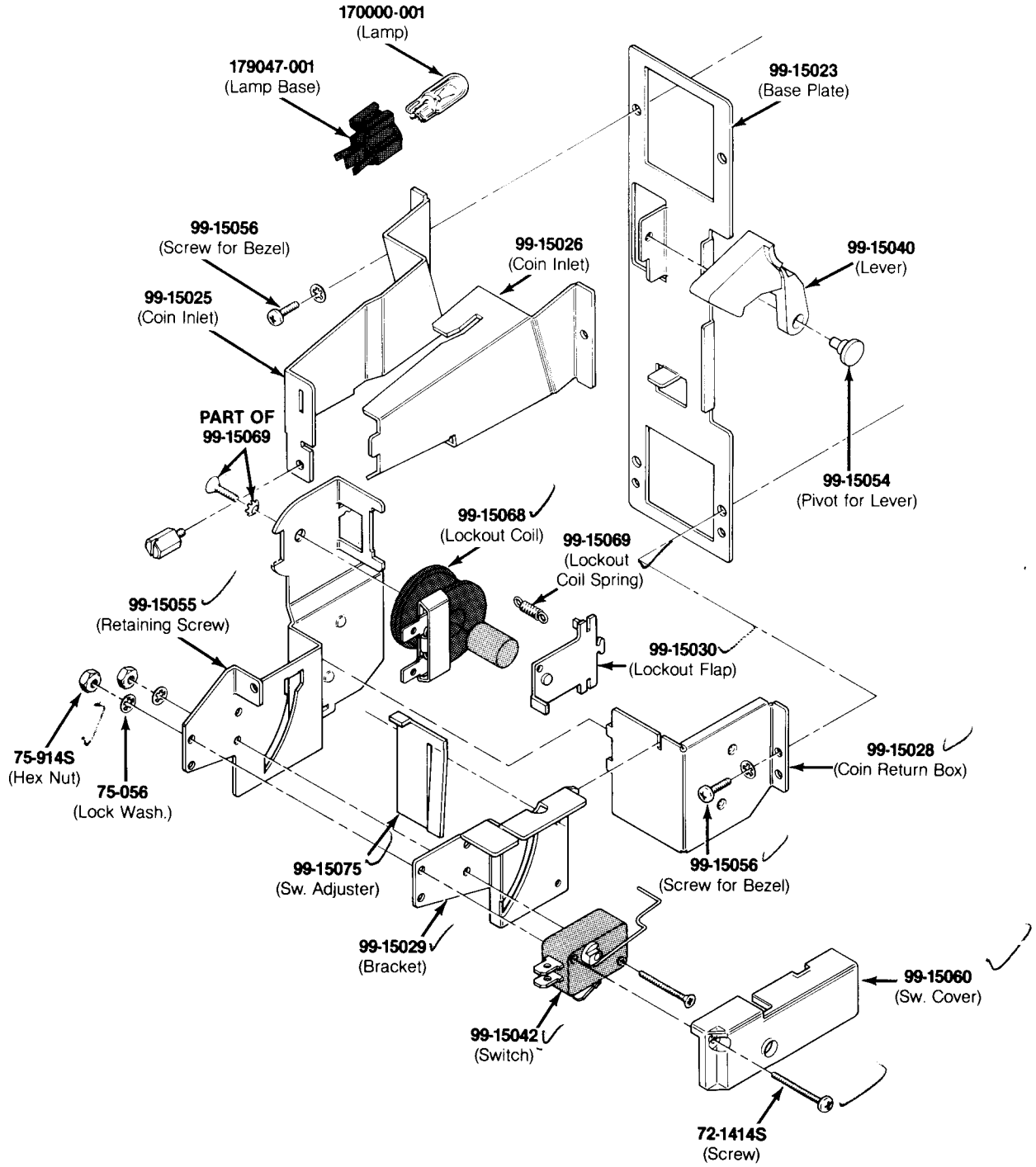
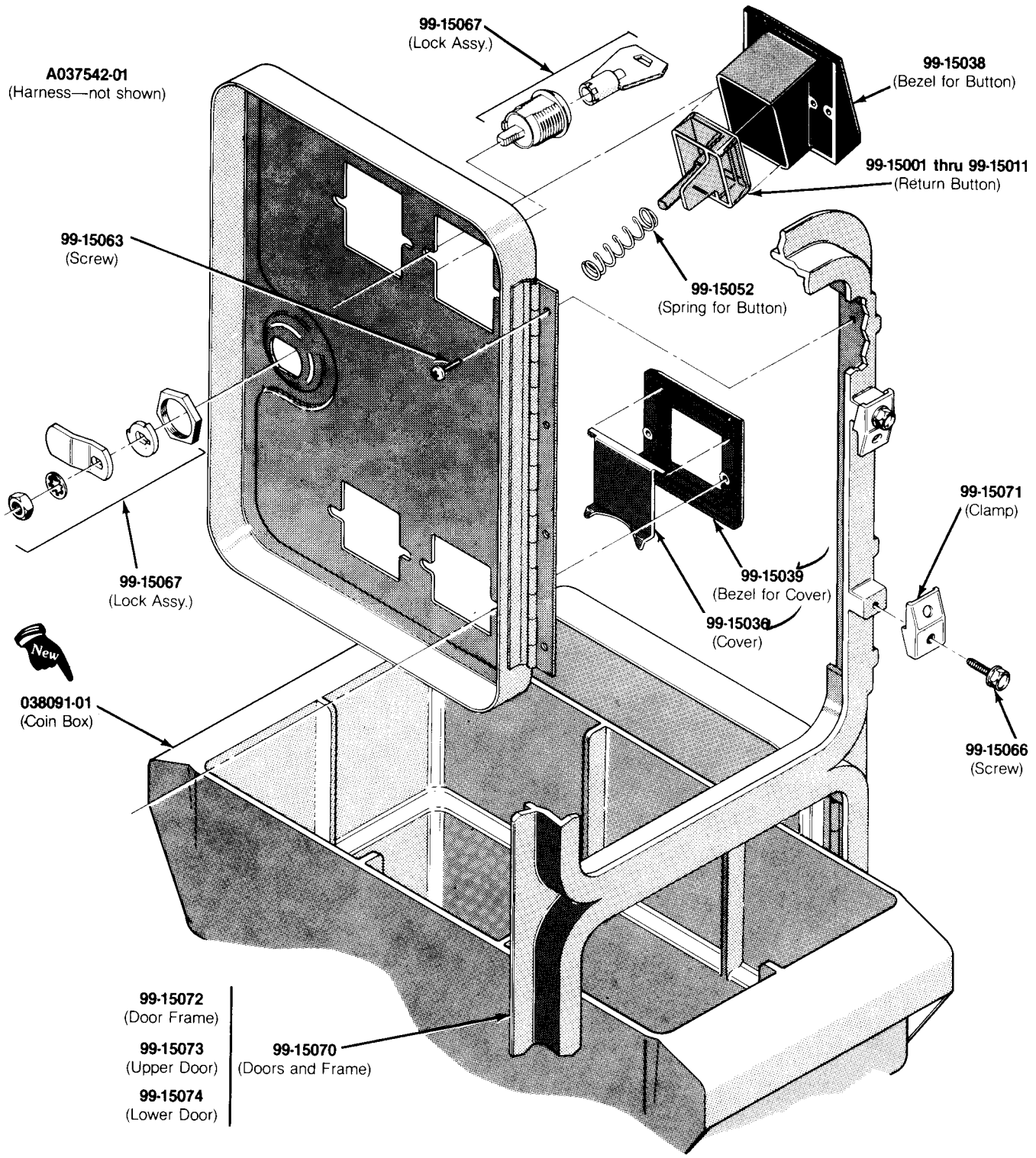


Figure 3-10 Vertically Mounted Coin Door
A037619-xx D



A037619-01 — U.S. 25¢/25¢ Coin Door
A037619-02 — U.S. 50¢/50¢ Coin Door
A037619-03 — Canadian 25¢/25¢ Coin Door
A037619-04 — British 10 P/10 P Coin Door
A037619-05 — British 10 P/50 P Coin Door
A037619-06 — British 20 P/50 P Coin Door
A037619-07 — Australian 20¢/20¢ Coin Door
A037619-08 — German 1 DM/1 DM Coin Door
A037619-09 — German 2 DM/1 DM Coin Door
A037619-10 — German 2 DM/5 DM Coin Door
A037619-11 — German 1 DM/5 DM Coin Door
A037619-12 — 5 Fr/5 Fr Coin Door
A037619-13 — Swiss 1 Fr/1 Fr Coin Door
A037619-14 — French 1 Fr/1 Fr Coin Door
A037619-15 — French 2 Fr/1 Fr Coin Door
A037619-16 — Swedish 1 Kr/1 Kr Coin Door
A037619-17 — Spanish 25 Pts/25 Pts Coin Door
A037619-18 — Italian 100 L/100 L Coin Door
A037619-19 — Hong Kong $1/$1 Coin Door
A037619-20 — Japanese 100Y/100Y Coin Door

Figure 3-10 Vertically Mounted Coin Door, continued
A037619-xx D

Vertically Mounted Coin Door
Parts List

Part No.	*Description*
A037542-01	Harness Assembly
72-1414S	#4-40 × 7/8-Inch Cross-Recessed Pan-Head Steel Machine Screw
75-056	#6 Internal-Tooth Zinc-Plated Steel Lock Washer
75-914S	#4-40 Steel Machine Hex Nut
75-3414S	#4-40 × 7/8-Inch 82° Cross-Recessed Flat-Head Steel Machine Screw
99-15001	Coin Return Button with U.S. 25¢ Price Plate
99-15002	Coin Return Button with U.S. $1 Price Plate
99-15003	Coin Return Button with German 1 DM Price Plate
99-15004	Coin Return Button with German 2 DM Price Plate
99-15005	Coin Return Button with German 5 DM Price Plate
99-15006	Coin Return Button with Belgian 5 Fr Price Plate
99-15007	Coin Return Button with French 1 Fr Price Plate
99-15008	Coin Return Button with Japanese 100 Yen Price Plate
99-15009	Coin Return Button with British 10 Pence Price Plate
99-15010	Coin Return Button with Australian 20¢ Price Plate
99-15011	Coin Return Button with Italian 100 Lire Price Plate
99-15023	Base Plate
99-15025	Left Half of Coin Inlet
99-15026	Right Half of Coin Inlet
99-15027	Side Plate of Coin Return Box
99-15028	Base Plate of Coin Return Box
99-15029	Switch Bracket
99-15030	Flap for Lockout Coil *(U.S. 25¢)*
99-15036	Metal Coin Return Cover
99-15038	Bezel for Coin Return Button
99-15039	Metal Bezel for Coin Return Cover
99-15040	Coin Return Lever
99-15042	Coin Switch for U.S. 25¢
99-15052	Spring for Coin Return Button
99-15054	Pivot for Coin Return Lever
99-15055	Retaining Screw
99-15056	#4-40 × 5/16-Inch Cross-Recessed Pan-Head Steel Machine Screw
99-15060	Switch Cover
99-15063	Screw for Hinge
99-15066	Screw for Clamp
99-15067	Lock Assembly
99-15068	Lockout Coil
99-15069	Spring for Lockout Coil
99-15070	Doors and Frame
99-15071	Clamp for Frame
99-15072	Door Frame
99-15073	Upper Door
99-15074	Lower Door
99-15075	Switch Adjuster
038091-01	Coin Box *(Not included in assembly) Acceptable substitute is part number A037491-01*
170000-001	6.3V Miniature Wedge-Base Incandescent Lamp
171006-035	Metal Coin Mechanism
179047-001	Lamp Base

G. Printed-Circuit Boards

WARNING

Before you remove or repair any printed-circuit board (PCB), **switch the game to *off*.**

Removing the Printed-Circuit Boards:

1. Open the rear access panel.
2. For the *game PCB,* unplug the two edge connectors (*see Figure 3-11*).
3. Remove the screw and two washers that secure the PCB to the cabinet. **Carefully** slide the PCB straight out of its slots. Be careful not to twist the board, as this may loosen connections or components. Replace or repair as required, and reinstall the PCB.
4. For the *Regulator/Audio II PCB,* disconnect the five small harness connectors on this board.
5. Remove the screw and two spacers that secure the Regulator/Audio II PCB to the cabinet, and carefully remove the board from its slot. Do not twist the board, as this may loosen connections or components. Replace or repair as required, and reinstall the PCB.

CAUTION

Make sure that the connectors on the PCB are properly plugged in. Note that they are keyed to fit only one way. If they do not slip on easily, do not force them. **A reversed connector may damage your game** and void the warranty.

6. Close and lock the rear access panel.
7. Make sure that the game is operating correctly by performing the self-test. Performing self-test is very important when you repair a PCB.

Printed-Circuit Board Mounting Hardware Parts List

Part No.	*Description*
72-6810S	#8 x ⅝-Inch Cross-Recessed Pan-Head Screw
034536-02	Foam Pad
038178-03	Dual-Slotted Retainer
175004-708	#8 Fiber Washer
176015-110	#10 x ⅝-Inch Pan-Head Screw

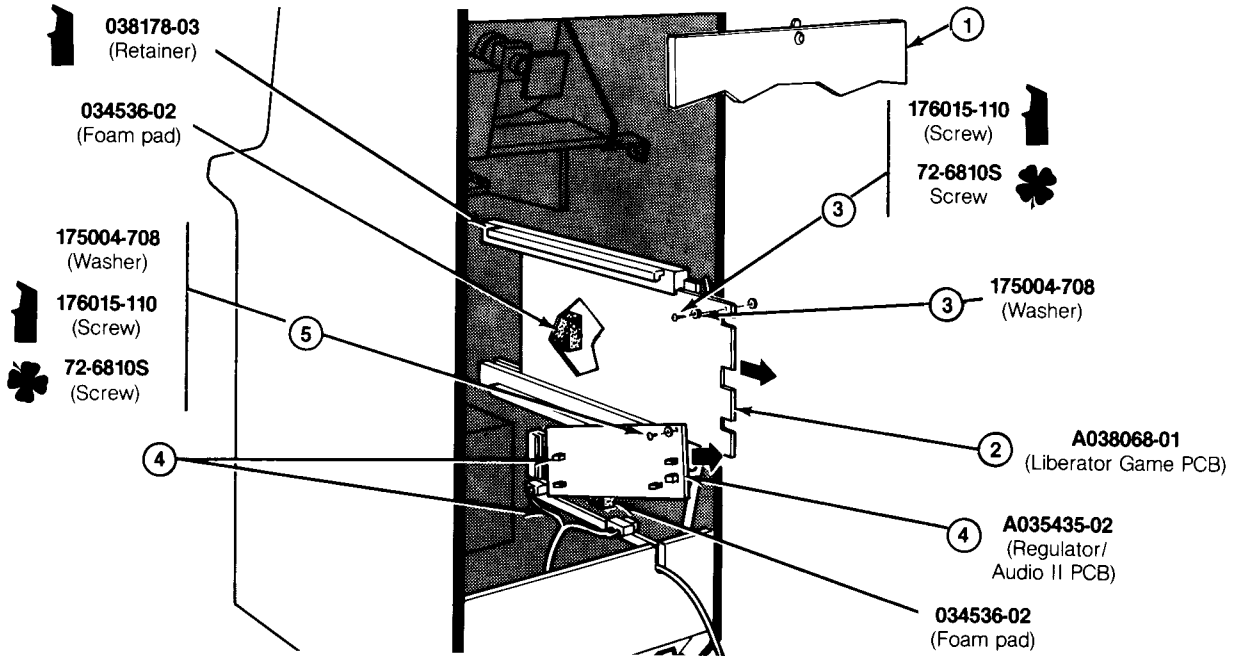
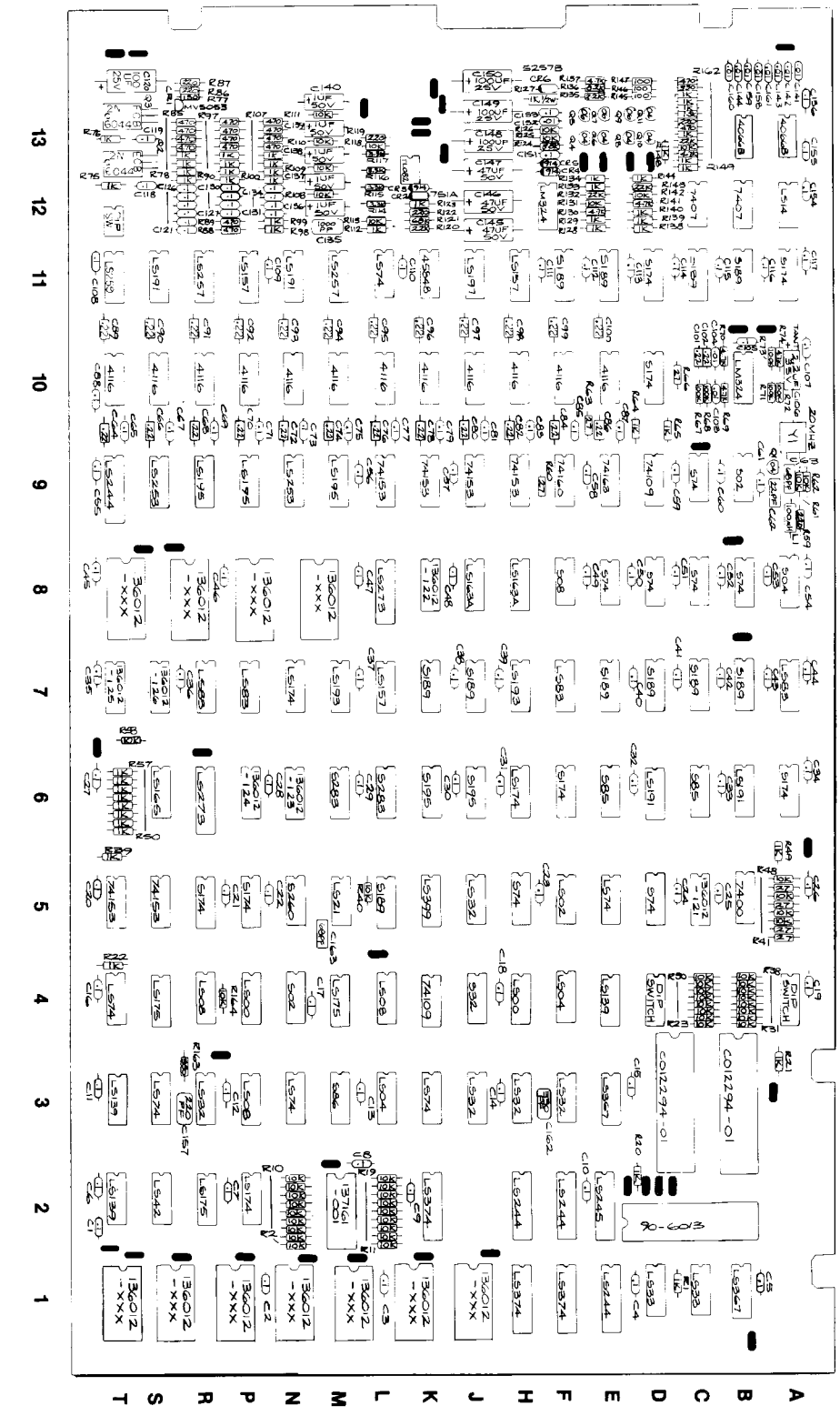


Figure 3-11 Removing the Printed-Circuit Boards



Acceptable substitutes are A038068-11 and A038068-31.

Figure 3-12 Liberator™ Game PCB Assembly A038068-21 B

Liberator™ Game PCB Assembly Parts List

Designator	Description	Part No.
	Capacitors	
C1-C61	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C62	22 pF, 100 V, Epoxy-Dipped Mica Radial-Lead Capacitor	128002-220
C63	68 pF, 100 V, Epoxy-Dipped Mica Radial-Lead Capacitor	128002-680
C64	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C65	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C66	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C67	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C68	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C69	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C70	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C71	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C72	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C73	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C74	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C75	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C76	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C77	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C78	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C79	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C80	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C81	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C82	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C83	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C84	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C85	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C86	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C87, C88	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C89-C102	0.22 μF, +80, -20%, 25 V Ceramic-Disk Radial-Lead Capacitor	122008-224
C103, C104	0.01 μF, +80, -20%, 25 V Ceramic-Disk Axial-Lead Capacitor	122005-103
C105	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C106	2.2 μF, ±10%, 35 V Tantalum Capacitor	122000-225
C107-C119	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C120	100 μF, 25 V, Aluminum Electrolytic Axial-Lead Capacitor	24-250107
C121-C134	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C135	1000 pF, 100 V, Epoxy-Dipped Mica Radial-Lead Capacitor	128002-102
C136-C140	1 μF, 50 V, Aluminum Electrolytic Axial-Lead Capacitor	24-500105
C141-C144	0.01 μF, +80, -20%, 25 V Ceramic-Disk Axial-Lead Capacitor	122005-103
C145-C147	47 μF, 50 V, Aluminum Electrolytic Axial-Lead Capacitor	24-500476
C148-C150	100 μF, 25 V, Aluminum Electrolytic Axial-Lead Capacitor	24-250107
C151	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C152	0.01 μF, +80, -20%, 25 V Ceramic-Disk Axial-Lead Capacitor	122005-103
C153-C156	0.1 μF, +80, -20%, 50 V Ceramic-Disk Radial-Lead Capacitor	122002-104
C157	220 pF, 100 V, Epoxy-Dipped Mica Radial-Lead Capacitor	128002-221
C158-C161	0.01 μF, +80, -20%, 25 V Ceramic-Disk Axial-Lead Capacitor	122005-103
C162	330 pF, 100 V, Mica Capacitor	128002-331
C163	68 pF, 100 V, Epoxy-Dipped Mica Radial-Lead Capacitor	128002-680

(Continued on next page)

Liberator™ Game PCB Assembly
Parts List, continued

Designator	Description	Part No.
	Diodes	
CR1	Type-MV5053 Light-Emitting Diode	38-MV5053
CR2	Type1N751A, ±5%, 5.1 V, 500 mW Zener Diode	32-1N751A
CR3-CR5	Type-1N914, 75 V Switching Diode	31-1N914
CR6	Type1N5257B, ±5%, 33 V Zener Diode	131003-001
	Integrated Circuits	
A6	Type-74LS174 Integrated Circuit	137209-001
A7	Type-74LS83 Integrated Circuit	37-74LS83
A8	Type-74S04 Integrated Circuit	37-74S04
A11	Type-74LS174 Integrated Circuit	137209-001
A12	Type-74LS14 Integrated Circuit	37-74LS14
A13	Type-4066B Integrated Circuit	37-4066
B1	Type-74LS367 Integrated Circuit	37-74LS367
B5	Type-7400 Integrated Circuit	37-7400
B6	Type-74LS191 Integrated Circuit	37-74LS191
B7	Type-74S189 Integrated Circuit	37-74S189
B8	Type-74S74 Integrated Circuit	37-74S74
B9	Type-74S02 Integrated Circuit	37-74S02
B10	Type-LM324 Integrated Circuit	37-LM324
B11	Type-74S189 Integrated Circuit	37-74S189
B12	Type-7407 Integrated Circuit	37-7407
B13	Type-4066B Integrated Circuit	37-4066
C1	Type-74LS33 Integrated Circuit	137239-001
C6	Type-74S85 Integrated Circuit	37-74S85
C7	Type-74S189 Integrated Circuit	37-74S189
C8, C9	Type-74S74 Integrated Circuit	37-74S74
C11	Type-74S189 Integrated Circuit	37-74S189
C12	Type-7407 Integrated Circuit	37-7407
D1	Type-74LS33 Integrated Circuit	137239-001
D5	Type-74S74 Integrated Circuit	37-74S74
D6	Type-74LS191 Integrated Circuit	37-74LS191
D7	Type-74S189 Integrated Circuit	37-74S189
D8	Type-74S74 Integrated Circuit	37-74S74
D9	Type-74109 Integrated Circuit	37-74109
D10, D11	Type-74LS174 Integrated Circuit	137209-001
E1	Type-74LS244 Integrated Circuit	37-74LS244
E2	Type-74LS245 Integrated Circuit	37-74LS245
E3	Type-74LS367 Integrated Circuit	37-74LS367
E4	Type-74LS139 Integrated Circuit	37-74LS139
E5	Type-74LS74 Integrated Circuit	37-74LS74
E6	Type-74S85 Integrated Circuit	37-74S85
E7	Type-74S189 Integrated Circuit	37-74S189

(Continued on next page)

Liberator™ Game PCB Assembly Parts List, continued

Designator	Description	Part No.
E8	Type-74S74 Integrated Circuit	37-74S74
E9	Type-74163 Integrated Circuit	37-74163
E11	Type-74S189 Integrated Circuit	37-74S189
F1	Type-74LS374 Integrated Circuit	37-74LS374
F2	Type-74LS244 Integrated Circuit	37-74LS244
F3	Type-74LS32 Integrated Circuit	37-74LS32
F4	Type-74LS04 Integrated Circuit	37-74LS04
F5	Type-74LS02 Integrated Circuit	37-74LS02
F6	Type-74LS174 Integrated Circuit	137209-001
F7	Type-74LS83 Integrated Circuit	37-74LS83
F8	Type-74S08 Integrated Circuit	37-74S08
F9	Type-74160 Integrated Circuit	37-74160
F11	Type-74S189 Integrated Circuit	37-74S189
F/H12	Type-LM324 Integrated Circuit	37-LM324
H1	Type-74LS374 Integrated Circuit	37-74LS374
H2	Type-74LS244 Integrated Circuit	37-74LS244
H3	Type-74LS32 Integrated Circuit	37-74LS32
H4	Type-74LS00 Integrated Circuit	37-74LS00
H5	Type-74S74 Integrated Circuit	37-74S74
H6	Type-74LS174 Integrated Circuit	37-74LS174
H7	Type-74LS193 Integrated Circuit	37-74LS193
H8	Type-74LS163A Integrated Circuit	37-74LS163A
H9	Type-74153 Integrated Circuit	37-74153
H11	Type-74LS157 Integrated Circuit	37-74LS157
J3	Type-74LS32 Integrated Circuit	37-74LS32
J4	Type-74S32 Integrated Circuit	37-74S32
J5	Type-74LS32 Integrated Circuit	37-74LS32
J6	Type-74LS195 Integrated Circuit	137208-001
J7	Type-74S189 Integrated Circuit	37-74S189
J8	Type-74LS163A Integrated Circuit	37-74LS163A
J9	Type-74153 Integrated Circuit	37-74153
J11	Type-74LS197 Integrated Circuit	137240-001
K2	Type-74LS374 Integrated Circuit	37-74LS374
K3	Type-74LS74 Integrated Circuit	37-74LS74
K4	Type-74109 Integrated Circuit	37-74109
K5	Type-74LS399 Integrated Circuit	37-74LS399
K6	Type-74LS195 Integrated Circuit	137208-001
K7	Type-74S189 Integrated Circuit	37-74S189
K9	Type-74153 Integrated Circuit	37-74153
K11	Schmitt Trigger Hex Integrated Circuit	37-4584B
K12	Type-TL082 Integrated Circuit	37-TL082CP
L3	Type-74LS04 Integrated Circuit	37-74LS04
L4	Type-74LS08 Integrated Circuit	37-74LS08
L5	Type-74S189 Integrated Circuit	37-74S189

(Continued on next page)

Liberator™ Game PCB Assembly
Parts List, continued

Designator	*Description*	*Part No.*
L6	Type-74LS283 Integrated Circuit	137241-001
L7	Type-74LS157 Integrated Circuit	37-74LS157
L8	Type-74LS273 Integrated Circuit	37-74LS273
L9	Type-74153 Integrated Circuit	37-74153
L11	Type-74LS74 Integrated Circuit	37-74LS74
M3	Type-74S86 Integrated Circuit	137002-001
M4	Type-74LS175 Integrated Circuit	37-74LS175
M5	Type-74LS21 Integrated Circuit	137210-001
M6	Type-74LS283 Integrated Circuit	137241-001
M7	Type-74LS193 Integrated Circuit	37-74LS193
M9	Type-74LS195 Integrated Circuit	37-74LS195
M11	Type-74LS257 Integrated Circuit	37-74LS257
N3	Type-74LS74 Integrated Circuit	37-74LS74
N4	Type-74S02 Integrated Circuit	37-74S02
N5	Type-74S260 Integrated Circuit	37-74S260
N7	Type-74LS174 Integrated Circuit	37-74LS174
N9	Type-74LS253 Integrated Circuit	37-74LS253
N11	Type-74LS191 Integrated Circuit	37-74LS191
P2	Type-74LS174 Integrated Circuit	37-74LS174
P3	Type-74LS08 Integrated Circuit	37-74LS08
P4	Type-74LS00 Integrated Circuit	37-74LS00
P5	Type-74LS174 Integrated Circuit	137209-001
P7	Type-74LS83 Integrated Circuit	37-74LS83
P9	Type-74LS195 Integrated Circuit	37-74LS195
P11	Type-74LS157 Integrated Circuit	37-74LS157
R2	Type-74LS175 Integrated Circuit	37-74LS175
R3	Type-74LS32 Integrated Circuit	37-74LS32
R4	Type-74LS08 Integrated Circuit	37-74LS08
R5	Type-74LS174 Integrated Circuit	137209-001
R6	Type-74LS273 Integrated Circuit	37-74LS273
R7	Type-74LS83 Integrated Circuit	37-74LS83
R9	Type-74LS195 Integrated Circuit	37-74LS195
R11	Type-74LS257 Integrated Circuit	37-74LS257
S2	Type-74LS42 Integrated Circuit	37-74LS42
S3	Type-74LS74 Integrated Circuit	37-74LS74
S4	Type-74LS175 Integrated Circuit	37-74LS175
S5	Type-74153 Integrated Circuit	37-74153
S6	Type-74LS165 Integrated Circuit	37-74LS165
S9	Type-74LS253 Integrated Circuit	37-74LS253
S11	Type-74LS191 Integrated Circuit	37-74LS191
T2, T3	Type-74LS139 Integrated Circuit	37-74LS139
T4	Type-74LS74 Integrated Circuit	37-74LS74
T5	Type-74153 Integrated Circuit	37-74153
T9	Type-74LS244 Integrated Circuit	37-74LS244
T11	Type-74LS259 Integrated Circuit	37-74LS259

(Continued on next page)

Liberator™ Game PCB Assembly
Parts List, continued

Designator	Description	Part No.
	Resistors	
R1	1 kΩ, ±5%, ¼ W Resistor	110000-102
R2-19	10 kΩ, ±5%, ¼ W Resistor	110000-103
R20-R22	1 kΩ, ±5%, ¼ W Resistor	110000-102
R23-R38	10 kΩ, ±5%, ¼ W Resistor	110000-103
R39	1 kΩ, ±5%, ¼ W Resistor	110000-102
R40	10 kΩ, ±5%, ¼ W Resistor	110000-103
R41, R42	27 Ω, ±5%, ¼ W Resistor	110000-270
R43, R44	10 kΩ, ±5%, ¼ W Resistor	110000-103
R45	27 Ω, ±5%, ¼ W Resistor	110000-270
R46	10 kΩ, ±5%, ¼ W Resistor	110000-103
R47	27 Ω, ±5%, ¼ W Resistor	110000-270
R48	10 kΩ, ±5%, ¼ W Resistor	110000-103
R49-R57	1 kΩ, ±5%, ¼ W Resistor	110000-102
R58	10 kΩ, ±5%, ¼ W Resistor	110000-103
R59	220 Ω, ±5%, ¼ W Resistor	110000-221
R60	27 Ω, ±5%, ¼ W Resistor	110000-270
R61, R62	10 kΩ, ±5%, ¼ W Resistor	110000-103
R63	27 Ω, ±5%, ¼ W Resistor	110000-270
R64, R65	1 kΩ, ±5%, ¼ W Resistor	110000-102
R66	27 Ω, ±5%, ¼ W Resistor	110000-270
R67, R68	100 kΩ, ±5%, ¼ W Resistor	110000-104
R69, R70	4.7 kΩ, ±5%, ¼ W Resistor	110000-472
R71-R73	100 kΩ, ±5%, ¼ W Resistor	110000-104
R74	47 kΩ, ±5%, ¼ W Resistor	110000-473
R75, R76	1 kΩ, ±5%, ¼ W Resistor	110000-102
R77	150 Ω, ±5%, ¼ W Resistor	110000-151
R78-R81	1 kΩ, ±5%, ¼ W Resistor	110000-102
R82-R85	470 Ω, ±5%, ¼ W Resistor	110000-471
R86, R87	220 Ω, ±5%, ¼ W Resistor	110000-221
R88, R89	470 Ω, ±5%, ¼ W Resistor	110000-471
R90-R93	1 kΩ, ±5%, ¼ W Resistor	110000-102
R94-R97	470 Ω, ±5%, ¼ W Resistor	110000-471
R98-R103	1 kΩ, ±5%, ¼ W Resistor	110000-102
R104-R107	470 Ω, ±5%, ¼ W Resistor	110000-471
R108-R111	10 kΩ, ±5%, ¼ W Resistor	110000-103
R112	1 kΩ, ±5%, ¼ W Resistor	110000-102
R113	10 kΩ, ±5%, ¼ W Resistor	110000-103
R114-R117	3.3 kΩ, ±5%, ¼ W Resistor	110000-332
R118	10 kΩ, ±5%, ¼ W Resistor	110000-103
R119	220 Ω, ±5%, ¼ W Resistor	110000-221
R120	22 kΩ, ±5%, ¼ W Resistor	110000-223
R121	68 kΩ, ±5%, ¼ W Resistor	110000-683
R122	220 Ω, ±5%, ¼ W Resistor	110000-221
R123	1 kΩ, ±5%, ¼ W Resistor	110000-102

[Continued on next page]

Liberator™ Game PCB Assembly
Parts List, continued

Designator	*Description*	*Part No.*
R124	3.3 kΩ, ±5%, ¼ W Resistor	110000-332
R125, R126	10 kΩ, ±5%, ¼ W Resistor	110000-103
R127	1 kΩ, ±5%, ½ W Resistor	110001-102
R128, R129	1 kΩ, ±5%, ¼ W Resistor	110000-102
R130	4.7 kΩ, ±5%, ¼ W Resistor	110000-472
R131	10 kΩ, ±5%, ¼ W Resistor	110000-103
R132	22 kΩ, ±5%, ¼ W Resistor	110000-223
R133, R134	1 kΩ, ±5%, ¼ W Resistor	110000-102
R135	2.2 kΩ, ±5%, ¼ W Resistor	110000-222
R136	8.2 kΩ, ±5%, ¼ W Resistor	110000-822
R137	4.7 kΩ, ±5%, ¼ W Resistor	110000-472
R138–R140	1 kΩ, ±5%, ¼ W Resistor	110000-102
R141	4.7 kΩ, ±5%, ¼ W Resistor	110000-472
R142	10 kΩ, ±5%, ¼ W Resistor	110000-103
R143	22 kΩ, ±5%, ¼ W Resistor	110000-223
R144	1 kΩ, ±5%, ¼ W Resistor	110000-102
R145–R147	100 Ω, ±5%, ¼ W Resistor	110000-101
R148–R150	1 kΩ, ±5%, ¼ W Resistor	110000-102
R151	4.7 kΩ, ±5%, ¼ W Resistor	110000-472
R152	10 kΩ, ±5%, ¼ W Resistor	110000-103
R153	22 kΩ, ±5%, ¼ W Resistor	110000-223
R154	1 kΩ, ±5%, ¼ W Resistor	110000-102
R155	470 Ω, ±5%, ¼ W Resistor	110000-471
R156	220 Ω, ±5%, ¼ W Resistor	110000-221
R157	1.5 kΩ, ±5%, ¼ W Resistor	110000-151
R158–R160	1 kΩ, ±5%, ¼ W Resistor	110000-102
R161	330 Ω, ±5%, ¼ W Resistor	110000-331
R162	470 Ω, ±5%, ¼ W Resistor	110000-471
R163	330 Ω, ±5%, ¼ W Resistor	110000-331
R164	10 kΩ, ±5%, ¼ W Resistor	110000-103
	Programmable Read-Only Memories	
C5	Programmable Read-Only Memory	136012-121
K8	Programmable Read-Only Memory	136012-122
N6	Programmable Read-Only Memory	136012-123
P6	Programmable Read-Only Memory	136012-124
T7	Programmable Read-Only Memory	136012-125
S7	Programmable Read-Only Memory	136012-126
	For -11 version only	
C2	Type-6502A Microprocessor	90-6013
B/C3	Audio I/O N-Channel MOS/LSI Custom Chip	C012294-01
C/D3	Audio I/O N-Channel MOS/LSI Custom Chip	C012294-01
J1	Type-137184-001 Programmable Read-Only Memory	136012-216

(Continued on next page)

Liberator™ Game PCB Assembly Parts List, continued

Designator	Description	Part No.
K/L1	Type-137184-001 Programmable Read-Only Memory	136012-215
L/M1	Type-137184-001 Programmable Read-Only Memory	136012-214
M2	4 μs, 64 x 8, Tri-State Electrically Alterable Read-Only Memory	137161-001
M/N8	Type-137184-001 Programmable Read-Only Memory	136012-118
N1	Type-137184-001 Programmable Read-Only Memory	136012-213
P8	Type-137184-001 Programmable Read-Only Memory	136012-120
P/R1	Type-137184-001 Programmable Read-Only Memory	136012-212
R/S1	Type-137184-001 Programmable Read-Only Memory	136012-211
R/S8	Type-137184-001 Programmable Read-Only Memory	136012-117
T1	Type-137184-001 Programmable Read-Only Memory	136012-228
T8	Type-137184-001 Programmable Read-Only Memory	136012-119
	For -21 version only	
C2	Type-6502A Microprocessor	90-6013
B/C3	Audio I/O N-Channel MOS/LSI Custom Chip	C012294-01
C/D3	Audio I/O N-Channel MOS/LSI Custom Chip	C012294-01
J1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-206
K/L1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-205
L/M1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-204
M2	4 μSec, 64 x 8, Tri-State Electrically Alterable Read-Only Memory	137161-001
M/N8	Type-137171-001 Electrically Programmable Read-Only Memory	136012-108
N1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-203
P8	Type-137171-001 Electrically Programmable Read-Only Memory	136012-110
P/R1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-202
R/S1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-201
R/S8	Type-137171-001 Electrically Programmable Read-Only Memory	136012-107
T1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-200
T8	Type-137171-001 Electrically Programmable Read-Only Memory	136012-109
	For -31 version only	
C2	Type-6502A Microprocessor	90-6013
B/C3	Audio I/O N-Channel MOS/LSI Custom Chip	C012294-01
C/D3	Audio I/O N-Channel MOS/LSI Custom Chip	C012294-01
J1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-206
K/L1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-205
L/M1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-204
M2	4 μs, 64 x 8, Tri-State Electrically Alterable Read-Only Memory	137161-001
M/N8	Type-137171-001 Electrically Programmable Read-Only Memory	136012-118
N1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-203
P8	Type-137171-001 Electrically Programmable Read-Only Memory	136012-120
P/R1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-202
R/S1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-201
R/S8	Type-137171-001 Electrically Programmable Read-Only Memory	136012-117
T1	Type-137171-001 Electrically Programmable Read-Only Memory	136012-200
T8	Type-137171-001 Electrically Programmable Read-Only Memory	136012-119

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Liberator™ Game PCB Assembly
Parts List, continued

Designator	Description	Part No.
	Random-Access Memories	
E10	Random-Access Memory	100017-001
F10	Random-Access Memory	100017-001
H10	Random-Access Memory	100017-001
J10	Random-Access Memory	100017-001
K10	Random-Access Memory	100017-001
L10	Random-Access Memory	100017-001
M10	Random-Access Memory	100017-001
N10	Random-Access Memory	100017-001
P10	Random-Access Memory	100017-001
R10	Random-Access Memory	100017-001
S10	Random-Access Memory	100017-001
T10	Random-Access Memory	100017-001
	Sockets	
B/C3	40-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C40
C2	40-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C40
C/D3	40-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C40
J1	24-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C24
K/L1	24-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C24
L/M1	24-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C24
M2	22-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C22
M/N8	24-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C24
N1	24-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C24
P8	24-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C24
P/R1	24-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C24
R/S1	24-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C24
R/S8	24-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C24
T1	24-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C24
T8	24-Contact Medium-Insertion-Force Integrated Circuit Socket	79-42C24
	Switches	
A4	8-Station, SPST, Dual-Inline-Package Switch	66-118P1T
D4	8-Station, SPST, Dual-Inline-Package Switch	66-118P1T
T12	4-Station, SPST, Dual-Inline-Package Switch	66-114P1T
	Transistors	
Q1	Type-2N3904 NPN 60 V, 1W Transistor	34-2N3904
Q2, Q3	Type-2N6044 Darlington NPN, 80 V, 8 A Transistor	34-2N6044
Q4	Type-2N3904 NPN 60 V, 1W Transistor	34-2N3904
Q5	Type-2N3906 PNP 40 V, 1W Transistor	33-2N3906

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Liberator™ Game PCB Assembly Parts List, continued

Designator	*Description*	*Part No.*
Q6	Type-2N3904 NPN 60 V, 1W Transistor	34-2N3904
Q7	Type-2N3906 PNP 40 V, 1W Transistor	33-2N3906
Q8	Type-2N3904 NPN 60 V, 1W Transistor	34-2N3904
Q9	Type-2N3906 PNP 40 V, 1W Transistor	33-2N3906
Q10, Q11	Type-2N3904 NPN 60 V, 1W Transistor	34-2N3904
	Miscellaneous	
	Test Point *Acceptable substitute is part no. 020670-01*	179051-002
Q2, Q3	Nylon Snap-In Fastener	81-4302
L1	100 μH, ± 10%, Hot-Molded Plastic Fixed R.F. Choke *Acceptable substitute is part no. 41-3003*	141002-001
Y1	20.00 MHz Crystal	144000-003

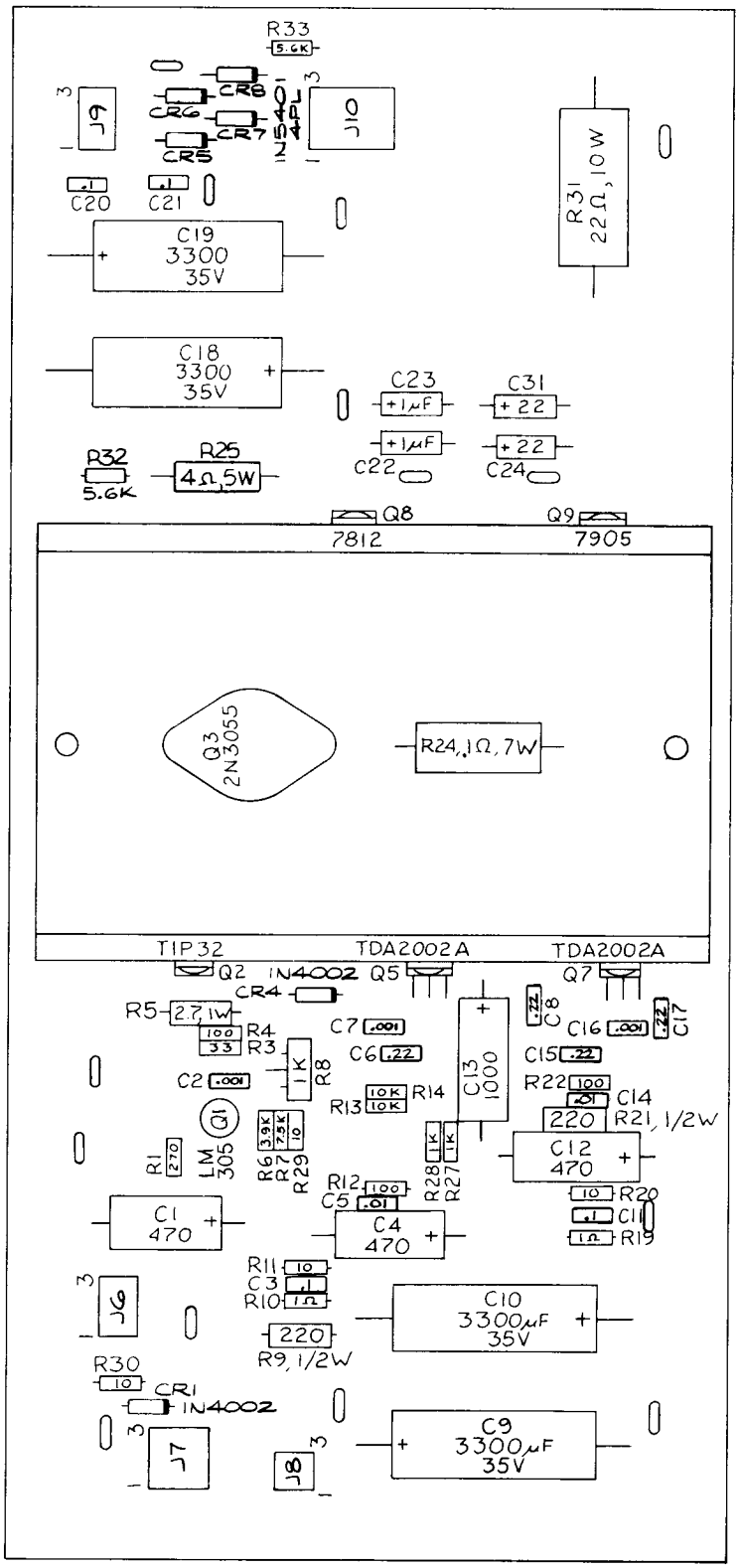

Figure 3-13 Regulator/Audio II PCB Assembly A035435-02 G

Regulator/Audio II PCB Assembly
Parts List

Designator	Description	Part No.
	Capacitors	
C1	470 μF, 25 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor	24-250477
C2	0.001 μF, 50 V, Ceramic-Disc Axial-Lead Capacitor	122002-102
C3	0.1 μF, 50 V, Ceramic-Disc Axial-Lead Capacitor	29-088
C4	470 μF, 25 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor	24-250477
C5	0.01 μF, 25 V Minimum, Ceramic-Disc Axial-Lead Capacitor *Acceptable substitute is part no. 122005-103*	100015-103
C6	0.22 μF, 25 V, Ceramic-Disc Axial-Lead Capacitor	122004-224
C7	0.001 μF, 50 V, Ceramic-Disc Axial-Lead Capacitor	122002-102
C8	0.22 μF, 25 V, Ceramic-Disc Axial-Lead Capacitor	122004-224
C9, C10	3300 μF, 35 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor	24-350338
C11	0.1 μF, 50 V, Ceramic-Disc Axial-Lead Capacitor	29-088
C12	470 μF, 25 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor	24-250477
C13	1000 μF, 25 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor	24-250108
C14	0.01 μF, 25 V Minimum, Ceramic-Disc Axial-Lead Capacitor *Acceptable substitute is part no. 122005-103*	100015-103
C15	0.22 μF, 25 V, Ceramic-Disc Axial-Lead Capacitor	122004-224
C16	0.001 μF, 50 V, Ceramic-Disc Axial-Lead Capacitor	122002-102
C17	0.22 μF, 25 V, Ceramic-Disc Axial-Lead Capacitor	122004-224
C18, C19	3300 μF, 35 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor	24-350338
C20, C21	0.1 μF, 50 V, Ceramic-Disc Axial-Lead Capacitor	29-088
C22, C23	1 μF, 50 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor	24-500105
C24	22 μF, 35 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor	24-350226
C31	22 μF, 35 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor	24-350226
	Diodes	
CR1	Type-1N4002, 1 A, 100 V Silicon Rectifier Diode	31-1N4002
CR4	Type-1N4002, 1 A, 100 V Silicon Rectifier Diode	31-1N4002
CR5-CR8	Type-1N5401, 3 A, 100 V Silicon Rectifier Diode	31-1N5401
	Integrated Circuits	
Q1	Type-LM305, 5 V, Linear Voltage Regulator	37-LM305
Q5	Type-TDA2002A, 8 W, Linear Audio Amplifier Integrated Circuit	137151-002
Q7	Type-TDA2002A, 8 W, Linear Audio Amplifier Integrated Circuit	137151-002
Q8	Type-7812, + 12 V, Voltage Regulator	37-7812
Q9	Type-7905, -5 V, Voltage Regulator	37-7905
	Resistors	
R1	270 Ω, ±5%, ¼ W Resistor	110000-271
R3	33 Ω, ±5%, ¼ W Resistor	110000-330
R4	100 Ω, ±5%, ¼ W Resistor	110000-101
R5	2.7 Ω, ±5%, 1 W Resistor	110009-027

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Regulator/Audio II PCB Assembly
Parts List, continued

Designator	*Description*	*Part No.*
R6	3.9 kΩ, ±5%, ¼ W Resistor	110000-392
R7	7.5 kΩ, ±5%, ¼ W Resistor	110000-752
R8	1 kΩ Vertical PCB-Mounting Cermet Potentiometer *Acceptable substitute is part no. 119002-102*	19-315102
R9	220 Ω, ±5%, ½ W Resistor	110001-221
R10	1 Ω, ±5%, ¼ W Resistor	110000-010
R11	10 Ω, ±5%, ¼ W Resistor	110000-100
R12	100 Ω, ±5%, ¼ W Resistor	110000-101
R13, R14	10 kΩ, ±5%, ¼ W Resistor	110000-103
R19	1 Ω, ±5%, ¼ W Resistor	110000-010
R20	10 Ω, ±5%, ¼ W Resistor	110000-100
R21	220 Ω, ±5%, ½ W Resistor	110001-221
R22	100 Ω, ±5%, ¼ W Resistor	110000-101
R24	0.1 Ω, ±3%, 7 W Wirewound Resistor	19-100P1015
R25	4 Ω, ±5%, 5 W Wirewound Resistor	116001-040
R27, R28	1 kΩ, ±5%, ¼ W Resistor	110000-102
R29, R30	10 Ω, ±5%, ¼ W Resistor	110000-100
R31	22 Ω, ±5%, 10 W Wirewound Resistor	116000-220
R32, R33	5.6 kΩ, ±5%, ¼ W Resistor	110000-562
	Transistors	
Q2	Type-TIP32 PNP Power Transistor	33-TIP32
Q3	Type-2N3055 NPN Silicon Transistor	34-2N3055
	Mechanical Parts	
J6	6-Position Connector Receptacle	79-58306
J7	9-Position Connector Receptacle	79-58308
J8	4-Position Connector Receptacle	79-58354
J9	6-Position Connector Receptacle	79-58306
J10	12-Position Connector Receptacle	79-58346
Q3	#6-32 x ½-Inch Cross-Recessed Pan-Head Corrosion-Resistant Steel Machine Screw	72-1608C
Q5	#6-32 x ¼-Inch Binder-Head Nylon Screw	75-F60405
Q8	#6 x ⅜-Inch Cross-Recessed Pan-Head Thread-Forming Type-AB Zinc-Plated-Steel Screw	72-6606S
	Heat Sink	034531-01
	Test Point *Acceptable substitute is part no. 020670-01*	179051-001

H. Power Supply Assembly

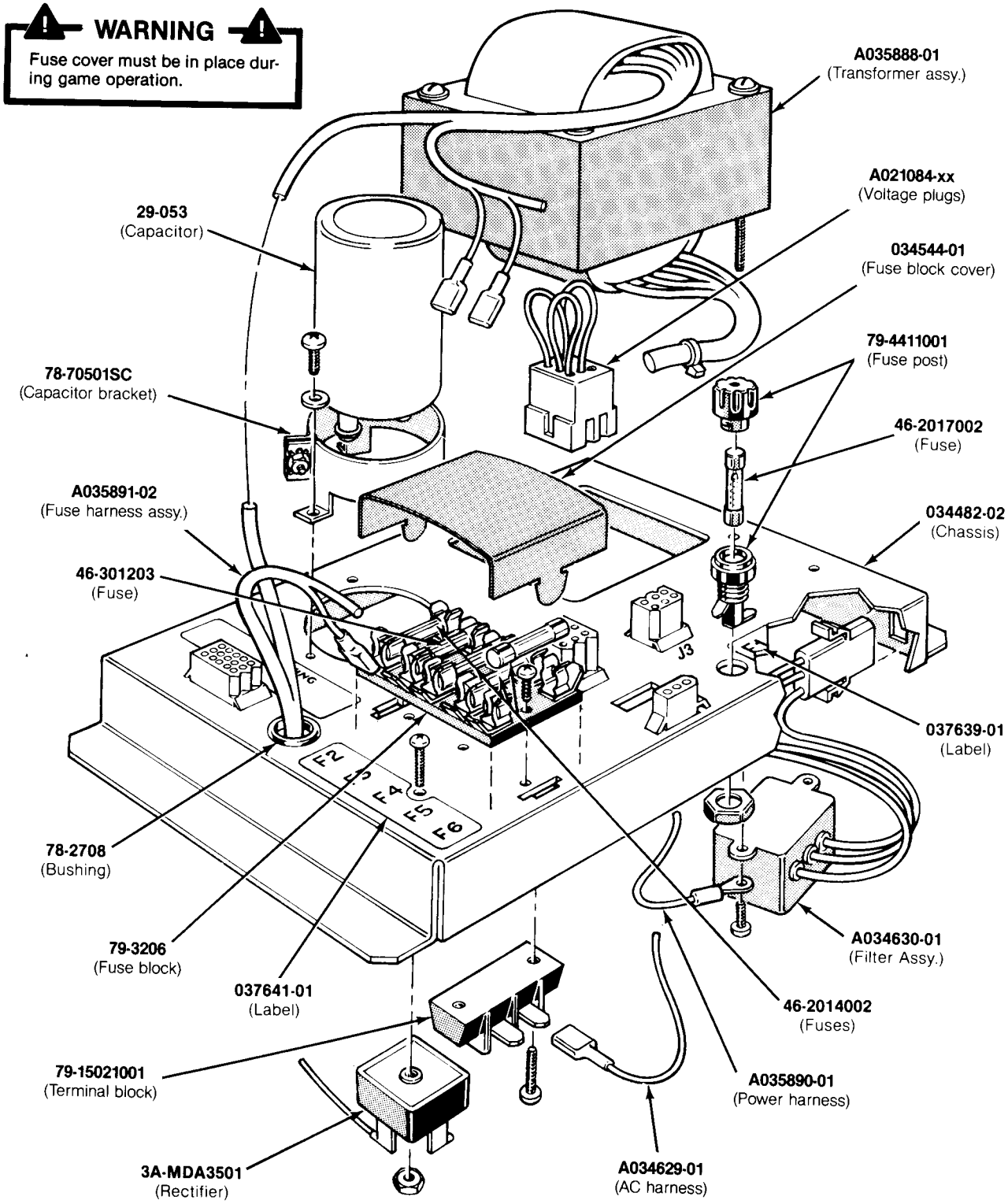


Figure 3-14 Power Supply Assembly A037671-01 and -02 C

Power Supply Assembly
Parts List

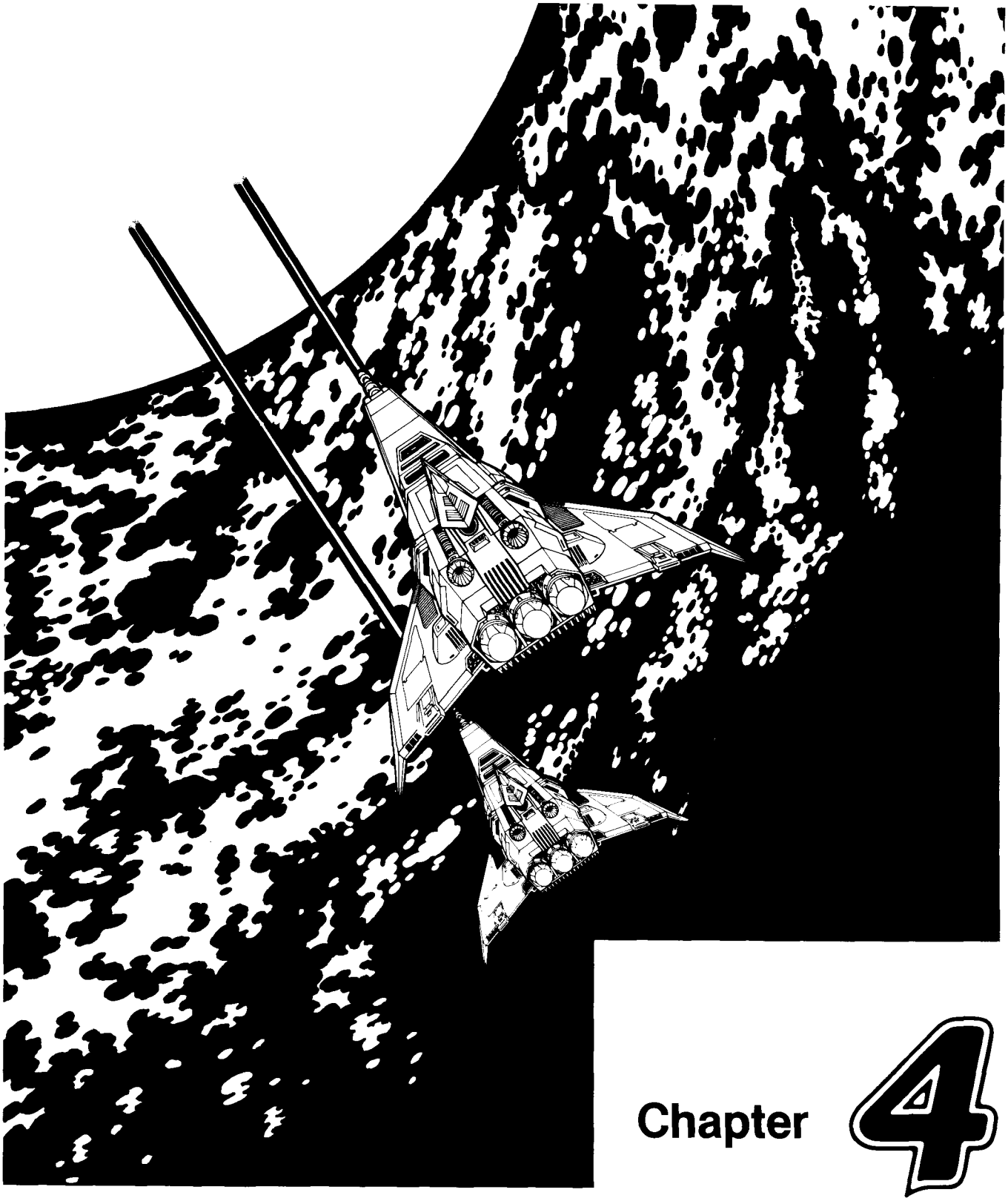
Part No.	*Description*
A021084-01	Voltage Plug for 100 V (90-110 VAC) *(violet wire color—plugs into* **J3***)*
A021084-02	Voltage Plug for 120 V (105-135 VAC) *(yellow wire color—plugs into* **J3***)**
A021084-04	Voltage Plug for 220 V (200-240 VAC) *(blue wire color—plugs into* **J3***)*
A021084-05	Voltage Plug for 240 V (220-260 VAC) *(brown wire color—plugs into* **J3***)*
A034629-01	AC Harness Assembly **(J4A)**
A034630-01	RFI Filter Assembly **(FL1**—*designation not marked)*
A035888-01	Transformer Assembly **(T1**—*designation covered) (Acceptable substitute is part no. A035888-02)*
A035890-01	Power Harness Assembly **(J2)**
A035891-02	Fuse Harness Assembly **(F2-F6)**
29-053	27,000 μF, 15 VDC Electrolytic Capacitor **(C1)**
3A-MDA3501	Type-MDA 3501 Bridge Rectifier **(CR1)**
46-2014002	4 A, 250 V, 3AG Slow-Blow Glass Cartridge-Type Fuse **(F2, F4-F6)**
46-2017002	7 A, 250 V, 3AG Slow-Blow Glass Cartridge-Type Fuse **(F1)**
46-301203	20 A, 32 V, 3AG Slow-Blow Glass Cartridge-TypeFuse **(F3)**
78-2708	Nylon Type 6/6 Hole Bushing with ⅝-Inch Inside Diameter x $\frac{5}{64}$-Inch Outside Diameter x ¼-Inch Thick
78-70501SC	2-Inch Diameter Capacitor Mounting Bracket **(C1)**
79-15021001	2-Circuit Single-Row Terminal Block *(located under* **F4***)*
79-3206	5-Position 3AG Fuse Block with ¼-Inch Quick-Disconnect Terminals **(F2-F6)**
79-4411001	Panel-Mounting Non-Indicating 3AG Cartridge-Type Fuse Post **(F1)**
034482-02	Power Supply Chassis Base
034544-01	Fuse Block Cover **(F2-F6)**
037243-01	Metal Base Plate *(not shown in illustration)*
037639-01	Label for Fuse Value **(F1)**
037641-01	Label for Fuse Values **(F2-F6)**

**This is the only plug provided on the North American power supply.*

NOTE

A037671-01 power supply assembly has the 120 V plug.
A037671-02 has the 100 V, 220 V, and 240 V plugs.
A037671-03 has the 220 V and 240 V plugs.

Glossary of Terms



Chapter 4

Glossary of Terms

AC Alternating current; from zero it rises to a maximum positive level, then passes through zero again to a maximum negative level.

ACTIVE STATE The true state of a signal. For example: The active state for $\overline{\text{START}}$ is low.

ADDRESS A value that identifies a specific location of data in memory; normally expressed in hexadecimal notation.

ANALOG Measurable in an absolute quantity (as opposed to on or off). Examples of analog devices are volume controls, light dimmers, and stereo amplifiers.

ANODE The positive (arrow) end of a diode.

AMPLIFIER A device used to increase the strength of an applied signal.

AMPLITUDE The maximum instantaneous value of a waveform pulse from zero.

ASTABLE Having no normal state. An astable device will free-run or oscillate as long as operating voltage is applied. The oscillation frequency is usually controlled by external circuitry.

AUXILIARY COIN SWITCH
A momentary-contact pushbutton switch with a black cap. It is located on the utility panel. The auxiliary coin switch adds credits to the game without activating the coin counter.

BEZEL A cut, formed, or machined retention device, such as the conical device used to mount a pushbutton switch to a control panel, or the formed device used to frame the video display screen.

BIDIRECTIONAL Able to send or receive data on the same line (e.g., the data bus of a microprocessor).

BINARY A number system that expresses all values by using the two digits 0 and 1.

BIT A binary digit; expressed as a 1 or a 0.

BLANKING Turning off the beam on a cathode-ray tube during retrace.

BLOCK DIAGRAM
A drawing in which functional circuitry units are represented by blocks. Very useful during initial troubleshooting.

BUFFER
1. An isolating circuit designed to eliminate the reaction of a driven circuit on the circuits driving it (e.g., a buffer amplifier).
2. A device used to supply additional drive capability.

BUS An electrical path over which information is transferred from any of several sources to any of several destinations.

CAPACITOR A device capable of storing electrical energy. A capacitor blocks the flow of DC current while allowing AC current to pass.

CATHODE The negative end of a diode.

CHIP An integrated circuit comprising many circuits on a single wafer slice.

CLOCK A repetitive timing signal for synchronizing system functions.

COINCIDENCE Occurring at the same time.

COIN COUNTER
A 6-digit electro-mechanical device that counts the coins inserted in the coin mechanism(s).

COIN MECHANISM
A device on the inside of the coin door that inspects the coin to determine if the correct coin has been inserted.

COMPLEMENTARY
Having opposite states, such as the outputs of a flip-flop.

COMPOSITE SYNC
Horizontal and vertical synchronization pulses that are bused together into a single signal. This signal provides the timing necessary to keep the display in synchronization with the game circuitry.

COMPOSITE VIDEO
Complete video signal from the game system to drive the display circuitry, usually comprising H SYNC, V SYNC, and the video.

CREDIT One play for one person based on the game switch settings.

CRT Cathode-ray tube.

DATA General term for the numbers, letters, and symbols that serve as input for device processing.

DARLINGTON A two-transistor amplifier that provides extremely high gain.

DC Direct current, meaning current flowing in one direction and of a fixed value.

DEFLECTION YOKE
Electromagnetic coils around the neck of a cathode-ray tube. One set of coils deflects the electron beam horizontally, and the other set deflects the beam vertically.

DIAGNOSTICS A programmed routine for checking circuitry. For example: The **self-test** is a diagnostic routine.

DIODE A semiconductor device that conducts in only one direction.

DISCRETE Non-integrated components, such as resistors, capacitors, and transistors.

DMA Direct memory access. DMA is a process of accessing memory by bypassing the microprocessor logic. DMA is normally used for transferring data between the input/output ports and memory.

DOWN TIME The period during which a game is malfunctioning or not operating correctly due to machine failure.

LOGIC STATE The binary (1 or 0) value at the node of a logic element or integrated circuit during a particular time. Also called the logic level. The figures below show the voltage levels corresponding to the logic states (levels) in a TTL system.

LOGIC 0, LOW	{0 VDC to +0.8 VDC}
GREY AREA (TRI-STATE LEVEL)	{+0.8 VDC to +2.4 VDC}
LOGIC 1, HIGH	{+2.4 VDC to +5 VDC}

MULTIPLEXER A device that takes several low-speed inputs and combines them into one high-speed data stream for simultaneous transmission on a single line.

NMI Non-maskable interrupt. NMI is a request for service by the microprocessor from external logic. The microprocessor cannot ignore this interrupt request.

PAGE A subsection of memory. A read-only memory device (see ROM) is broken into discrete blocks of data. These blocks are called pages. Each block has X number of bytes.

PCB The abbreviation for printed-circuit board.

PHOTOTRANSISTOR
A transistor that is activated by an external light source.

POTENTIOMETER
1. A resistor that has a continuously moving contact which is generally mounted on a moving shaft. Used chiefly as a voltage divider. Also called a POT (slang).
2. An instrument for measuring a voltage by balancing it against a known voltage.

RAM Random-access memory. A device for the temporary storage of data.

RASTER-SCAN DISPLAY
A display system whereby images are displayed by continuously scanning the cathode-ray tube horizontally and vertically with an electron beam. The display system controls the intensity of the electron beam.

RETRACE In a raster-scan display, retrace is the time during which the cathode-ray tube electron beam is resetting either from right to left or from bottom to top.

RESISTOR A device designed to have a definite amount of resistance. Used in circuits to limit current flow or to provide a voltage drop.

ROM Read-only memory. A device for the permanent storage of data.

SIGNATURE ANALYSIS
A process of isolating digital logic faults at the component level by means of special test equipment called signature analyzers. Basically, signature analyzers (e.g., the ATARI® CAT Box) convert lengthy bit streams into four digit hexadecimal signatures. The signature read by the analyzer at each circuit node is then compared with the known good signature for that node. This process continues until a fault is located.

TROUBLESHOOT
The process of locating and repairing a fault.

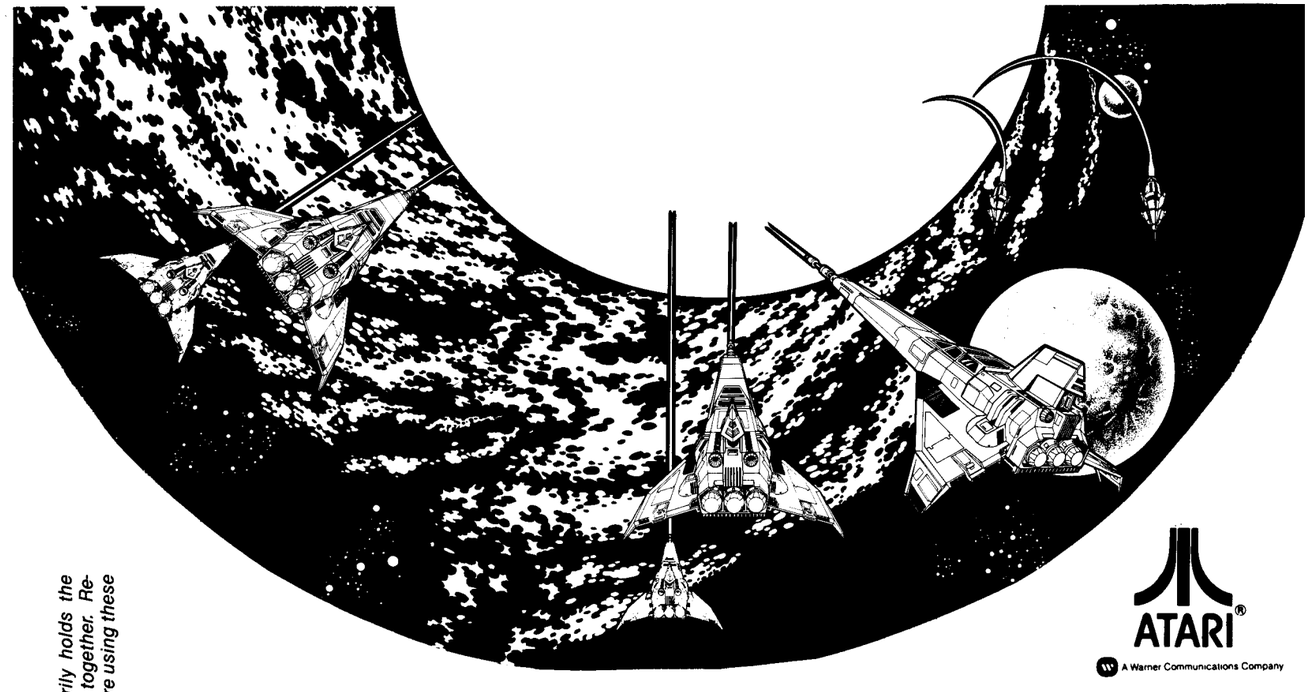
VECTOR A line segment drawn between specific X and Y coordinates on a cathode-ray tube.

WATCHDOG A counter circuit designed to protect the microprocessor from self-destruction if a program malfunction occurs. If a malfunction does occur, the counter applies continuous pulses to the reset line of the microprocessor, which causes the microprocessor to keep resetting.

X-Y DISPLAY A display system whereby images are displayed with vectors.

ZENER DIODE A special diode used as a regulator. Its main characteristic is breaking down at a specified reverse-bias (Zener) voltage.

Table of Contents



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NOTE
This staple temporarily holds the schematic package together. Remove the staple before using these schematics.

Schematic Package Supplement to

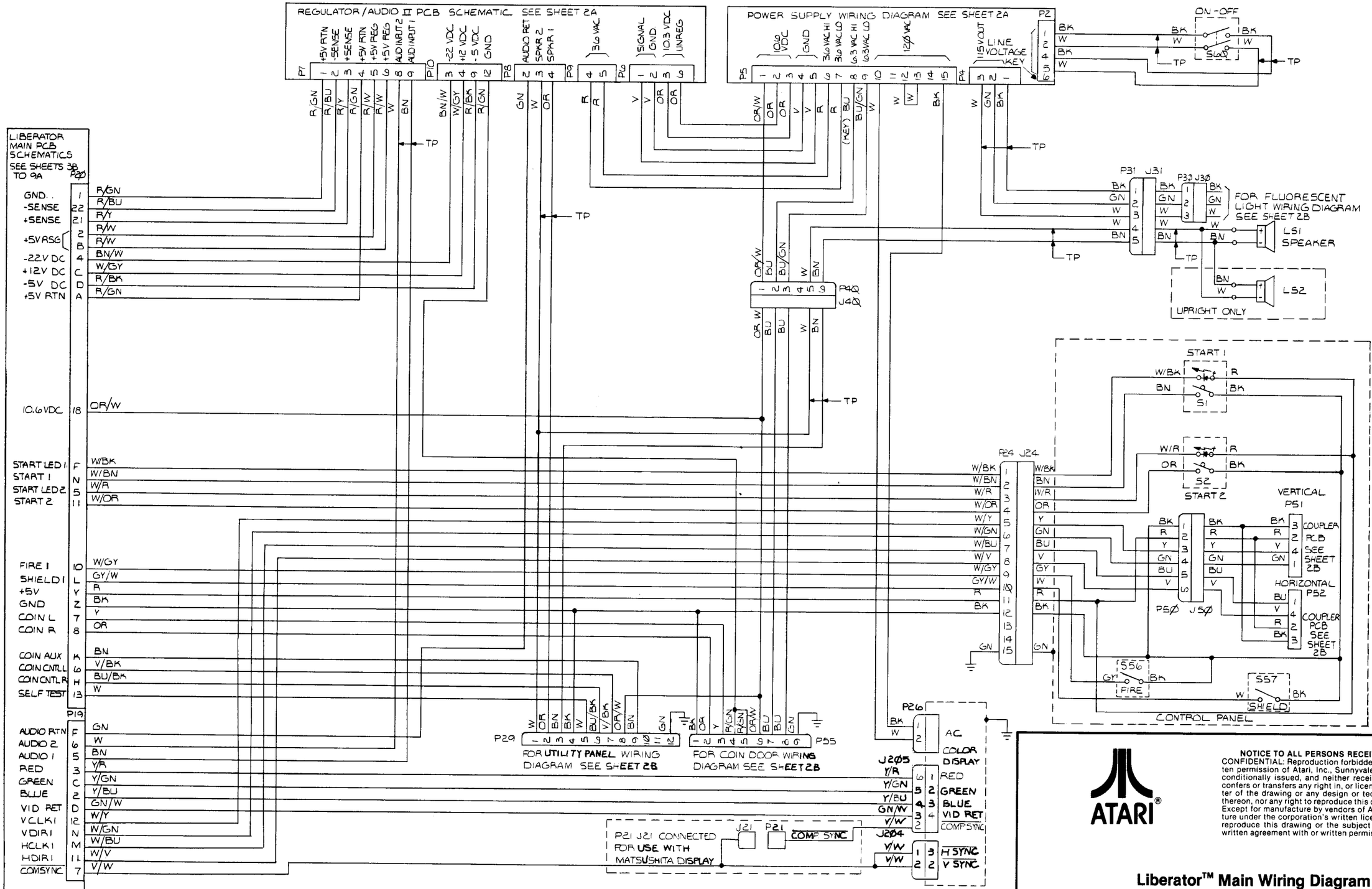
TM

LIBERATOR

Operation, Maintenance, and Service Manual

10L

SP-209 Sheet 1A
1st Printing



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Liberator™ Main Wiring Diagram

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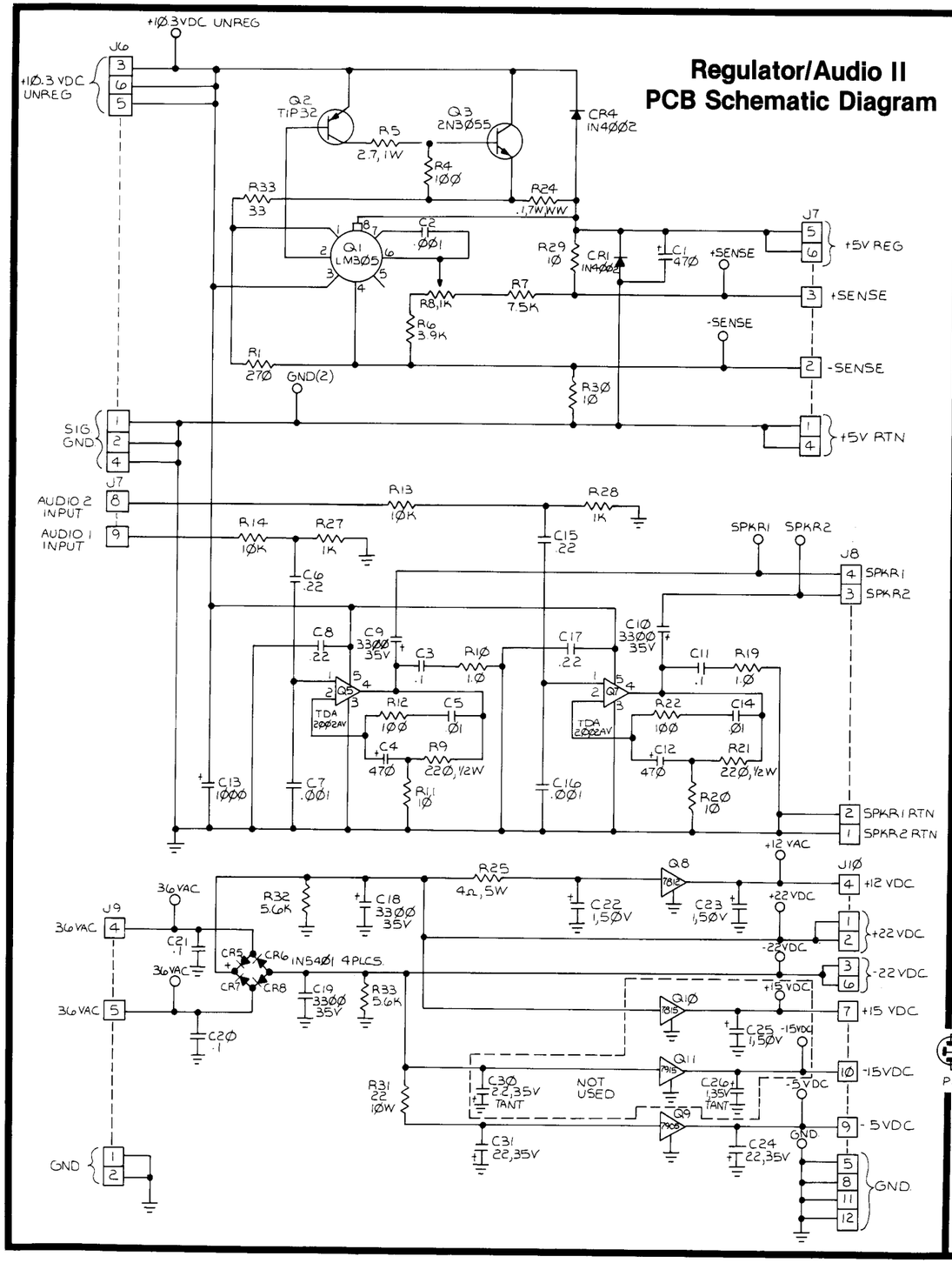
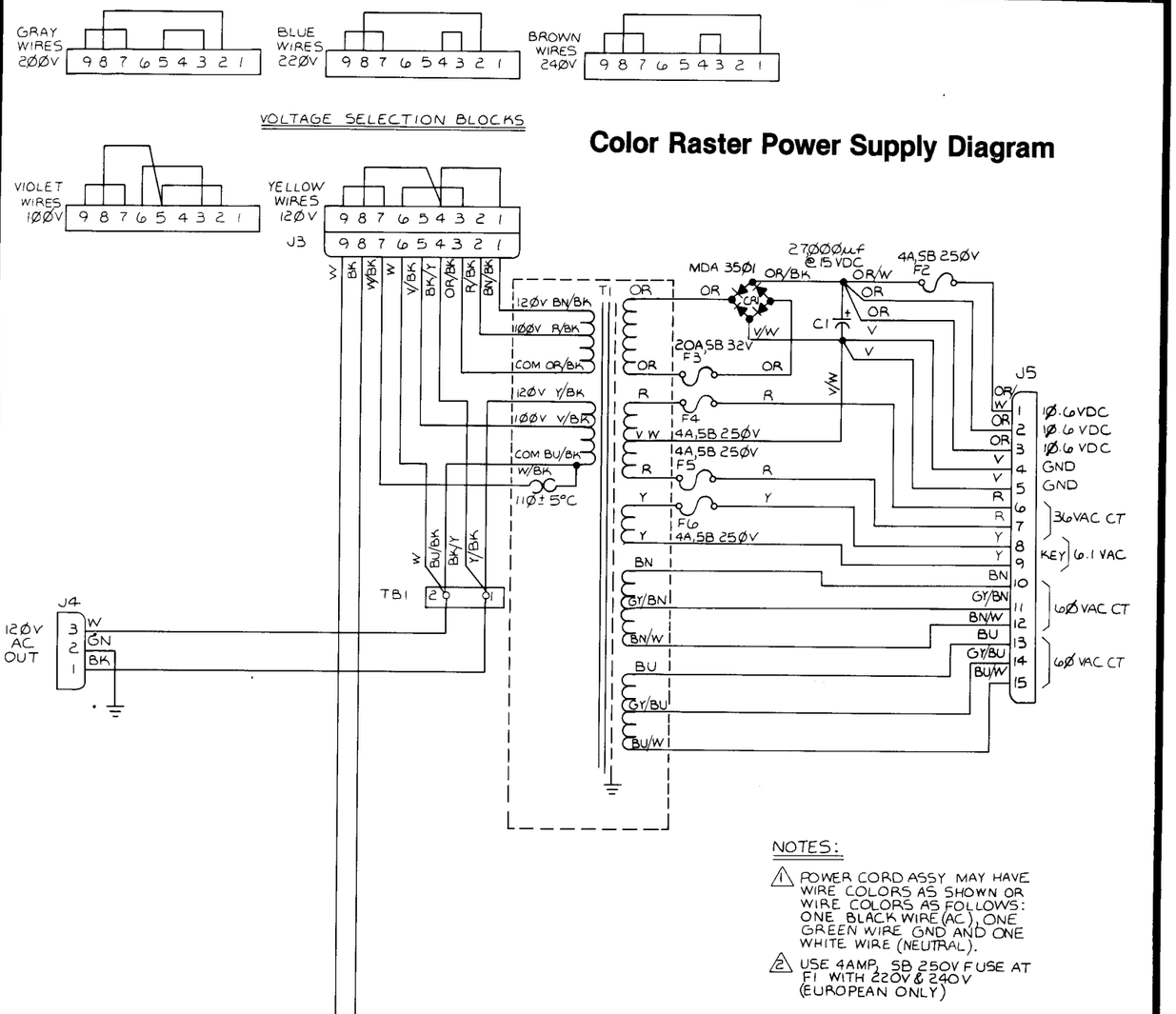
SP-209 Sheet 1B
1st Printing

Regulator/Audio II PCB Schematic Diagram



Color Raster Power Supply Diagram



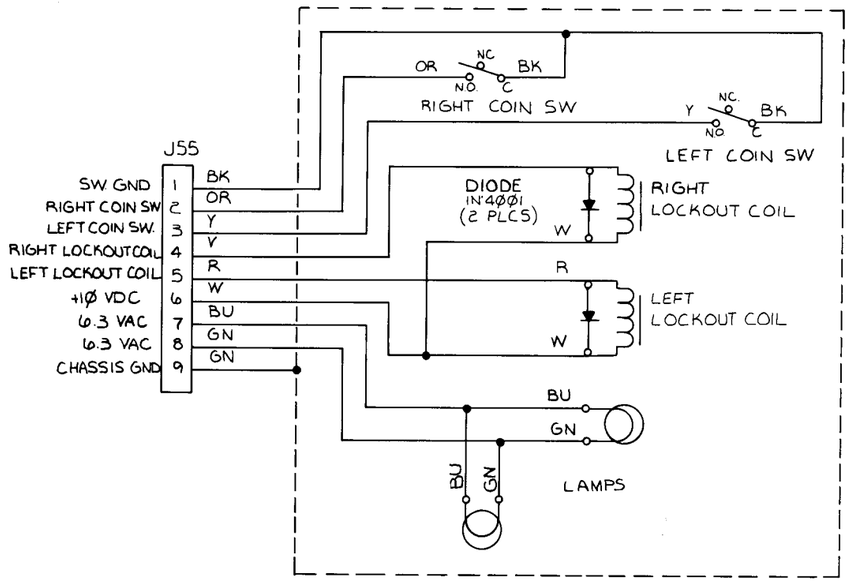
NOTES:

1. POWER CORD ASSY. MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE GND AND ONE WHITE WIRE (NEUTRAL).
2. USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY)

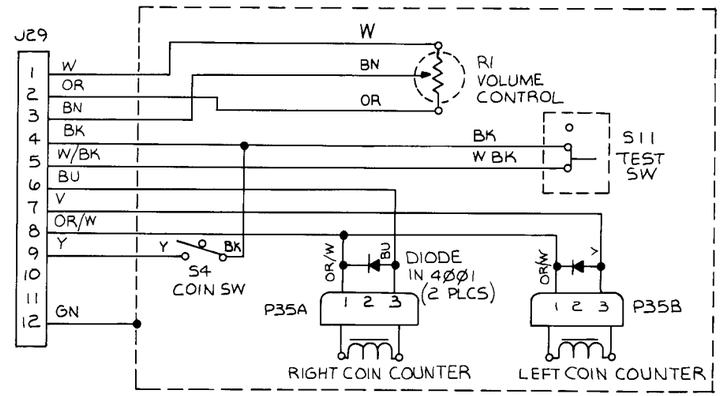
Liberator™ Reg./Audio II PCB and Power Supply Diagrams

SP-209 Sheet 2A
1st Printing

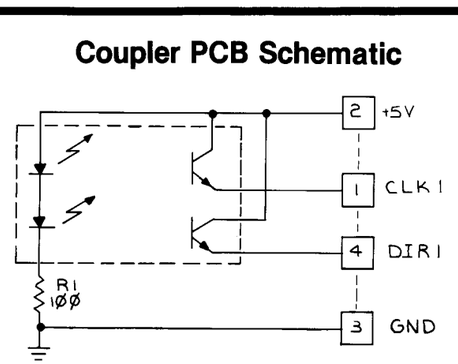
Coin-Door Wiring Diagram



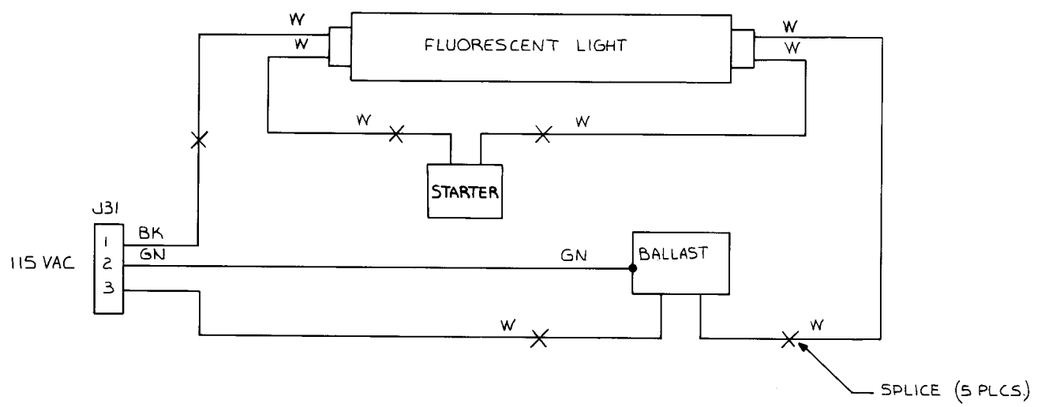
Utility Panel Wiring Diagram



Coupler PCB Schematic



Fluorescent Light Wiring Diagram



Liberator™ Game Wiring Interfaces

SP-209 Sheet 2B
1st Printing

MEMORY MAP

HEXA-DECIMAL ADDRESS	ADDRESS BUS A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		D	D	D	D	D	D	D	D	XCOORD
0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		D	D	D	D	D	D	D	D	YCOORD
0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0		D	D	D						BIT MODE DATA
0003-033F 0340-303F 3D40-3FFF	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	WORKING RAM SCREEN RAM WORKING RAM
4000	0	1	0	0	0												R	D	D	D	D	D	D	D	D	$\overline{\text{EARD}}$
5000	0	1	0	1	0											0	R								D	COIN AUX ($\overline{\text{CTRLD}}$ SET LOW)
																								D		COIN LEFT ($\overline{\text{CTRLD}}$ SET LOW)
																							D			COIN RIGHT ($\overline{\text{CTRLD}}$ SET LOW)
																						D				SLAM ($\overline{\text{CTRLD}}$ SET LOW)
																					D					SPARE ($\overline{\text{CTRLD}}$ SET LOW)
																				D						SPARE ($\overline{\text{CTRLD}}$ SET LOW)
																			D							COCKTAIL ($\overline{\text{CTRLD}}$ SET LOW)
																		D								SELF-TEST ($\overline{\text{CTRLD}}$ SET LOW)
																						D	D	D	D	HDIR ($\overline{\text{CTRLD}}$ SET HIGH)
																		D	D	D	D					VDIR ($\overline{\text{CTRLD}}$ SET HIGH)
5001	0	1	0	1	0											1	R								D	SHIELD 2
																								D		SHIELD 1
																							D			FIRE 2
																						D				FIRE 1
																					D					SPARE
																				D						START 2
																			D							START 1
																		D								VBLANK
6000-6000F	0	1	1	0	0	0	0							A	A	A	A	W					D	D	D	D	$\overline{\text{BASRAM}}$
6200-621F	0	1	1	0	0	0	1							A	A	A	A	W	D	D	D	D	D	D	D	D	$\overline{\text{COLORAM}}$
6400	0	1	1	0	0	1	0											W									$\overline{\text{INTACK}}$
6600	0	1	1	0	0	1	1											W					D	D	D	D	EARCON
6800	0	1	1	0	1	0	0											W	D	D	D	D	D	D	D	D	$\overline{\text{STARTLG}}$
6A00	0	1	1	0	1	0	1											W									$\overline{\text{WDOG}}$
6C00	0	1	1	0	1	1	0									0	0	W				D					START LED 1
6C01																0	1	W				D					START LED 2
6C02																1	0	W				D					$\overline{\text{TBSWP}}$
6C03																1	1	W				D					SPARE
6C04																0	0	W				D					$\overline{\text{CTRLD}}$
6C05																0	1	W				D					COINCNTRR
6C06																1	1	W				D					COINCNTRL
6C07																1	1	W				D					PLANET
6E00-6E3F	0	1	1	0	1	1	1							A	A	A	A	W	D	D	D	D	D	D	D	D	$\overline{\text{EARWR}}$
7000-701F	0	1	1	1	0									A	A	A	A		D	D	D	D	D	D	D	D	$\overline{\text{IOS2}}$
7800-781F	0	1	1	1	1									A	A	A	A		D	D	D	D	D	D	D	D	$\overline{\text{IOS1}}$
8000-EFFF	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	ROM

Schematic Reference Designators and Symbols

Logic symbols depict the logic function performed by that particular device and may differ from the manufacturer's data.

REFERENCE DESIGNATORS:

C	Capacitor
CR	Diode, signal or rectifier
F	Fuse
J	Connector
L	Inductor, fixed or variable
LS	Speaker
P	Connector
Q	Transistor or silicon-controlled rectifier
R	Resistor, fixed or variable
S	Switch
T	Transformer
TP	Twisted wire pair
VR	Voltage regulator
Y	Crystal

WIRE COLORS:

R	Red
GN	Green
Y	Yellow
W	White
BU	Blue
BN	Brown
BK	Black
OR	Orange
V	Violet
GY	Gray

Electrical components shown on the schematic diagrams are in the following units unless otherwise noted:

Capacitors = microfarads (μf)
Resistors = ohms (Ω)
Inductors = microhenrys (μh)

SYMBOLS:

Ground

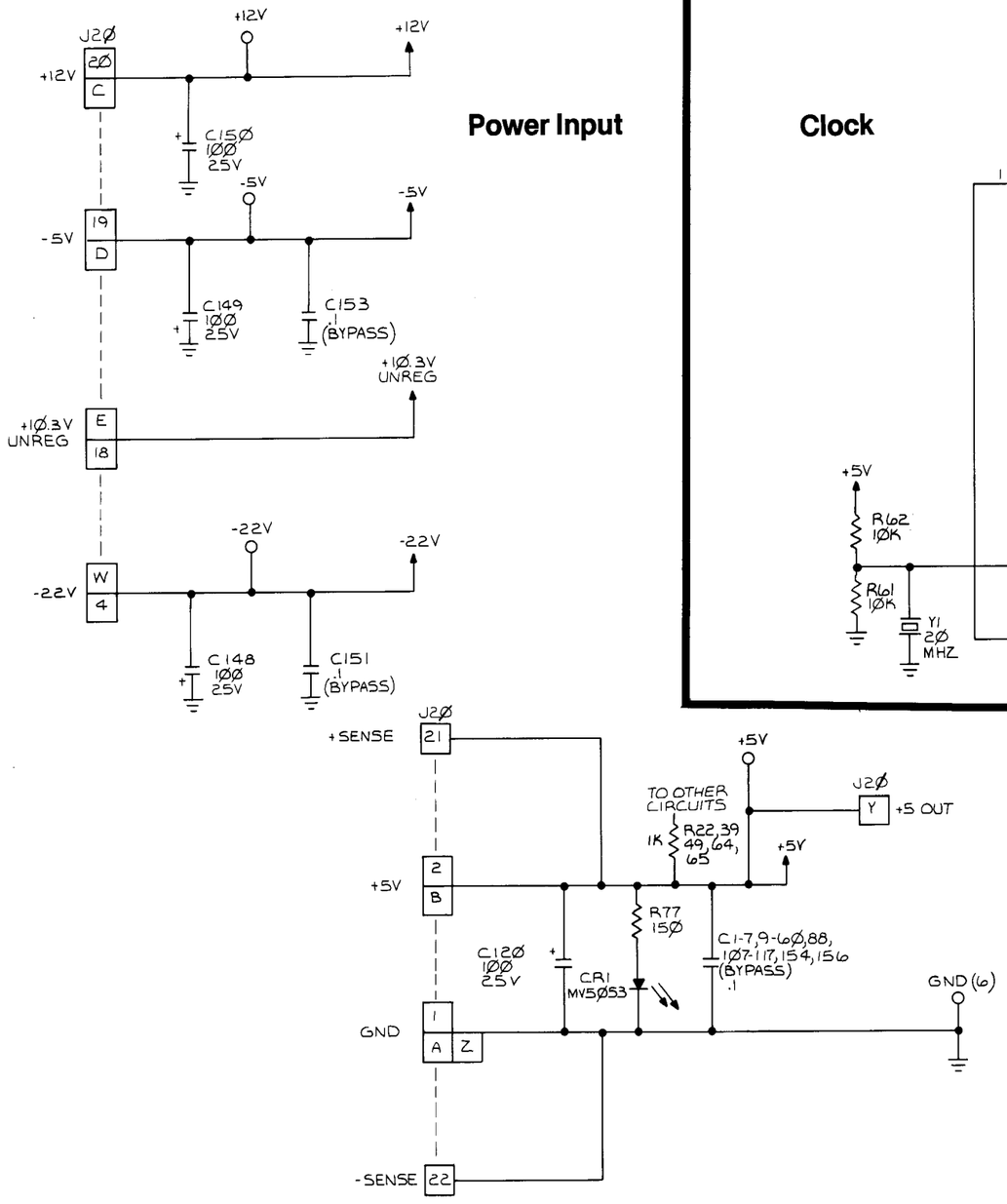
Test Point

PCB edge connector pad

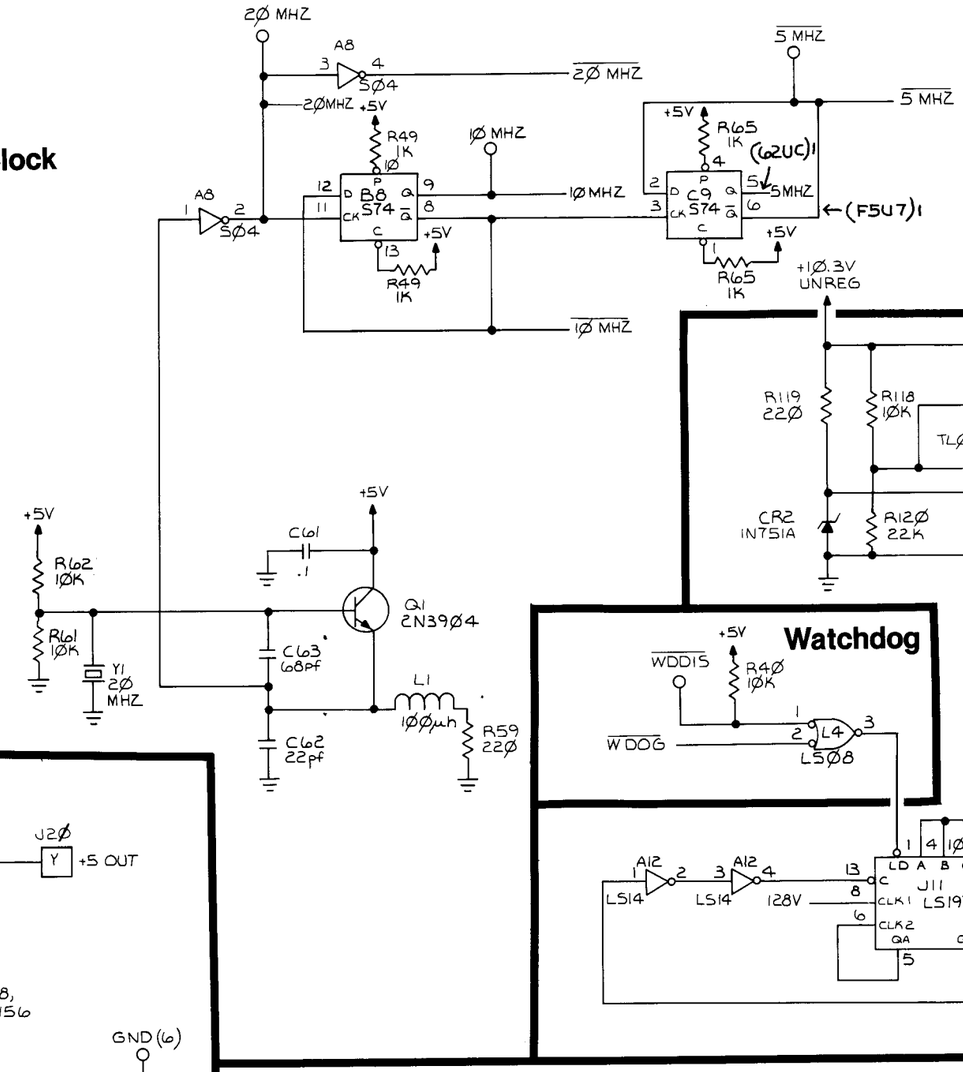
PCB test connector pad

Liberator™ Memory Map and Schematic Notes

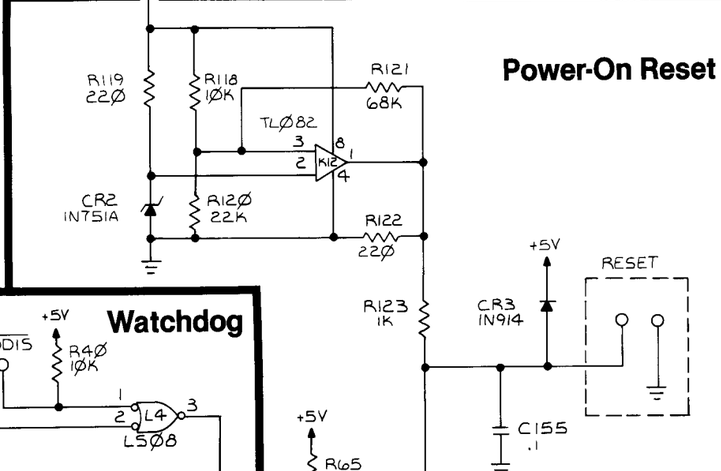
Power Input



Clock



Power-On Reset



Watchdog

NOTE

To avoid faulty readings while testing signatures, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the entire test.

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Liberator™ PCB Schematic Diagram

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SP-209 Sheet 3B
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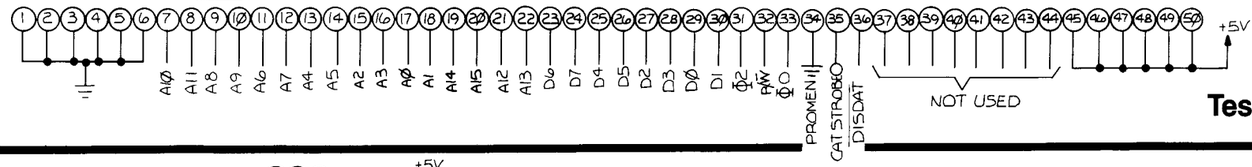
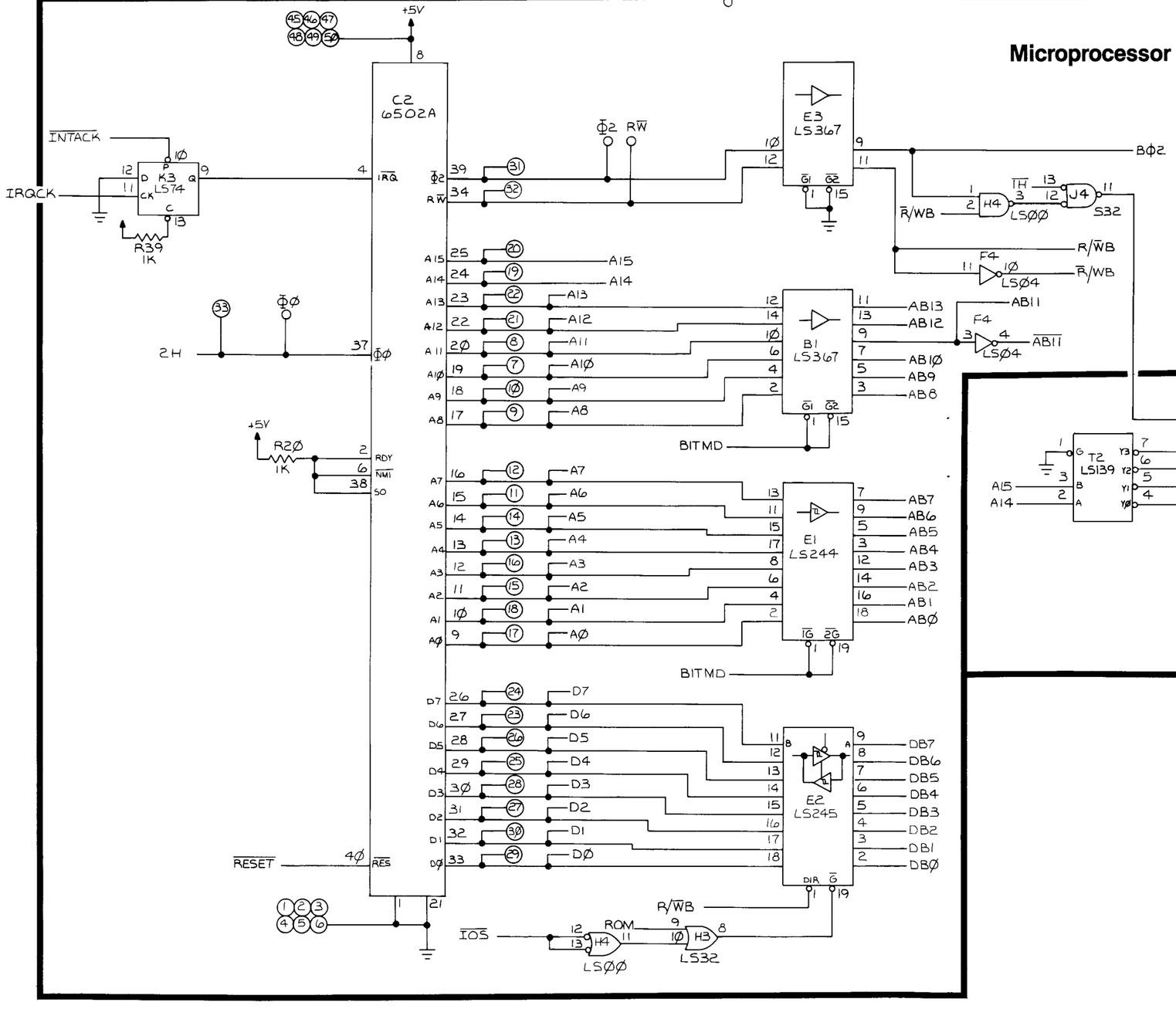
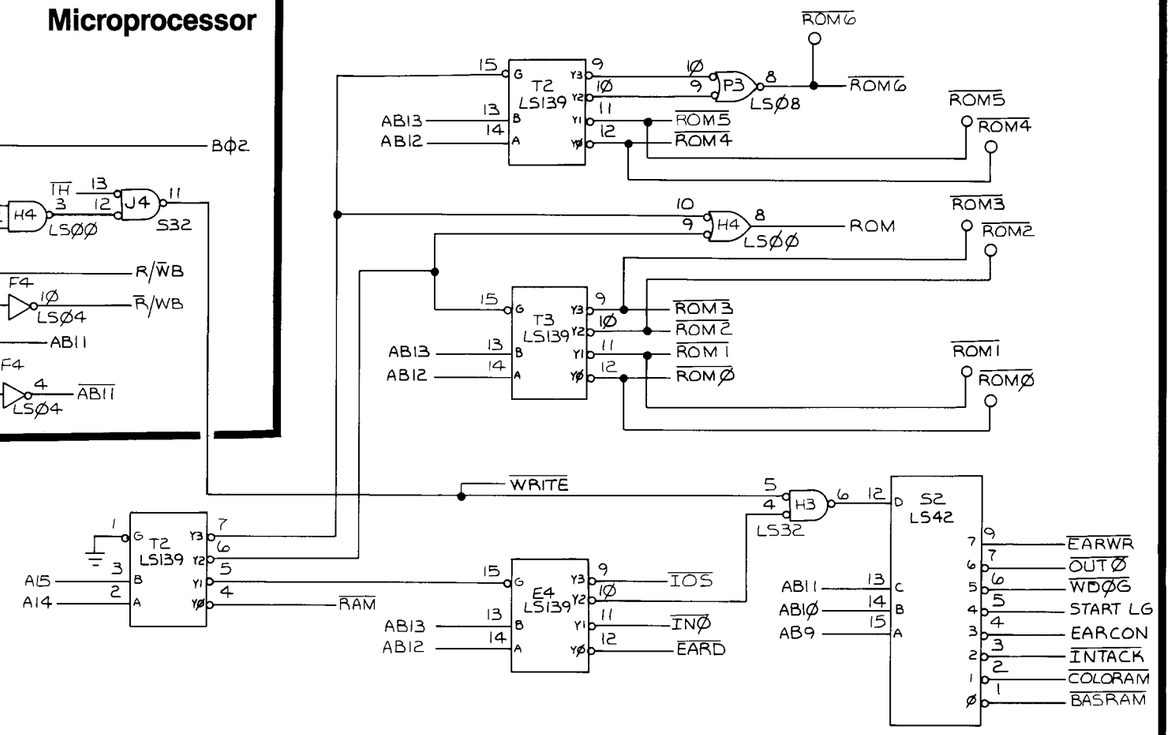
Test Connector



Microprocessor



Address Decoders



Liberator™ PCB Schematic Diagram

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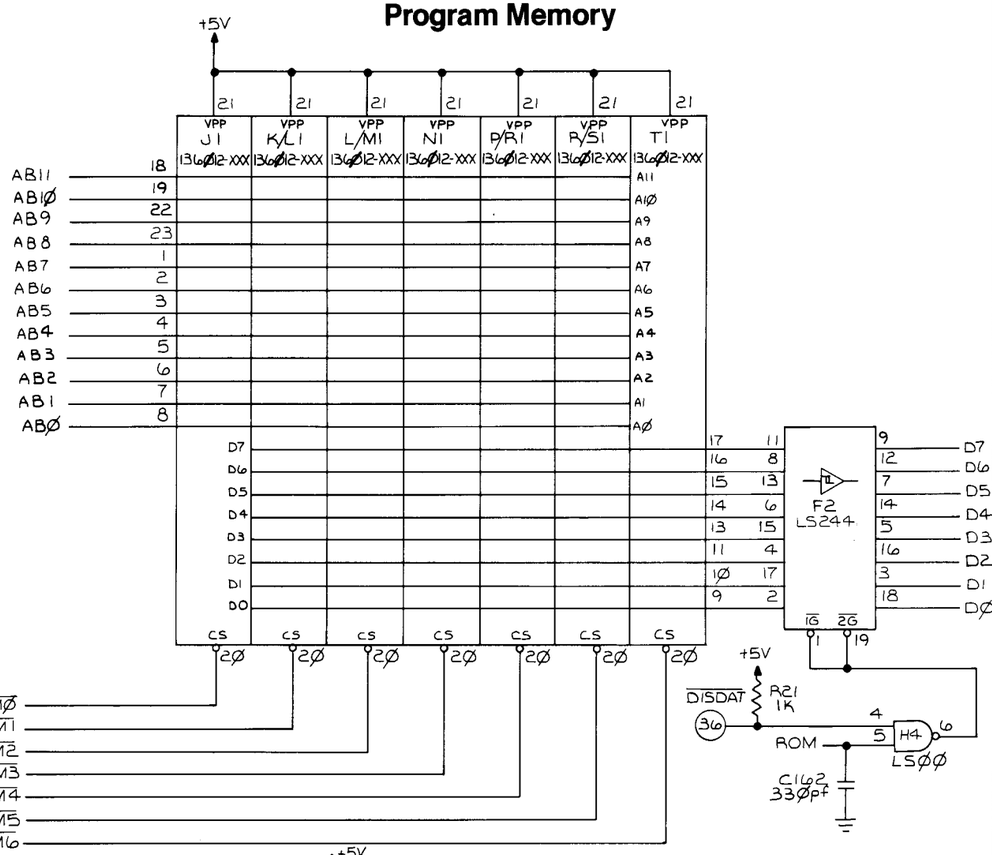
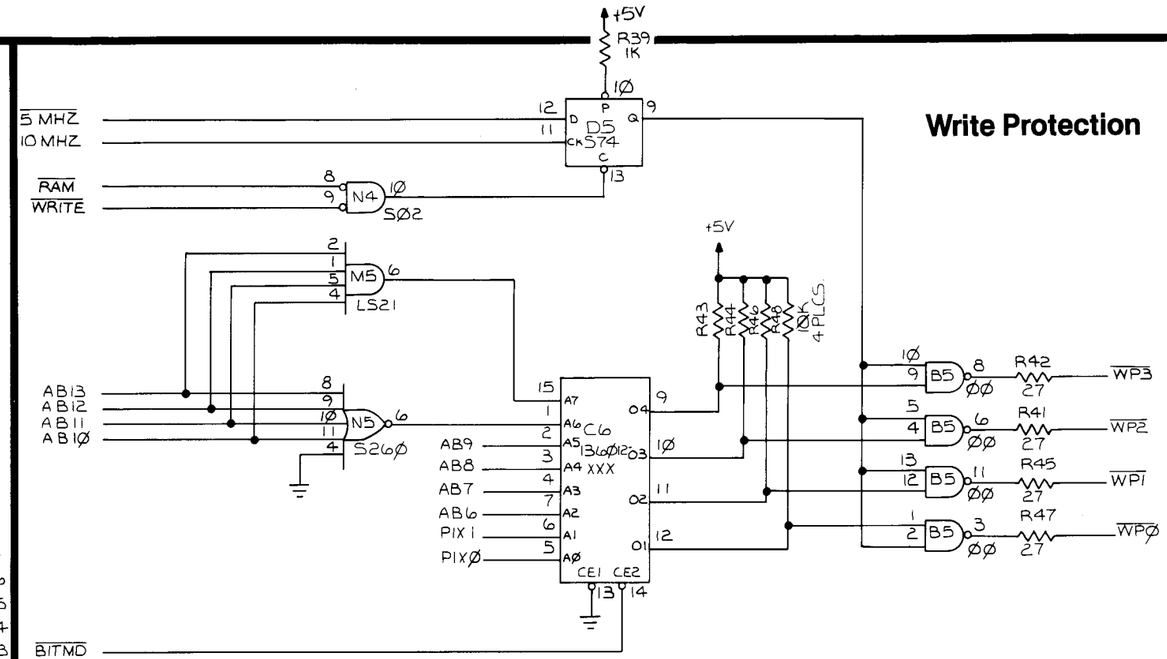
1st Printing

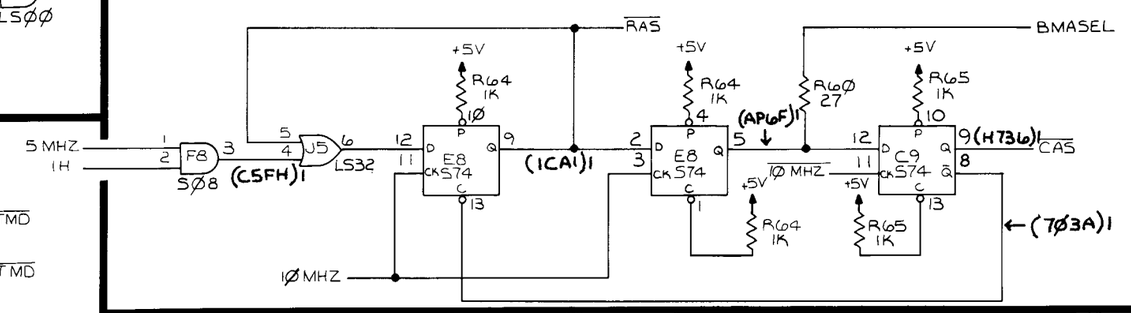
Program Memory



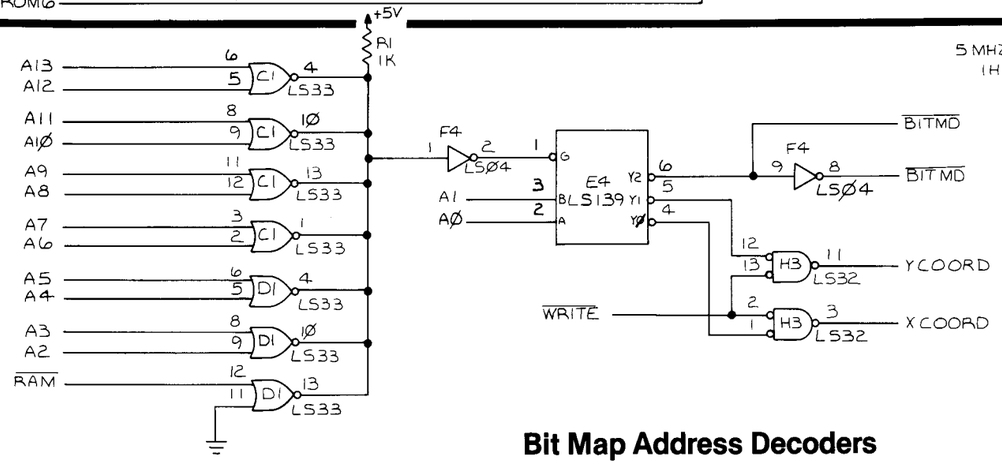
Write Protection



Refresh



Bit Map Address Decoders



NOTE

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Liberator™ PCB Schematic Diagram

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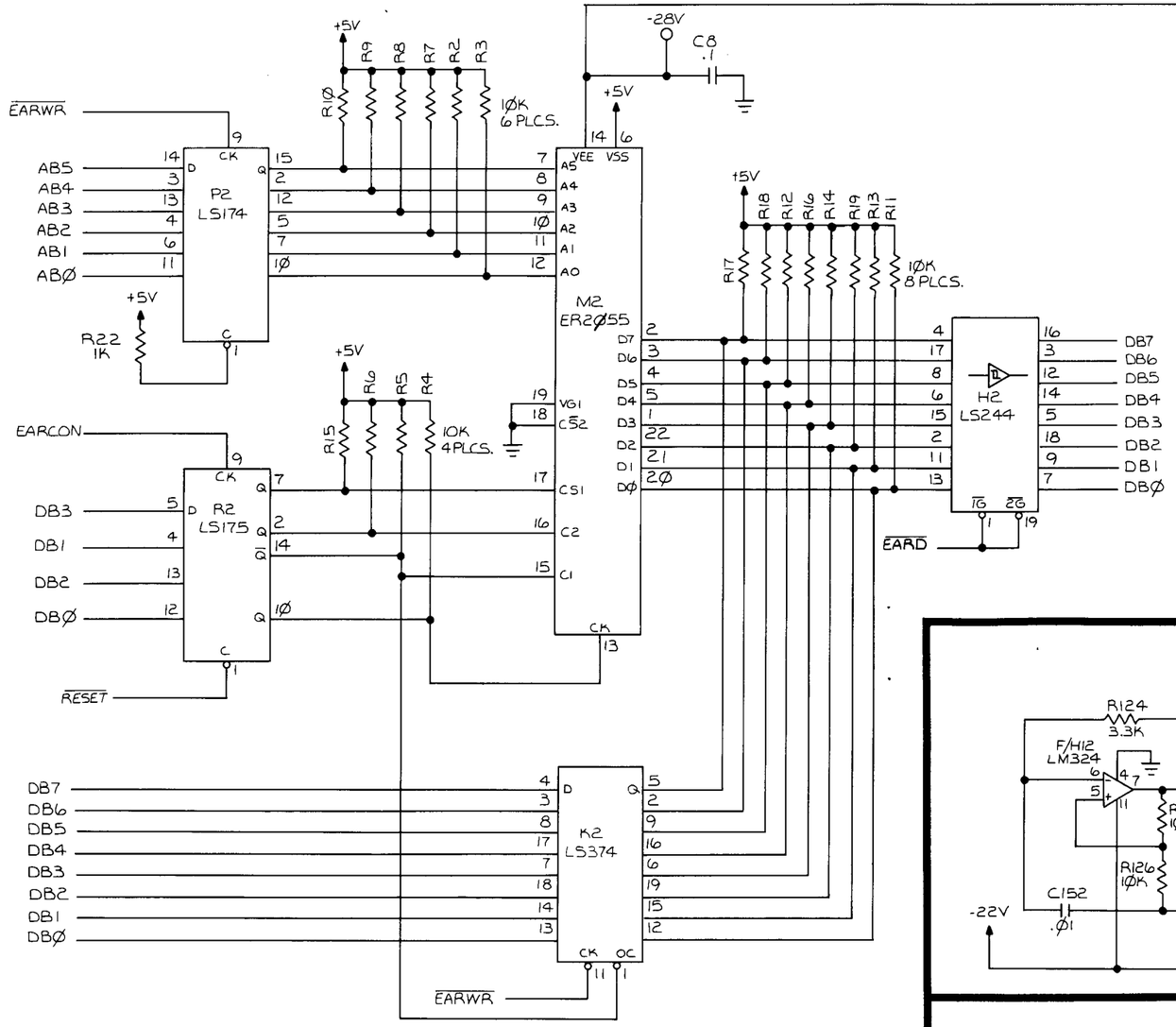
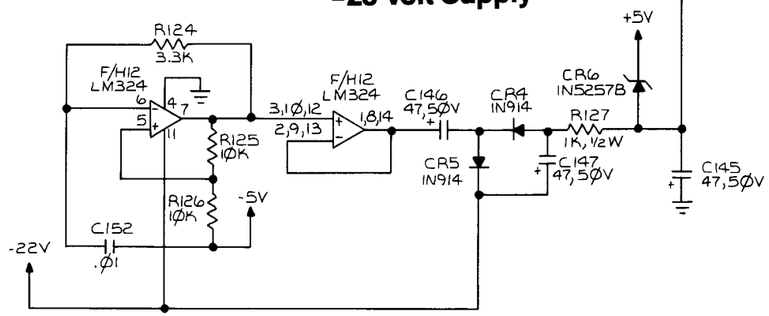
SP-209 Sheet 4B

1st Printing

EAROM



-28 Volt Supply



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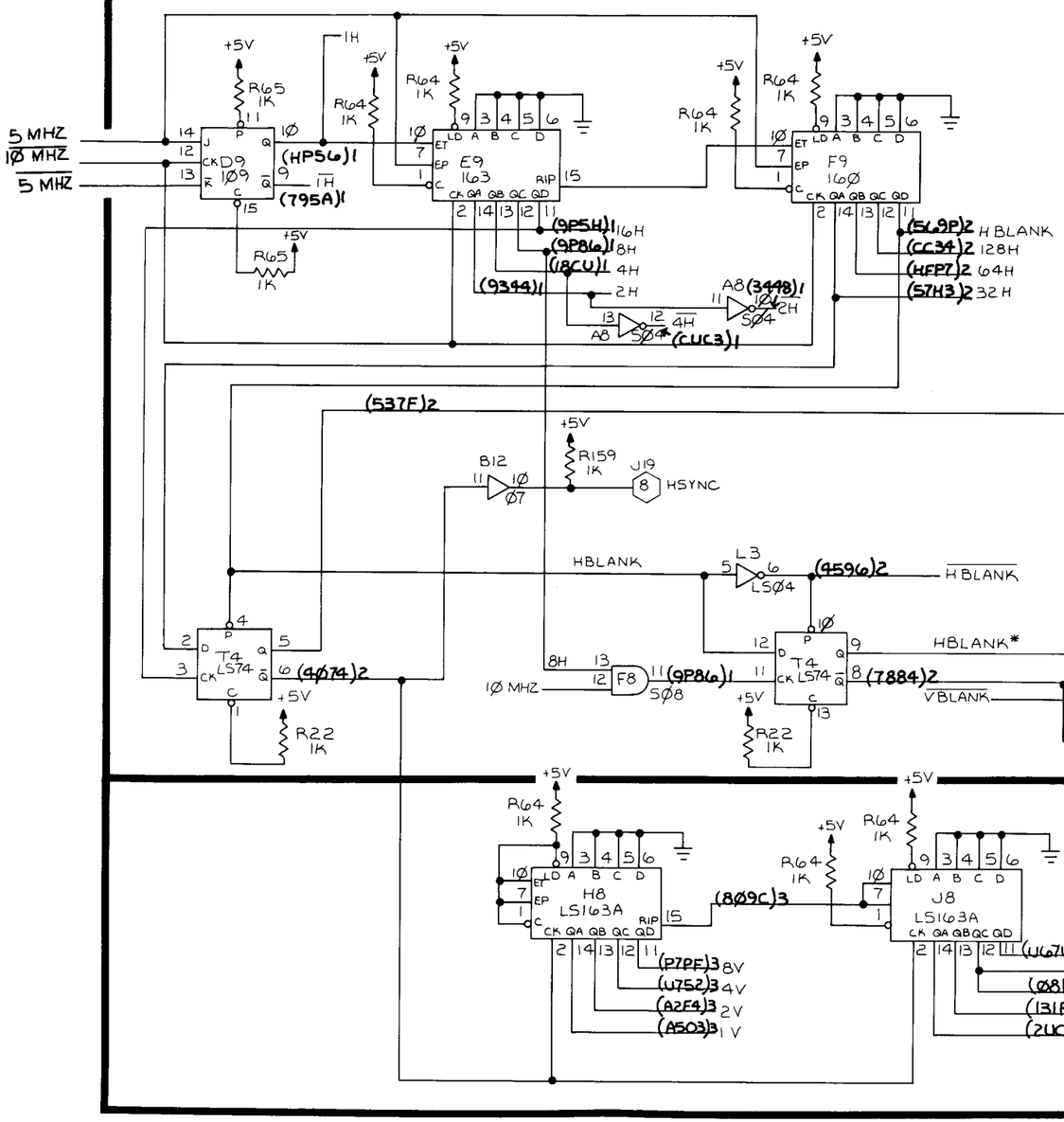
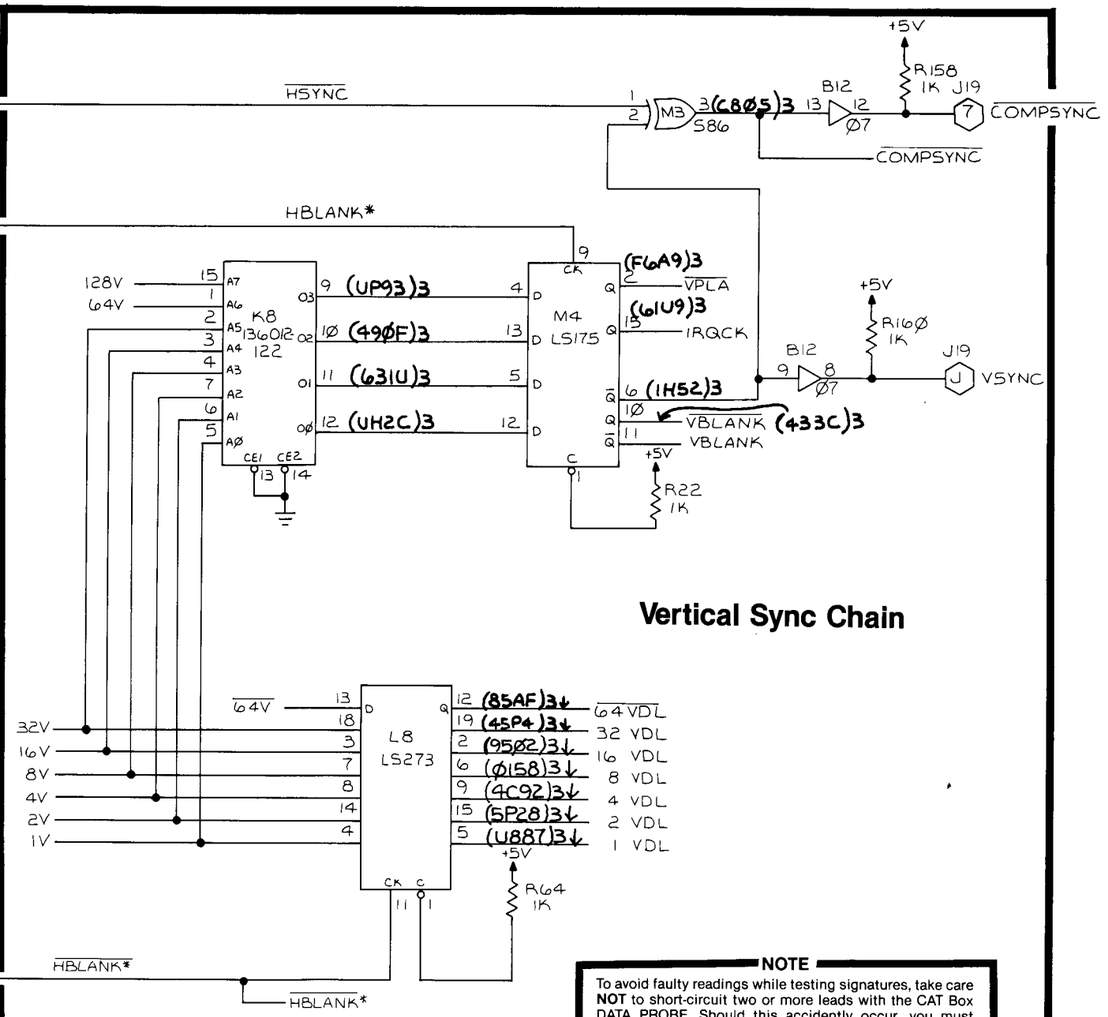
Liberator™ PCB Schematic Diagram

SP-209 Sheet 5A
1st Printing

Horizontal Sync Chain



Vertical Sync Chain



NOTE

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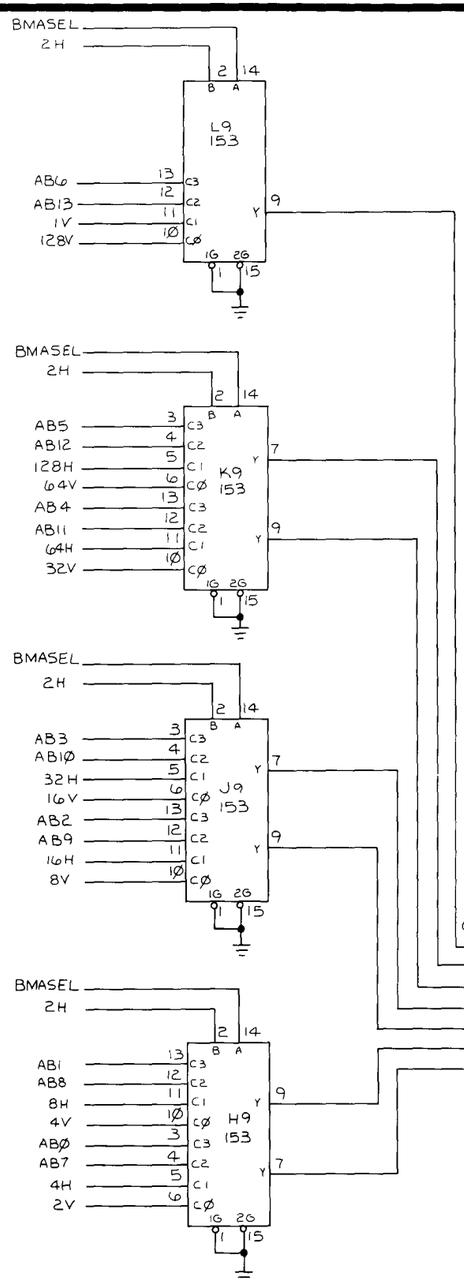
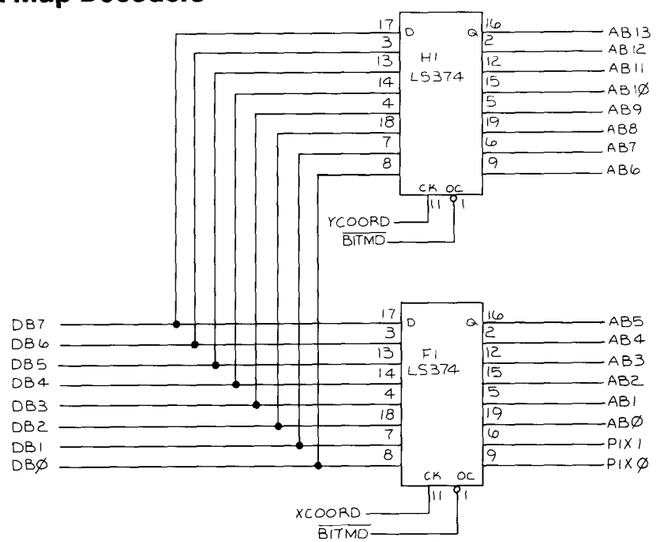
Liberator™ PCB Schematic Diagram

SP-209 Sheet 5B
1st Printing

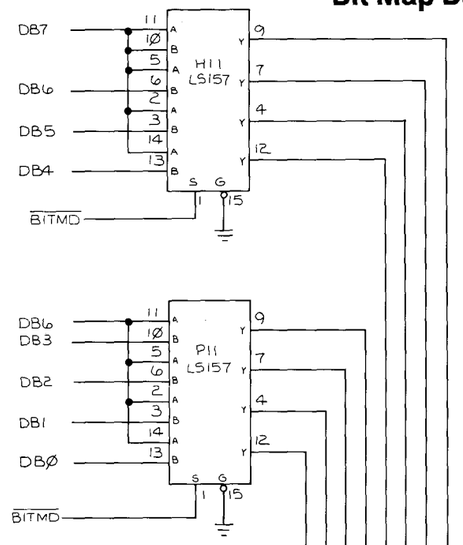
Bit Map Address Multiplexers



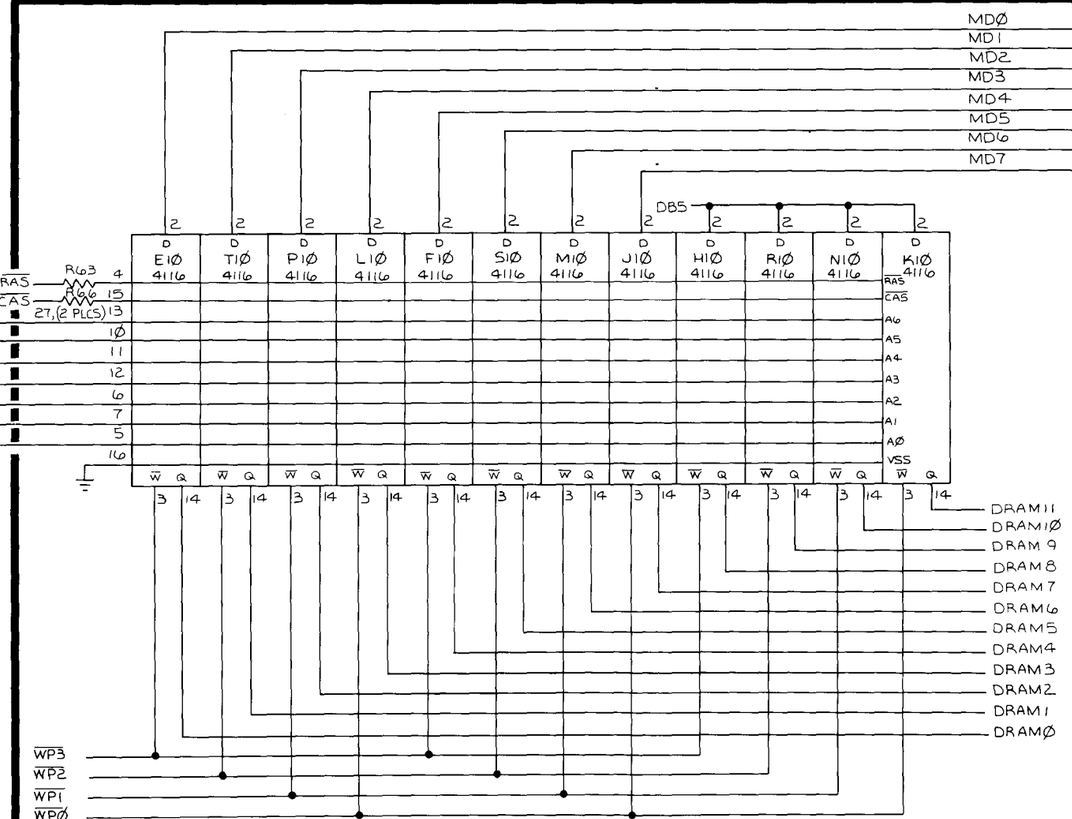
Bit Map Decoders



Bit Map Data Multiplexers



Bit Map Memory



Liberator™ PCB Schematic Diagram

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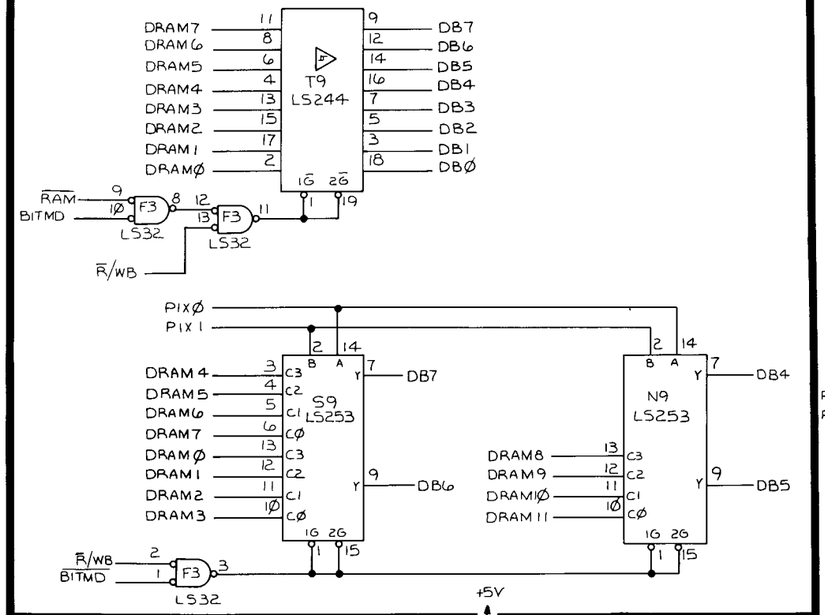
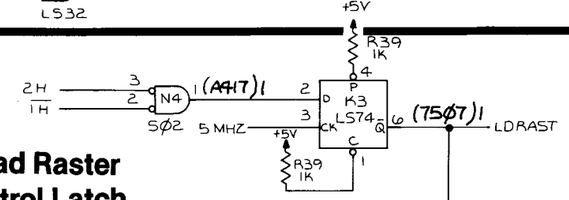
1st Printing

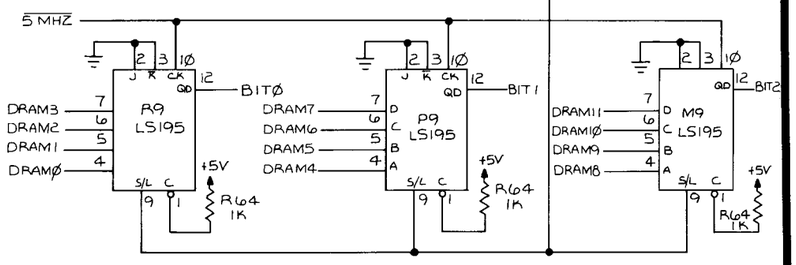
Bit Map Data Buffers



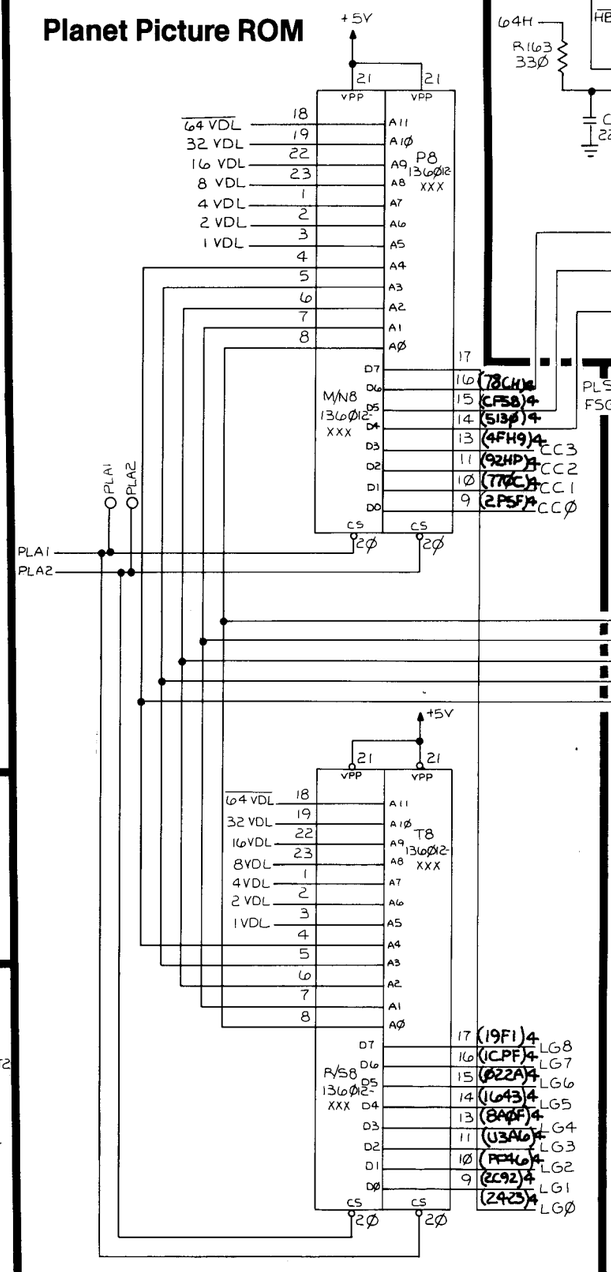
Load Raster Control Latch



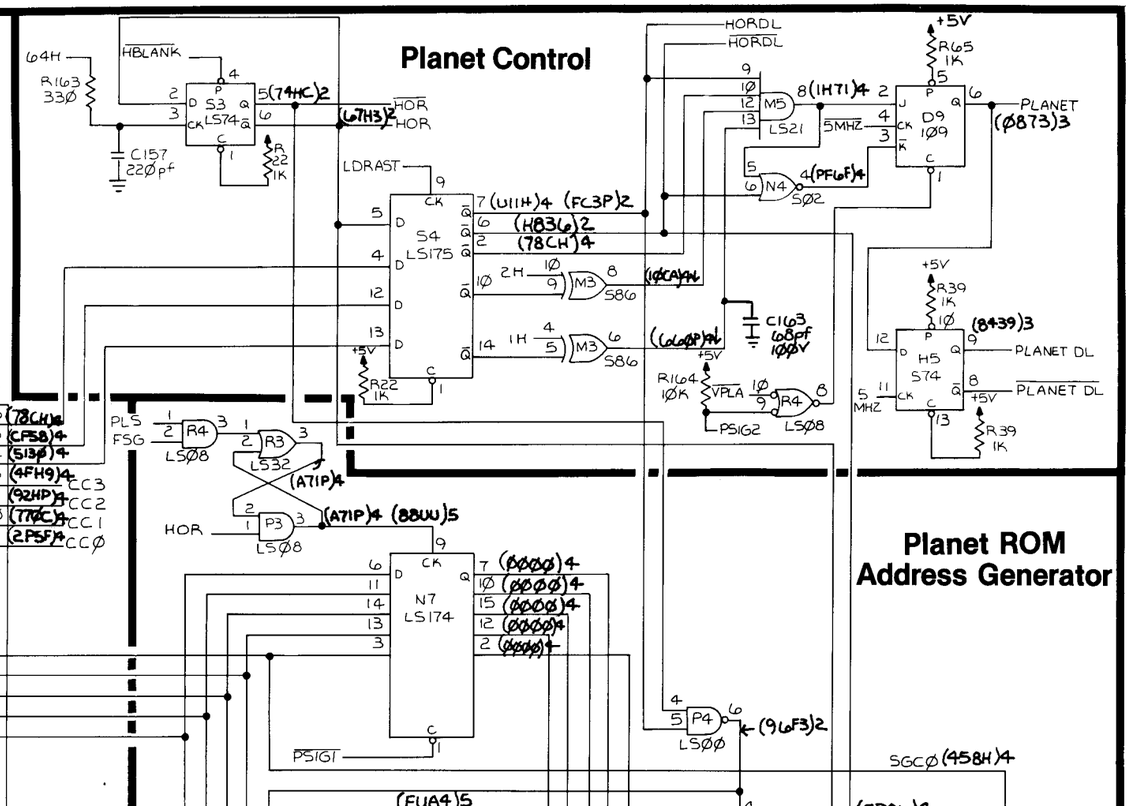
Bit Map Shift Registers



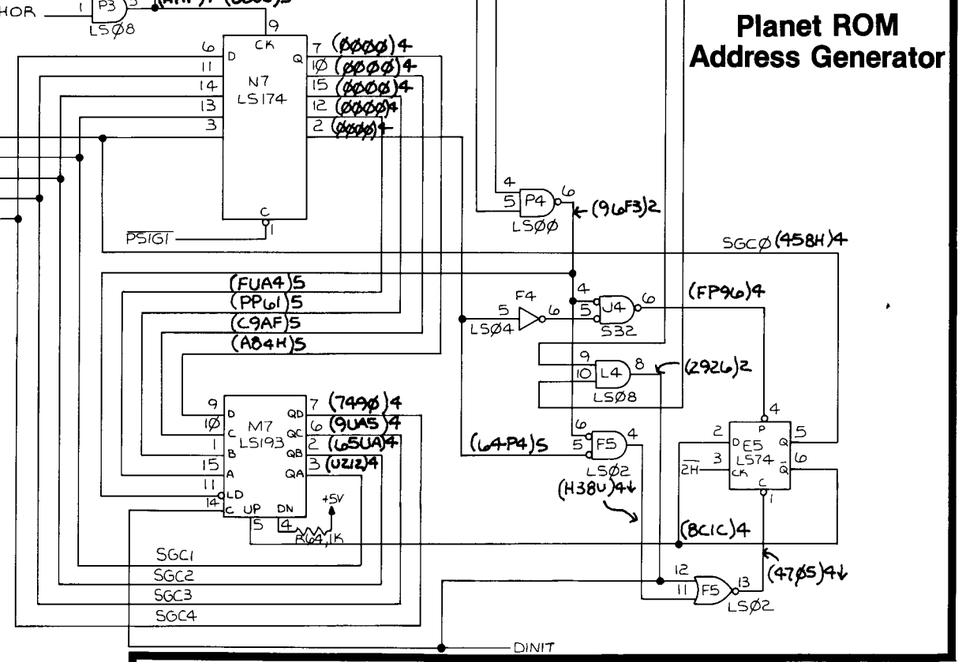
Planet Picture ROM



Planet Control



Planet ROM Address Generator



NOTE

To avoid faulty readings while testing signatures, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the entire test.

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Liberator™ PCB Schematic Diagram

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SP-209 Sheet 6B
1st Printing

Longitude Scaling

Multiplier

Multiply Clock

Latitude Scaling

NOTE

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Liberator™ PCB Schematic Diagram

Line Buffer Address Controller

Line Buffer

Valid Segment Detector

Base RAM

NOTE

To avoid faulty readings while testing signatures, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the entire test.

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Liberator™ PCB Schematic Diagram

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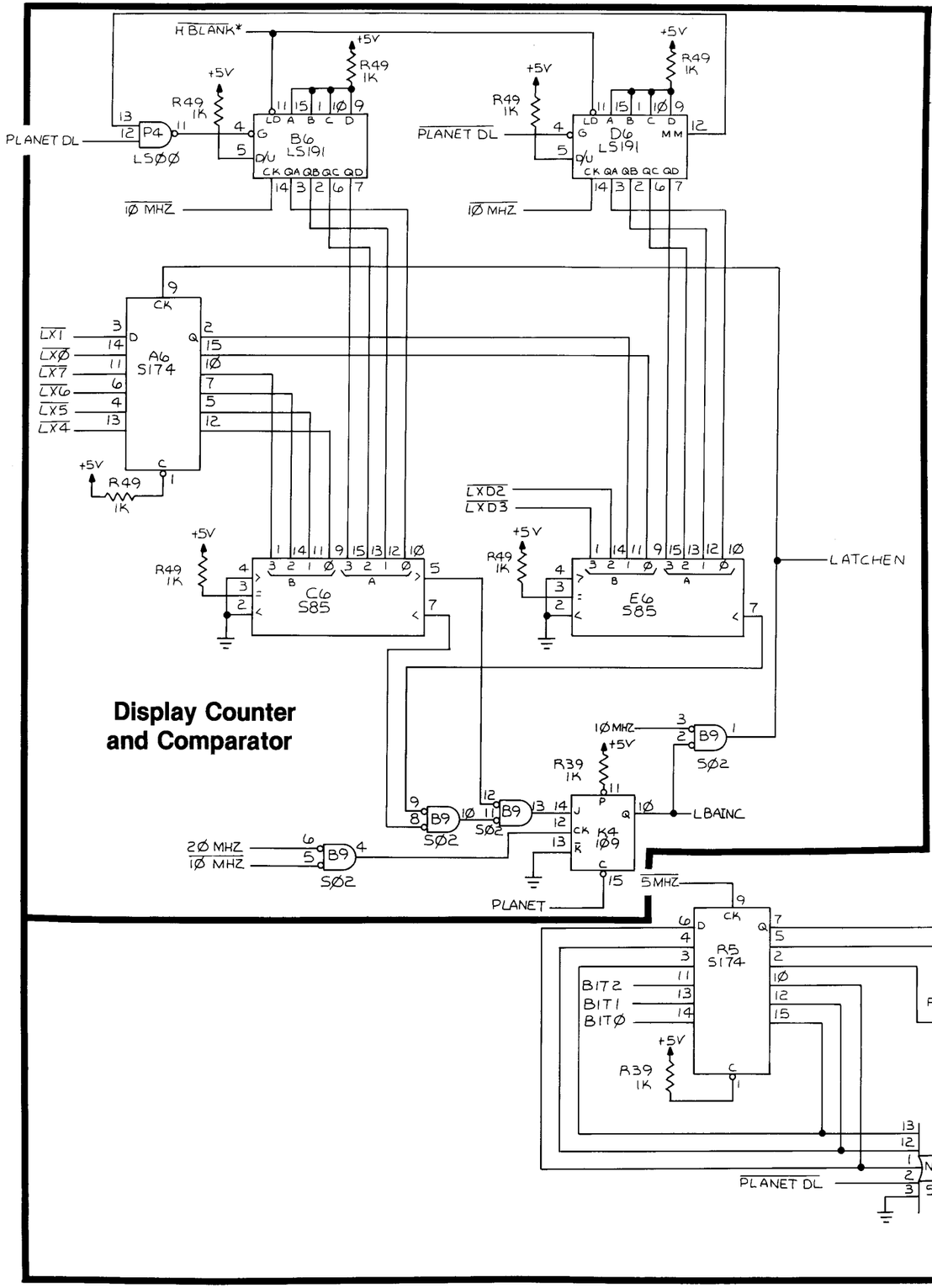
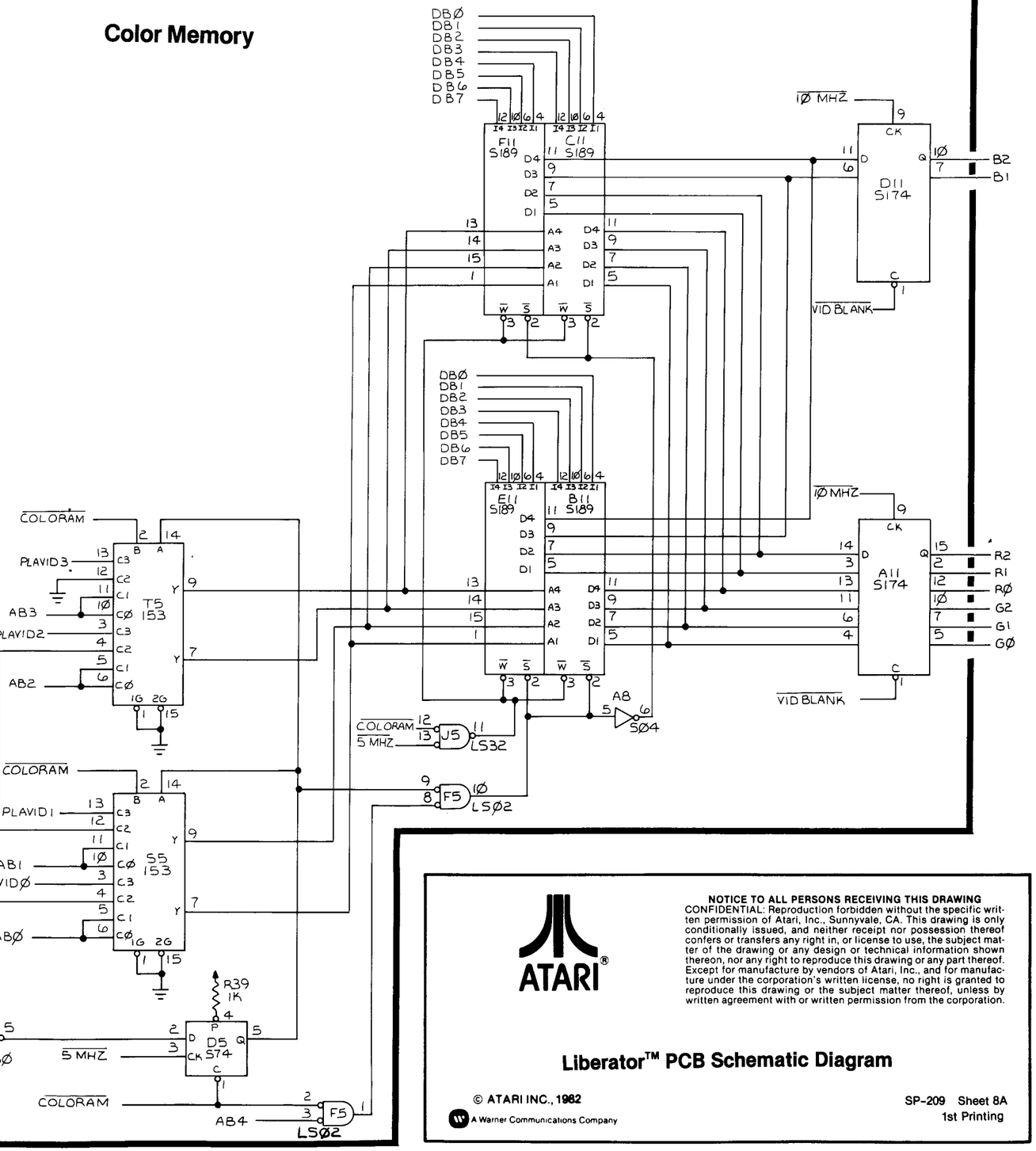
1st Printing

Display Counter and Comparator



Color Memory



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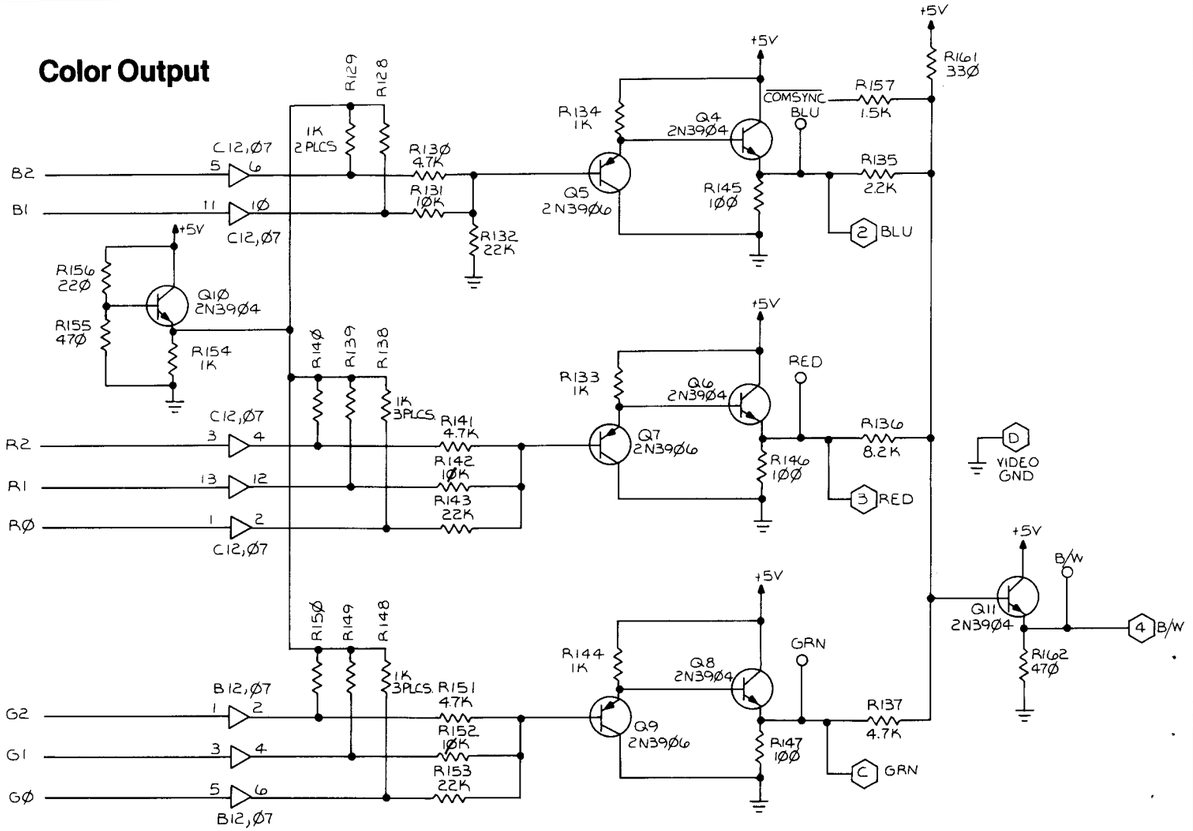
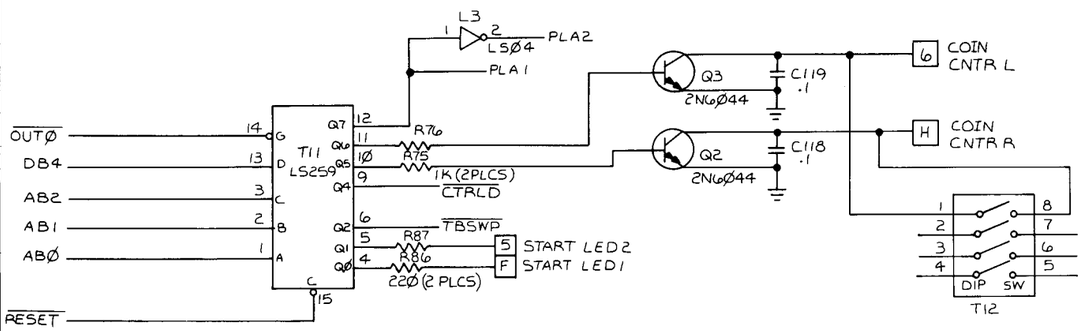
Liberator™ PCB Schematic Diagram

SP-209 Sheet 8A
1st Printing

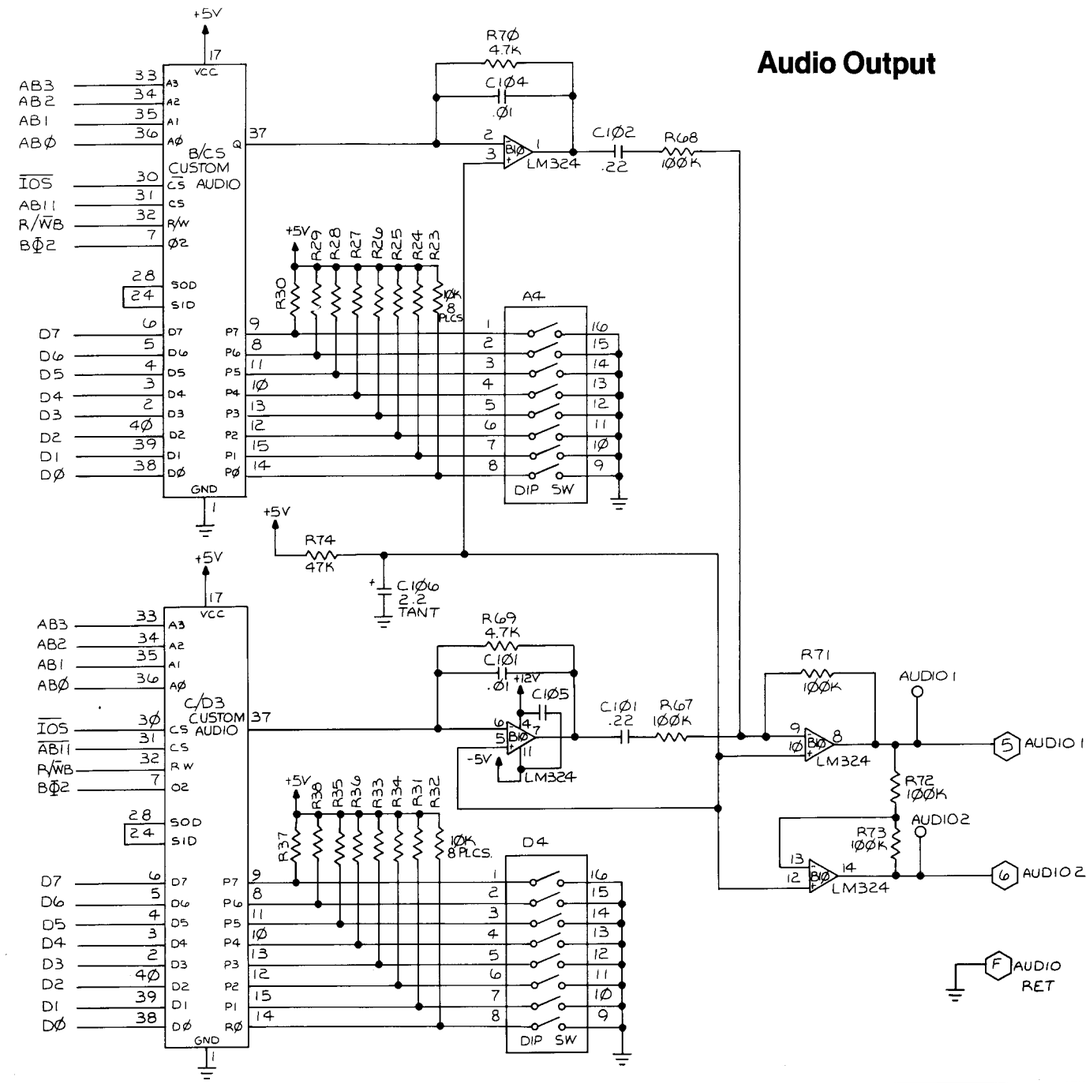
Color Output



Coin Door and LED Output



Audio Output



Liberator™ PCB Schematic Diagram

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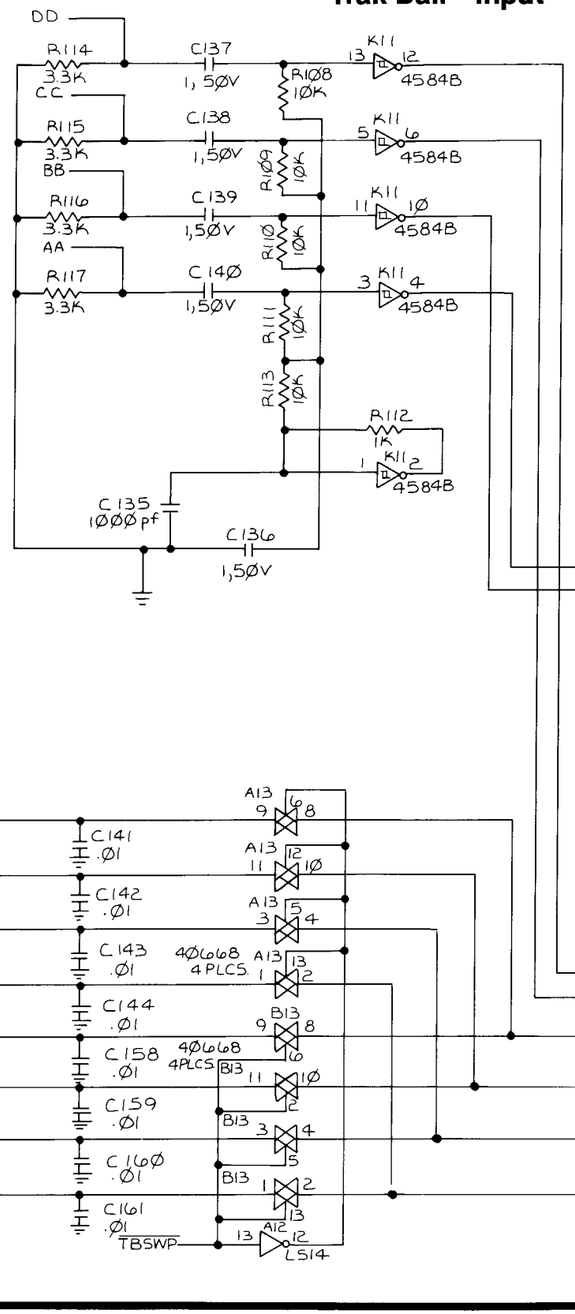
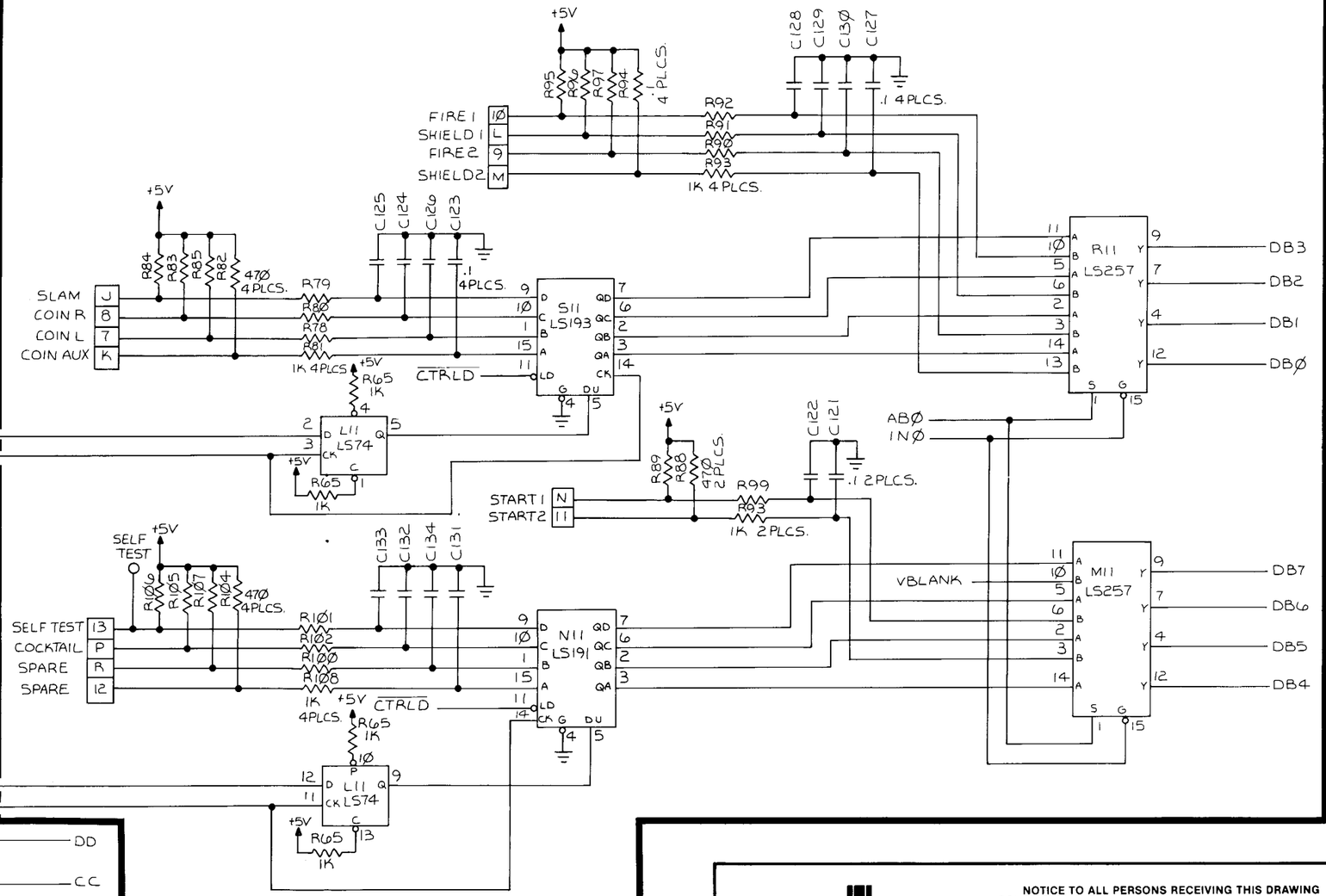
Trak-Ball™ Input



Coin Door and Control Panel Input



Liberator™ PCB Schematic Diagram

Description of Liberator PCB Signal Names

A0-A15

Address bits on Microprocessor Address Bus lines A0-A15 are software-generated by Microprocessor C2. When BITMD is low, A0-A13 are applied through buffers B1 and E1 to produce the bits on AB0-AB13.

AB0-AB13, $\overline{AB11}$

Address bits on Buffered Microprocessor Address Bus lines AB0-AB13 are software-generated either by Microprocessor C2 or by Bit Map Decoders H1 and F1. When BITMD is low, bits AB0-AB13 are generated via buffers B1 and E1. When BITMD is high and $\overline{BITMD}$ is low, Bit Map Decoders H1 and F1 generate the bits on lines AB0-AB13.

In the Address Decoders circuit, bits on lines AB12 and AB13 are the input signals for decoders T2, T3, and E4; and bits on lines AB9-AB11 are input signals for decoder S2.

Lines AB0-AB11 carry the addresses for the Program Memories.

AB11 is inverted by gate F4 to produce AB11. AB11 is a control bit for custom audio chip B/C3 in the Audio Output circuit. $\overline{AB11}$ is a control bit for custom audio chip C/D3 in the Audio Output circuit.

The Bit Map Address Multiplexers use the bits on lines AB0-AB13, together with those on 1V-128V and 4H-128H, to produce the address bits for the Bit Map Memories. The Bit Map Memory address bits are software-generated by Bit Map Address Multiplexers L9, K9, J9, and H9. When 2H and BMASEL are both low, these address bits are derived from the bits on 2V-128V. When 2H is low and BMASEL is high, the address bits are derived from 4H-128H and 1V. When 2H is high and BMASEL is low, these address bits are derived from AB7-AB13. When both 2H and BMASEL are high, these address bits are from AB0-AB6.

The Base RAM circuit uses the bits on lines AB0-AB3, together with those on 8V-128V, to produce address bits A1-A4 for Base RAM L5.

The Color Memory circuit uses the bits on lines AB0-AB3, together with those on PLAVID0-PLAVID3 and BIT0-BIT2, to produce the address bits for the Color Memories. In addition, the bit on AB4 is gated with $\overline{COLORAM}$ by gate F5 to produce the chip select signals for the Color Memories.

The EAROM circuit uses the bits on lines AB0-AB5 to produce the address bits for EAROM M2.

AUDIO1-AUDIO2

The Audio 1 and Audio 2 signals are game PCB output signals that are generated by custom audio chips B/C3 and C/D3 of the Audio Output circuit. AUDIO1 is the inverse of AUDIO2. These signals are applied to the Audio/Regulator II PCB to ultimately drive speakers 1 and 2.

$\overline{BASRAM}$

The Base RAM Enable signal is software-generated at pin 1 of Address Decoder S2 during addresses 0003 through 033F. $\overline{BASRAM}$ is the select signal for the Base RAM circuit.

BIT0-BIT2

The Pixel Bits on lines BIT0-BIT2 are generated from the Bit Map Shift Registers. When LDRAST is high and the Bit Map Shift Registers receive the next clock pulse, BIT0 is generated at pin 12 of R9 from the data bits on DRAM0-DRAM3; BIT1 is generated at pin 12 of P9 from the data bits on DRAM4-DRAM7; and BIT2 is generated at pin 12 of M9 from the data bits on DRAM8-DRAM11. BIT0-BIT2 are used by the Color Memory circuit to produce the address for the Color Memories.

$\overline{BITMD}$

The Bit Mode Enable signal is software-generated at pin 6 of Bit Map Address Decoder E4 during address 0002. $\overline{BITMD}$ is the output control signal for Bit Map Decoders H1 and F1. When $\overline{BITMD}$ goes low, the data bits latched by H1 and F1 from DB0-DB7 on the last positive-going transitions of XCOORD and YCOORD, are placed on lines AB0-AB13 and PIX0-PIX1.

BITMD

The Bit Mode Disable signal is software-generated at pin 8 of inverter F4 in the Bit Map Address Decoders circuit during address 0002. BITMD is the disenable signal for buffers B1 and E1 of the Microprocessor circuit. When BITMD goes high, the buffers are tri-stated and the bit map addresses are put on the address bus.

BLU

The Blue Signal is a game PCB output signal developed from the bits on B1 and B2. BLU is generated at the emitter of Q4 in the Color Output circuit. The bits on B1 and B2 are summed at the base of Q5 and buffered by Q5 and Q4 to produce BLU.

BMASEL

The Bit Map Address Select signal is hardware-generated at pin 5 of latch E8 in the Refresh circuit. In the Bit Map Address Multiplexers circuit, BMASEL is the A select signal for Bit Map Address Multiplexers H9, J9, K9, and L9.

BΦ2

The active high-level Phase 2 Clock signal is hardware-generated from the internal clock circuitry of Microprocessor C2 and buffered by E3. BΦ2 is gated with $\overline{R}$/WB and $\overline{1H}$ to produce $\overline{WRITE}$. BΦ2 is also used as the clock for custom audio chips B/C3 and C/D3 of the Audio Output circuit.

B/W

The Black and White Video signal is a game PCB output signal that is generated at the emitter of Q11 in the Color Output circuit from $\overline{COMPSYNC}$, BLU, GRN, and RED. This signal can be used by a black and white video display when a color display is not available.

$\overline{CAS}$

The active low-level Column Address Select signal is hardware-generated at pin 9 of latch C9 in the Refresh circuit. $\overline{CAS}$ is used to refresh the column address of the dynamic Bit Map Memories.

CC0-CC3

The bits on Planet Color Code lines CC0-CC3 are software-generated by Planet Picture ROMs P8 and M/N8.

CLRLDWE

The Clear/Load/Write Enable signal is hardware-generated at pin 9 of latch C8 in the Multiply Clock circuit. CLRLDWE is a control signal for the Multiply Clock circuit.

COINCNTRL

The Coin Counter Left signal is a game PCB output signal generated at the collector of Q3 in the Coin Door and Utility Panel Output circuit. COINCNTRL is applied to the game utility panel to activate the Left Coin Counter.

COINCNTRR

The Coin Counter Right signal is a game PCB output signal generated at the collector of Q2 in the Coin Door and Utility Panel Output circuit. COINCNTRR is applied to the game utility panel to activate the Right Coin Counter.

$\overline{COLORAM}$

The active low-level Color RAM Enable signal is software-generated at pin 2 of Address Decoder S2 during addresses 6200 through 621F and is used in the Color Memory circuit. When $\overline{COLORAM}$ is low, the Color Memory address bits are from AB0-AB3. When $\overline{COLORAM}$ is high and the A select signal is low, the Color Memory address bits are from BIT0-BIT2. When $\overline{COLORAM}$ and the A select signal are high, the Color Memory Address bits are from PLAVID0-PLAVID3. When both $\overline{COLORAM}$ and 5MHZ go low, the Color Memories are enabled to write data.

$\overline{COMPSYNC}$

The active low-level Composite Synchronization signal is hardware-generated at pin 3 of gate M3 in the Vertical Sync Chain by exclusive-ORing $\overline{HSYNC}$ and VSYNC. $\overline{COMPSYNC}$ is applied directly to the video display circuitry for further processing.

$\overline{CTRLD}$

The active low-level Control Load signal is generated at pin 9 of latch T11 in the Coin Counter and LED Output circuit. When $\overline{CTRLD}$ goes low, counters S11 and N11 are loaded from the Coin Door and Control Panel Input switches.

D0-D7

Microprocessor Data Bus lines D0-D7 form a bidirectional data bus between the Microprocessor, the Program Memory, and the Audio Output circuits.

DB0-DB7

Buffered Microprocessor Data Bus lines DB0-DB7 form a buffered bidirectional data bus between microprocessor data-bus buffer E2 and Bit Map Decoders H1 and F1; Bit Map Data Multiplexers H11 and P11; Bit Map Data Buffers T9, S9, and N9; Bit Map Memories H10, R10, N10, and K10; Longitude Scaling latch R6; Color Memories F11, C11, E11, and B11; EAROM latches R2 and K2; EAROM buffer H2; Coin Door and LED Output decoder T11; and Coin Door and Control Panel Input multiplexers R11 and M11.

DINIT

The active high-level Display Initialize signal is generated at pin 8 of gate L4 in the Planet ROM Address Generator circuit. When high, DINIT clears counter M7 and (via gate F5) clears latch E5. In the Line Buffer Address Controller circuit, DINIT clears flip-flop K4 and counter H7.

$\overline{DISDAT}$

Disable Data is an active low-level signal generated by test equipment connected to the $\overline{DISDAT}$ test point.

DRAM0-DRAM11

The bits on Bit Map Data Bus lines DRAM0-DRAM11 are software-generated by the Bit Map Memories. When BITMD, $\overline{RAM}$, and $\overline{R}$/WB are all low, the bits on DRAM0-DRAM7 are passed through Bit Map Data Buffer T9 to the microprocessor data bus. Otherwise, when $\overline{BITMD}$ and $\overline{R}$/WB are low, the bits on DRAM0-DRAM11 are multiplexed by S9 and N9 of the Bit Map Data Buffer circuit and passed to lines DB4-DB7 of the microprocessor data bus.

In the Bit Map Shift Registers circuit, if LDRAST is high, the bits on DRAM0-DRAM3 are used by shift register R9 to produce BIT0; the bits on DRAM4-DRAM7 are used by shift register P9 to produce BIT1; and the bits on DRAM8-DRAM11 are used by shift register M9 to produce BIT2.

EARCON

The Electrically Alterable Read-Only Memory Control signal is software-generated at pin 4 of Address Decoder S2 at address 6600. EARCON is the clock signal for latch R2 in the EAROM circuit. When high, EARCON allows R2 to pass data bits on lines DB0-DB3 to the control lines of EAROM M2.

$\overline{EARD}$

The Electrically-Alterable Read-Only Memory Read Enable is software-generated at pin 12 of Address Decoder E4 at address 4000. $\overline{EARD}$ is the select signal for buffer H2 of the EAROM circuit. When low, $\overline{EARD}$ allows the eight data bits from EAROM M2 to be passed through buffer H2 to the microprocessor data bus.

$\overline{EARWR}$

The Electrically-Alterable Read-Only Memory Write Enable is software-generated at pin 9 of Address Decoder S2 at addresses 6E00 through 6E3F. $\overline{EARWR}$ is the clock signal for latches P2 and K2 in the EAROM circuit. When low, $\overline{EARWR}$ allows address bits on lines AB0-AB5 and data bits on lines DB0-DB7 to pass to the address and data input pins of EAROM M2.

FSG

The active high-level First Segment signal is the carry output of adder R7 in the Longitude Scaling circuit. When FSG is high and LDRAST is high, the C0 input of adder P7 is set high. In addition, FSG is gated with PLS and HOR by gates R4, R3, and P3 in the Planet ROM Address Generator circuit to produce the clock signal for latch N7.

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Liberator™ PCB Signal Name Descriptions

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Description of Liberator PCB Signal Names (continued)

GRN

The Green signal is a game PCB output signal developed from the bits on G0-G2. GRN is generated at the emitter of Q8 in the Color Output circuit. The bits on G0-G2 are summed at the base of Q9 and buffered by Q8 and Q9 to produce GRN.

HBLANK

The active high-level Horizontal Blanking signal is hardware-generated at pin 11 of counter F9 in the Horizontal Sync Chain. HBLANK is applied through inverter L3 to produce $\overline{\text{HBLANK}}$. If HBLANK is high when latch T4 is clocked, HBLANK* is set high and $\overline{\text{HBLANK}}$* is set low. When HBLANK goes low, HSYNC from latch T4 is preset to the high state.

$\overline{\text{HBLANK}}$

The active low-level Horizontal Blanking signal is hardware-generated at pin 6 of inverter L3 in the Horizontal Sync Chain by inverting HBLANK. When low, $\overline{\text{HBLANK}}$ presets HBLANK* from latch T4 to the low state and $\overline{\text{HBLANK}}$* to the high state. In the Planet Control circuit, when $\overline{\text{HBLANK}}$ goes low, it presets $\overline{\text{HOR}}$ from latch S3 to the high state and HOR to the low state.

HBLANK*

The active high-level Delayed Horizontal Blanking signal is hardware-generated at pin 9 of latch T4 in the Horizontal Sync Chain. HBLANK* is generated when HBLANK has been delayed by the gated result of 8H and 10MHZ. HBLANK* is the clock signal for latch M4 in the Vertical Sync Chain.

$\overline{\text{HBLANK}}$*

The active low-level Delayed Horizontal Blanking signal is hardware-generated at pin 8 of latch T4 in the Horizontal Sync Chain. $\overline{\text{HBLANK}}$* is generated when HBLANK has been delayed by the gated result of 8H and 10MHZ. $\overline{\text{HBLANK}}$* is the clock signal for latch L8 in the Vertical Sync Chain. In the Valid Segment Detector, $\overline{\text{HBLANK}}$* is gated with $\overline{\text{HORDL}}$ by gate P3 to produce the clock signal for latch N3. When $\overline{\text{HBLANK}}$* goes low, counters B6 and D6 in the Display Counter and Comparator circuit are enabled to load data.

HCLK1, HCLK2

The Trak-Ball™ Horizontal Clock signals are PCB input signals to the Trak-Ball™ Input circuit. When $\overline{\text{TBSWP}}$ is high, HCLK1 is the clock signal for latch L11 and counter S11 in the Coin Door and Control Panel Input circuit; when $\overline{\text{TBSWP}}$ is low, HCLK2 is the clock signal for latch L11 and counter S11.

HDIR1, HDIR2

The Trak-Ball™ Horizontal Direction signals are PCB input signals to the Trak-Ball™ Input circuit. When $\overline{\text{TBSWP}}$ is high, HDIR1 enables counter S11 in the Coin Door and Control Panel Input circuit to count; when $\overline{\text{TBSWP}}$ is low, HDIR2 enables counter S11.

HOR

The Horizontal Planet Enable signal is hardware-generated at pin 6 of latch S3 in the Planet Control circuit. When $\overline{\text{HBLANK}}$ goes low, HOR is preset to the low state. When latch S3 receives the next positive-going transition of clock 64H, HOR is set high. HOR is latched by S4 during the next positive-going transition of LDRAST to produce HORDL and $\overline{\text{HORDL}}$.

$\overline{\text{HOR}}$

The Complementary Horizontal Planet Enable signal is hardware-generated at pin 5 of latch S3 in the Planet Control circuit. When $\overline{\text{HBLANK}}$ goes low, $\overline{\text{HOR}}$ is preset to the high state. When latch S3 receives the next positive-going transition of clock 64H, $\overline{\text{HOR}}$ is set low. In the Planet ROM Address Generator circuit, when $\overline{\text{HOR}}$ goes high, it is gated with HORDL by gate P4 to produce the load signal for counter M7. In the Valid Segment Detector circuit, $\overline{\text{HOR}}$ is the clear signal for latch N3.

HORDL

The active high-level Delayed Horizontal Planet Enable signal is hardware-generated at pin 7 of latch S4 in the Planet Control circuit. HORDL is HOR which has been delayed by one cycle of LDRAST. HORDL, 2H, 1H, and all remaining output signals from latch S4 are gated by M3, M5, and N4 to produce PLANET, PLANETDL, and $\overline{\text{PLANETDL}}$ from latches D9 and H5. In the Planet ROM Address Generator circuit, when HORDL goes high, it is gated with $\overline{\text{HOR}}$ by gate P4 to produce the load signal for counter M7. In the Line Buffer Address Controller circuit, HORDL and $\overline{\text{4H}}$ are used by latch S3 and gate J3 to produce $\overline{\text{PINIT2}}$.

$\overline{\text{HORDL}}$

The Complementary Delayed Horizontal Planet Enable signal is hardware-generated at pin 6 of latch S4 in the Planet Control circuit. $\overline{\text{HORDL}}$ is the complement of HOR. HORDL, 2H, 1H, and all remaining output signals from latch S4 in the Planet Control circuit are used to produce PLANET, PLANETDL, and $\overline{\text{PLANETDL}}$. When high, $\overline{\text{HORDL}}$ is gated with HOR by gate L4 in the Planet ROM Address Generator circuit to produce DINIT. When low, $\overline{\text{HORDL}}$ is gated with $\overline{\text{HBLANK}}$* by gate P3 in the Valid Segment Detector circuit to produce the clock signal for latch N3.

HSYNC

The Horizontal Synchronization signal is hardware-generated at pin 6 of latch T4 in the Horizontal Sync Chain. HSYNC is generated from 32H when latch T4 is clocked by 16H. HSYNC is the clock signal for counters H8 and J8 in the Vertical Sync Chain. HSYNC is also applied directly to the video display circuitry for further processing.

$\overline{\text{HSYNC}}$

The Complementary Horizontal Synchronization signal is hardware-generated at pin 5 of latch T4 in the Horizontal Sync Chain. $\overline{\text{HSYNC}}$ is generated from 32H when latch T4 is clocked by 16H. $\overline{\text{HSYNC}}$ is exclusive-ORed with VSYNC by gate M3 in the Vertical Sync Chain to produce $\overline{\text{COMPSYNC}}$.

$\overline{\text{IN0}}$

The active low-level Input Switch 0 Enable signal is software-generated at pin 11 of Address Decoder E4 at addresses 5000 through 5001. $\overline{\text{IN0}}$ is the output control enable signal for multiplexers R11 and M11 in the Coin Door and Control Panel Input circuit.

$\overline{\text{INTACK}}$

The active low-level Interrupt Acknowledge signal is software-generated at pin 3 of Address Decoder S2 at address 6400. This signal is an acknowledgment from Microprocessor C2 that an interrupt request has been received. $\overline{\text{INTACK}}$ presets latch K3.

$\overline{\text{IOS}}$

The active low-level Input/Output Sound signal is software-generated at pin 9 of Address Decoder E4 during addresses 7000 through 781F. In the Microprocessor circuit, $\overline{\text{IOS}}$ is gated with the ROM signal by gates H4 and H3 to enable bidirectional data bus buffer E2 to pass data. When $\overline{\text{IOS}}$ or ROM is high, data buffer E2 is turned off, which allows custom audio chips B/C3 and C/D3 to pass data to the microprocessor data bus.

IRQCK

The active high-level Interrupt Request Clock is hardware-generated at pin 15 of latch M4 in the Vertical Sync Chain. IRQCK is the interrupt clock signal for Microprocessor C2.

LATCHEN

The active high-level Latch Enable is generated at pin 1 of gate B9 in the Display Counter and Comparator circuit. LATCHEN is the clock signal for latch A6 in the Display Counter and Comparator circuit and for latch P5 in the Line Buffer circuit.

LBAINC

The active high-level Line Buffer Address Increment signal is generated at pin 10 of J-K flip-flop K4 in the Display Counter and Comparator circuit. In the Line Buffer Address Controller circuit, when LBAINC is high and if either $\overline{\text{VASEG}}$ or LDRAST is high, J-K flip-flop K4 is clocked and counter H7 is enabled to count.

LDRAST

The active high-level Load Raster Enable signal is hardware-generated at pin 6 of Load Raster Control Latch K3. When high, LDRAST is the shift/load signal for Bit Map Shift Registers R9, P9, and M9; the clock signal for latch S4 in the Planet Control circuit; and the clock signal for latch S3 in the Line Buffer Address Controller circuit.

LGS0-LGS7

The Longitude Scaling bits on lines LGS0-LGS7 are software-generated by Longitude Scalers T7 and S7. These bits are developed from the output signals of the Planet Picture ROMs and the latched data bits from R6. The bits on LGS0-LGS7, together with those from Latitude Scalers P6 and N6, are used by the Multiplier circuit to produce the bits on lines X0-X7.

LX0-LX7, $\overline{\text{LXD2}}$-$\overline{\text{LXD3}}$

The bits on Display Segment Length lines LX0-LX7 are software-generated from Line Buffer RAMs B7, C7, D7, and E7. In the Valid Segment Detector, LX0- LX7 are used to produce $\overline{\text{VASEG}}$. In addition, the bits on LX2 and LX3 are applied to latch P5 to produce the delayed bits of $\overline{\text{LXD2}}$ and $\overline{\text{LXD3}}$.

In the Display Counter and Comparator circuit, the bits on LX0-LX1, LX4-LX7, and $\overline{\text{LXD2}}$-$\overline{\text{LXD3}}$ are applied to comparators C6 and E6.

MD0-MD7

The data bits on Multiplexed Data bus lines MD0-MD7 are generated by Bit Map Data Multiplexers H11 and P11 from the data bits on DB0-DB7. When $\overline{\text{BITMD}}$ goes high, H11 and P11 multiplex the data bits from DB0-DB7 to produce those on MD0-MD7. Bit Map Memories E10, T10, P10, L10, F10, S10, M10, and J10 use the data on lines MD0-MD7 to generate DRAM0-DRAM7.

$\overline{\text{MTR}}$

The Multiplier signal is generated at pin 7 of shift register S6 in the Multiplier circuit. $\overline{\text{MTR}}$ is the shift/load enable for shift registers K6 and J6.

MULCLK

The active high-level Multiply Clock signal is hardware-generated at pin 8 of gate J4 in the Multiply Clock circuit. MUCLK is the clock signal for shift register S6, latch H5, and decoders K5 and J6 in the Multiplier circuit.

$\overline{\text{OUT0}}$

The active low-level Output Port 0 signal is software-generated at pin 7 of Address Decoder S2 at address 6C00. $\overline{\text{OUT0}}$ is the enable signal for decoder T11 in the Coin Counter and LED Output circuit.

$\overline{\text{PINIT2}}$

The active low-level Process Initialize signal is generated at pin 6 of gate J3 in the Line Buffer Address Controller circuit. If HORDL and $\overline{\text{4H}}$ are low when LDRAST goes high, $\overline{\text{PINIT2}}$ is set low. $\overline{\text{PINIT2}}$ loads counter H7 and presets flip-flop K4 in the Line Buffer Address Controller. In the Multiplier circuit, $\overline{\text{PINIT2}}$ clears latches F6 and D10. In the Valid Segment Detector, $\overline{\text{PINIT2}}$ clears latch N3.

PIX0

The active high-level Pixel Bit 0 is software-generated at pin 9 of Bit Map Decoder F1 from the bit on DB0. In the Write Protection circuit, PIX0 and PIX1 are multiplexed by C5 to produce $\overline{\text{WP0}}$. In the Bit Map Data Buffers circuit, PIX0 is the A select signal for multiplexers S9 and N9.

PIX1

The active high-level Pixel Bit 1 is software-generated at pin 6 of Bit Map Decoder F1 from the bit on DB1. In the Write Protection circuit, PIX1 and PIX0 are multiplexed by C5 to produce $\overline{\text{WP0}}$. In the Bit Map Data Buffers circuit, PIX1 is the B select signal for multiplexers S9 and N9.

PLA1

The Planet 1 Select signal is generated at pin 12 of latch T11 in the Coin Counter and LED Output circuit from the data bit on DB4. PLA1 is the chip select signal for Planet Picture ROMs M/N8 and T8.

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Liberator™ PCB Signal Name Descriptions

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Description of Liberator PCB Signal Names (continued)

PLA2

The Planet 2 Select signal is generated at pin 2 of inverter L3 in the Coin Counter and LED Output circuit by inverting PLA1. PLA2 is the chip select signal for Planet Picture ROMs P8 and R/S8.

PLANET

The Planet Enable signal is generated at pin 6 of flip-flop D9 in the Planet Control circuit. PLANET changes states at a 5-MHz rate if either of the signals at pins 2 or 3 of D9 is high. When high, PLANET is used by latch H5 to produce PLANETDL and $\overline{\text{PLANETDL}}$. When low, PLANET clears flip-flop K4 in the Display Counter and Comparator circuit.

PLANETDL

The active high-level Delayed Planet Enable signal is generated at pin 9 of latch H5 in the Planet Control circuit. When PLANETDL is high and counter D6 of the Display Counter and Comparator circuit has reached its minimum count, gate P4 produces the enable signal for Counter B6. At this time, if counter B6 was previously loaded by HBLANK* going low, counter B6 begins counting down.

$\overline{\text{PLANETDL}}$

The Complementary Delayed Planet Enable signal is generated at pin 8 of latch H5 in the Planet Control circuit. $\overline{\text{PLANETDL}}$ is the enable signal for Counter D6 in the Display Counter and Comparator circuit. When $\overline{\text{PLANETDL}}$ goes low, counter D6 begins counting down. In the Color Memory circuit, $\overline{\text{PLANETDL}}$ is gated by N5 with the latched BIT0-BIT2 outputs from R5 by gate N5 to produce the input signal for latch D5.

PLAVID0-PLAVID3

The Planet Video signals are software-generated by Line Buffers J7 and K7, latched by P5, and applied through multiplexers S5 and T5 to produce the Color Memory address bits.

PLS

The active high-level Planet Segment signal is hardware-generated at pin 8 of latch C8 in the Multiply Clock circuit. In the Planet ROM Address Generator circuit, PLS is gated with FSG and HOR by gates R4, R3, and P3 to produce the clock signal for latch N7. In the Multiplier circuit, PLS is the clock signal for latches F6 and D10.

$\overline{\text{RAM}}$

The active low-level Random-Access Memory enable is software-generated at pin 4 of Address Decoder T2. $\overline{\text{RAM}}$ is gated with A2-A13 by gates D1 and C1 of the Bit Map Address Decoders to produce the enable signal for E4. In the Write Protection circuit, $\overline{\text{RAM}}$ is gated with WRITE to produce the clear signal for latch D5. In the Bit Map Data Buffer circuit, $\overline{\text{RAM}}$ is gated with BITMD and R/$\overline{\text{WB}}$ by gate F3 to produce the enable signal for buffer T9.

$\overline{\text{RAS}}$

The active low-level Row Address Select signal is hardware-generated at pin 9 of latch E8 in the Refresh circuit. $\overline{\text{RAS}}$ is used to refresh the row address of the dynamic Bit Map Memories.

RED

The Red signal is a game PCB output signal developed from the bits on R0- R2. RED is generated at the emitter of Q6 in the Color Output circuit. The bits on R0-R2 are summed at the base of Q7 and buffered by Q7 and Q6 to produce RED.

$\overline{\text{RESET}}$

Reset is an active low-level signal generated at pin 12 of counter J11 from either the Watchdog circuit or the Power-On Reset circuit. The Power-On Reset circuit sets $\overline{\text{RESET}}$ to an active low level either when the RESET test point is shorted to ground or during the time that the power-supply voltages are reaching their stabilized, regulated levels. This ensures that the Microprocessor Address Bus (A0-A15) is stabilized before Microprocessor C2 begins operation.

The Watchdog circuit sets $\overline{\text{RESET}}$ to an active low level if the microprocessor fails to output address before counter J11 has reached its maximum count.

$\overline{\text{RESET}}$ is the clear signal for latches R2 in the EAROM circuit and T11 in the Coin Counter and LED Output circuit.

ROM

The active high-level Read-Only Memory Enable signal is software-generated at pin 8 of gate H4 in the Address Decoders circuit during addresses 8000 through EFFF. In the Microprocessor circuit, ROM is gated with $\overline{\text{I/OS}}$ by gates H4 and H3 to enable bidirectional data-bus buffer E2 to pass data.

In addition, ROM is ANDed with $\overline{\text{DISDAT}}$ by gate H4 in the Program Memory circuit to enable buffer F2 to pass data.

$\overline{\text{ROM0}}$

The active low-level Read-Only Memory Chip Select 0 signal is software-generated at pin 12 of Address Decoder T3 during addresses 8000 through 8FFF. $\overline{\text{ROM0}}$ is the chip-select signal for Program Memory J1. When low, $\overline{\text{ROM0}}$ allows J1 to be addressed and to pass data to buffer F2.

$\overline{\text{ROM1}}$

The active low-level Read-Only Memory Chip Select 1 signal is software-generated at pin 11 of Address Decoder T3 during addresses 9000 through 9FFF. $\overline{\text{ROM1}}$ is the chip-select signal for Program Memory K/L1. When low, $\overline{\text{ROM1}}$ allows K/L1 to be addressed and to pass data to buffer F2.

$\overline{\text{ROM2}}$

The active low-level Read-Only Memory Chip Select 2 signal is software-generated at pin 10 of Address Decoder T3 during addresses A000 through AFFF. $\overline{\text{ROM2}}$ is the chip-select signal for Program Memory L/M1. When low, $\overline{\text{ROM2}}$ allows L/M1 to be addressed and to pass data to buffer F2.

$\overline{\text{ROM3}}$

The active low-level Read-Only Memory Chip Select 3 signal is software-generated at pin 9 of Address Decoder T3 during addresses B000 through BFFF. $\overline{\text{ROM3}}$ is the chip-select signal for Program Memory N1. When low, $\overline{\text{ROM3}}$ allows N1 to be addressed and to pass data to buffer F2.

$\overline{\text{ROM4}}$

The active low-level Read-Only Memory Chip Select 4 signal is software-generated at pin 12 of Address Decoder T2 during addresses C000 through CFFF. $\overline{\text{ROM4}}$ is the chip-select signal for Program Memory P/R1. When low, $\overline{\text{ROM4}}$ allows P/R1 to be addressed and to pass data to buffer F2.

$\overline{\text{ROM5}}$

The active low-level Read-Only Memory Chip Select 5 signal is software-generated at pin 11 of Address Decoder T2 during addresses D000 through DFFF. $\overline{\text{ROM5}}$ is the chip-select signal for Program Memory R/S1. When low, $\overline{\text{ROM5}}$ allows R/S1 to be addressed and to pass data to buffer F2.

$\overline{\text{ROM6}}$

The active low-level Read-Only Memory Chip Select 6 signal is software-generated at pin 8 of gate P3 in the Address Decoder circuit during addresses E000 through EFFF. $\overline{\text{ROM6}}$ is the chip-select signal for Program Memory T1. When low, $\overline{\text{ROM6}}$ allows T1 to be addressed and to pass data to buffer F2.

R/$\overline{\text{WB}}$

The Buffered Read(High)/Write(Low) Enable signal is generated at pin 10 of inverter F4 in the Microprocessor circuit. R/$\overline{\text{WB}}$ is gated with BΦ2 and 1H by gates H4 and J4 to produce WRITE. In the Bit Map Data Buffers circuit, R/$\overline{\text{WB}}$ is gated with $\overline{\text{RAM}}$, $\overline{\text{BITMD}}$, and BITMD by gate F3 to produce the enable signals for buffer T9 and multiplexers S9 and N9.

R/$\overline{\text{WB}}$

The Buffered Read(High)/Write(Low) Enable signal is generated by Microprocessor C2, buffered by E3, and applied to custom audio chips B/C3 and C/D3 of the Audio Output circuit and buffer E2 of the Microprocessor circuit. R/$\overline{\text{WB}}$ determines the direction of data flow through these devices.

SGC0-SGC4

The Planet Segment Code bits on lines SGC1-SGC4 are hardware-generated by counter M7 in the Planet ROM Address Generator circuit. The bit on line SGC0 is hardware-generated at pin 5 of latch E5. The Planet Segment Code provides the address bits for the Planet Picture ROM.

STARTLG

The active high-level Starting Longitude Enable signal is software-generated at pin 5 of Address Decoder S2 at address 6800. STARTLG is the clock signal for latch R6 in the Longitude Scaling circuit.

$\overline{\text{VASEG}}$

The active low-level Valid Segment signal is generated at pin 9 of latch N3 in the Valid Segment Detector. When the carry bit from adder F7 is set high and 2H is high, $\overline{\text{VASEG}}$ is set low on the next positive-going transition of 1H. $\overline{\text{VASEG}}$ is gated with LDRAST and LBAINC by gates N4 and J4 to clock flip-flop K4 and enable a count-up operation by counter H7.

VBLANK

The active high-level Vertical Blanking signal is hardware-generated at pin 11 of latch M4 in the Vertical Sync Chain. VBLANK is applied to multiplexer M11 in the Coin Door and Control Panel Input circuit. When IN0 is low and AB0 is high, VBLANK is read by Microprocessor C2 on data bus line DB7.

$\overline{\text{VBLANK}}$

The active low-level Vertical Blanking signal is hardware-generated at pin 10 of latch M4 in the Vertical Sync Chain. $\overline{\text{VBLANK}}$ is gated with HBLANK* by gate L4 of the Horizontal Sync Chain to produce $\overline{\text{VIDBLANK}}$.

VCLK1, VCLK2

The Trak-Ball™ Vertical Clock signals are PCB input signals to the Trak-Ball™ Input circuit. When $\overline{\text{TBSWP}}$ is high, VCLK1 is the clock signal for latch L11 and counter N11 in the Coin Door and Control Panel Input circuit; when $\overline{\text{TBSWP}}$ is low, VCLK2 is the clock signal for latch L11 and counter N11.

VDIR1, VDIR2

The Trak-Ball™ Vertical Direction signals are PCB input signals to the Trak-Ball™ Input circuit. When $\overline{\text{TBSWP}}$ is high, VDIR1 enables counter N11 in the Coin Door and Control Panel Input circuit to count; when $\overline{\text{TBSWP}}$ is low, BDIR2 enables counter N11.

$\overline{\text{VIDBLANK}}$

The active low-level Video Blanking signal is hardware-generated at pin 6 of gate L4 in the Horizontal Sync Chain. $\overline{\text{VIDBLANK}}$ is the clear signal for Color Memory latches A11 and D11.

$\overline{\text{VPLA}}$

The active low-level Vertical Planet Enable signal is hardware-generated at pin 2 of latch M4 in the Vertical Sync Chain. $\overline{\text{VPLA}}$ is gated with PSIG2 by gate R4 in the Planet Control circuit to produce the clear signal for latch D9.

VSYNC

The active high-level Vertical Synchronization signal is hardware-generated at pin 6 of latch M4 in the Vertical Sync Chain. VSYNC is exclusive-ORed with $\overline{\text{HSYNC}}$ by gate M3 to produce $\overline{\text{COMPSYNC}}$. VSYNC is also applied directly to the video display circuitry for further processing.

$\overline{\text{WDDIS}}$

Watchdog Disable is a test point at pin 1 of gate L4 in the Watchdog circuit. When $\overline{\text{WDDIS}}$ is grounded, $\overline{\text{RESET}}$ is prevented from going to an active low level (except when the RESET test point is grounded).

Liberator™ PCB Signal Name Descriptions

Description of Liberator PCB Signal Names (continued)

WDOG

The active low-level Watchdog signal is software-generated at pin 6 of Address Decoder S2. WDOG is gated with WDDIS by gate L4 in the Watchdog circuit to produce the load signal for counter J11 of the Power-On Reset circuit.

WP0-WP3

The active low-level Write Pulses 0-3 are software-generated from gate B5 in the Write Protection circuit. These pulses are the write enable signals for the Bit Map Memories.

WRITE

The active low-level Write Enable signal is hardware-generated at pin 11 of gate J4 in the Microprocessor circuit. WRITE is applied to gate H3 in the Bit Map Address Decoders circuit where it is used to develope YCOORD and XCOORD. In the Write Protection circuit, WRITE is gated with RAM by gate N4 to produce the clear signal for latch D5. In the Address Decoders circuit, WRITE is applied to gate H3 to produce the D input signal for decoder S2.

X0-X7

The Planet Scaling bits are generated by latches F6 and D10 in the Multiplier circuit. These bits are developed by those from the Longitude and Latitude Scaling circuits. In the Valid Segment Detector, the bits on X0-X7 and those on LX0-LX7 are summed to produce VASEG from the carry bit of adder F7.

XCOORD

The active high-level Pixel X Coordinate signal is software-generated at pin 3 of gate H3 in the Bit Map Address Decoders circuit during address 0000. XCOORD is the clock signal for Bit Map Decoder F1. When XCOORD goes high, F1 internally latches the data bits from DB0-DB7. Then, when BITMD goes low, these bits are output from F1 to lines PIX0-PIX1 and AB0-AB5.

YCOORD

The active high-level Pixel Y Coordinate signal is software-generated at pin 11 of gate H3 in the Bit Map Address Decoders circuit during address 0001. YCOORD is the clock signal for Bit Map Decoder H1. When YCOORD goes high, H1 internally latches the data bits from DB0-DB7. Then, when BITMD goes low, these bits are output from H1 to lines AB6-AB13.

1H

Horizontal Timing Signal 1 is hardware-generated at pin 10 of latch D9 in the Horizontal Sync Chain. 1H is ANDed with 5MHZ by gate F8 of the Refresh circuit for use in developing RAS. In the Multiply Clock circuit, 1H is ANDed with 2H by gate F8 to produce the clear signal for latch D8. 1H is the clock signal for latch N3 of the Valid Segment Detector. In the Planet Control circuit, 1H is exclusive-ORed with the output signal at pin 14 of latch S4 by gate M3.

1H

Complementary Horizontal Timing Signal 1 is hardware-generated at pin 9 of latch D9 in the Horizontal Sync Chain. In the Microprocessor circuit, 1H is gated with BΦ2 and R/WB by gates H4 and J4 to produce WRITE. 1H is NANDed with 2H by gate N4 of the Load Raster Control Latch to develop the input signal for latch K3.

2H

Horizontal Timing Signal 2 is hardware-generated at pin 14 of counter E9 in the Horizontal Sync Chain. 2H is applied through inverter A8 to produce 2H. 2H is the timing reference for Microprocessor C2. In the Bit Map Address Multiplexer Circuit, 2H is the B select input for multiplexers L9, K9, J9, and H9. 2H is gated with 1H by gate N4 to produce the input signal for Load Raster Control Latch K3. In the Multiply Clock, 2H is ANDed with 1H by gate F8 to produce the clear signal for latch D8. In the Planet Control circuit, 2H is exclusive-ORed with the output signal at pin 10 of latch S4 by gate M3.

2H

Complementary Horizontal Timing Signal 2 is hardware-generated at pin 10 of inverter A8 in the Horizontal Sync Chain. 2H is the clock signal for latch E5 of the Planet ROM Address Generator. In the Valid Segment Detector, 2H is gated by P4 to produce the input signal for latch N3. 2H is the clock signal for multiplexer K5 in the Base RAM circuit.

4H

Horizontal Timing Signal 4 is hardware-generated at pin 13 of counter E9 in the Horizontal Sync Chain. 4H is applied through inverter A8 to produce 4H. 4H is multiplexed with 2V, AB7, and AB0 by Bit Map Address Multiplexer H9.

4H

Complementary Horizontal Timing Signal 4 is hardware-generated at pin 12 of inverter A8 in the Horizontal Sync Chain. 4H is applied to gate J3 in the Line Buffer Address Controller to produce PINIT2.

8H

Horizontal Timing Signal 8 is hardware-generated at pin 12 of counter E9 in the Horizontal Sync Chain. 8H is ANDed with 10MHZ by gate F8 to produce the clock signal for latch T4 in the Horizontal Sync Chain. 8H is multiplexed with 4V, AB8, and AB1 by Bit Map Address Multiplexer H9.

16H

Horizontal Timing Signal 16 is hardware-generated at pin 11 of counter E9 in the Horizontal Sync Chain. 16H is the clock signal for latch T4 of the Horizontal Sync Chain. 16H is multiplexed with 8V, AB9, and AB2 by Bit Map Address Multiplexer J9.

32H

Horizontal Timing Signal 32 is hardware-generated at pin 14 of counter F9 in the Horizontal Sync Chain. 32H is used by latch T4 of the Horizontal Sync Chain to produce HSYNC and HSYNC. 32H is multiplexed with 16V, AB10, and AB3 by Bit Map Address Multiplexer J9.

64H

Horizontal Timing Signal 64 is hardware-generated at pin 13 of counter F9 in the Horizontal Sync Chain. 64H is multiplexed with 32V, AB11, and AB4 by Bit Map Address Multiplexer K9. In the Planet Control circuit, 64H is the clock signal for latch S3.

128H

Horizontal Timing Signal 128 is hardware-generated at pin 12 of counter F9 in the Horizontal Sync Chain. 128H is multiplexed with 64V, AB12, and AB5 by Bit Map Address Multiplexer K9.

5MHZ

The 5 MHz Clock signal is hardware-generated at pin 5 of Clock latch C9. 5MHZ is the P enable signal for counters E9 and F9 in the Horizontal Sync Chain. In the Refresh circuit, 5MHZ is ANDed with 1H by gate F8. 5MHZ is the clock signal for Load Raster Control Latch K3 and Planet Control latch H5.

5MHZ

The Complementary 5 MHz Clock signal is hardware-generated at pin 6 of Clock latch C9. 5MHZ is the input signal for latch D5 in the Write Protection circuit. 5MHZ is the clock signal for Bit Map Shift Registers M9, P9, and R9. In the Multiply Clock, 5MHZ is the input signal for latches D8 and C8. In the Planet Control circuit, 5MHZ is the clock signal for latch D9. 5MHZ is gated with VASEG and LDRAST by gates N4 and P4 in the Line Buffer Address Controller circuit. In the Base RAM circuit, 5MHZ is gated with BASRAM by J5 to produce the write enable signal for Base RAM L5. In the Color Memory, 5MHZ is the clock signal for latches R5 and D5. It is also gated with COLORAM by gate J5 to produce the write enable signal for Color RAMs B11, C11, E11, and F11.

10MHZ

The 10 MHZ Clock signal is hardware-generated at pin 9 of Clock latch B8. The 10 MHZ signal is used to clock latches E8 of the Refresh circuit, D8 of the Multiply Clock circuit, and D5 of the Write Protection circuit. 10 MHZ is ANDed with 8H by gate F8 in the Horizontal Sync Chain to produce the clock signal for latch T4. In the Multiply Clock circuit, 10 MHZ is used by latch C8 to produce the CLRLDWE and PLS signals. In the Display Counter and Comparator circuit, 10 MHZ is gated with LBAINC by gate B9 to produce LATCHEN.

10MHZ

The Complementary 10 MHz Clock signal is hardware-generated at pin 8 of Clock latch B8. 10MHZ is the clock signal for latch C9 in the Refresh circuit; devices D9, E9, and F9 in the Horizontal Sync Chain; counters B6 and D6 in the Display Counter and Comparator; and latches A11 and D11 in the Color Memory. In addition, 10MHZ is gated with 20MHZ by gate B9 of the Display Counter and Comparator to produce the clock signal for flip-flop K4.

20MHZ

The 20 MHz Clock signal is hardware-generated by crystal clock Y1 in the Clock circuit. 20MHZ is the clock signal for latches B8 in the Clock and Multiply Clock circuits. In the Display Counter and Comparator, 20MHZ is gated with 10MHZ by gate B9 to produce the clock signal for flip-flop K4.

20MHZ

The Complementary 20 MHz Clock signal is hardware-generated at pin 4 of inverter A8 in the Clock circuit. 20MHZ is the clock signal for latches C8 and D8 of the Multiply Clock.

1V

Vertical Timing Signal 1 is hardware-generated at pin 14 of counter H8 in the Vertical Sync Chain. 1V and 2V are multiplexed by K8 and latched by M4 to produce VBLANK and VBLANK. Also, 1V is used by latch L8 to produce 1VDL. 1V is multiplexed with 128V, AB13, and AB6 by Bit Map Address Multiplexer L9.

2V

Vertical Timing Signal 2 is hardware-generated at pin 13 of counter H8 in the Vertical Sync Chain. 2V and 1V are multiplexed by K8 and latched by M4 to produce VBLANK and VBLANK. Also, 2V is used by latch L8 to produce 2VDL. 2V is multiplexed with 4H, AB7, and AB0 by Bit Map Address Multiplexer H9.

4V

Vertical Timing Signal 4 is hardware-generated at pin 12 of counter H8 in the Vertical Sync Chain. 4V and 8V are multiplexed by K8 and latched by M4 to produce VSYNC. Also, 4V is used by latch L8 to produce 4VDL. 4V is multiplexed with 8H, AB8, and AB1 by Bit Map Address Multiplexer H9.

8V

Vertical Timing Signal 8 is hardware-generated at pin 11 of counter H8 in the Vertical Sync Chain. 8V and 4V are multiplexed by K8 and latched by M4 to produce VSYNC. Also, 8V is used by latch L8 to produce 8VDL. 8V is multiplexed with 16H, AB9, and AB2 by Bit Map Address Multiplexer J9.

16V

Vertical Timing Signal 16 is hardware-generated at pin 14 of counter J8 in the Vertical Sync Chain. 16V and 32V are multiplexed by K8 and latched by M4 to produce IRQCK. Also, 16V is used by latch L8 to produce 16VDL. 16V is multiplexed with 32H, AB10, and AB3 by Bit Map Address Multiplexer J9. 16V is applied with AB1 to Base RAM decoder L7 to generate address bit 3 for Base RAM L5.

32V

Vertical Timing Signal 32 is hardware-generated at pin 13 of counter J8 in the Vertical Sync Chain. 32V and 16V are multiplexed by K8 and latched by M4 to produce IRQCK. Also, 32V is used by latch L8 to produce 32VDL. 32V is multiplexed with 64H, AB11, and AB4 by Bit Map Address Multiplexer K9.

64V

Vertical Timing Signal 64 is hardware-generated at pin 12 of counter J8 in the Vertical Sync Chain. 64V and 128V are multiplexed by K8 and latched by M4 to produce VPLA. 64V is applied through inverter A8 to produce 64V. 64V is multiplexed with 128H, AB12, and AB5 by Bit Map Address Multiplexer K9.

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Description of Liberator PCB Signal Names (continued)

$\overline{64V}$

Complementary Vertical Timing Signal 64 is hardware-generated at pin 8 of inverter A8 in the Vertical Sync Chain. $\overline{64V}$ is used by latch L8 in the Vertical Sync Chain.

128V

Vertical Timing Signal 128 is hardware-generated at pin 11 of counter J8 in the Vertical Sync Chain. 128V and 64V are multiplexed by K8 and latched by M4 to produce $\overline{VPLA}$. 128V is the clock 1 signal for counter J11 of the Power-On Reset circuit. 128V is also multiplexed with 1V, AB13, and AB6 by Bit Map Address Multiplexer L9. 128V is applied with AB3 to Base RAM decoder L7 to generate address bit 4 for Base RAM L5.

1VDL

Delayed Vertical Timing Signal 1 is hardware-generated at pin 5 of latch L8 in the Vertical Sync Chain. 1VDL is derived from 1V after a delay by $\overline{HBLANK}$*. 1VDL is address bit 5 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 0 for Latitude Scalers P6 and N6.

2VDL

Delayed Vertical Timing Signal 2 is hardware-generated at pin 15 of latch L8 in the Vertical Sync Chain. 2VDL is derived from 2V after a delay by $\overline{HBLANK}$*. 2VDL is address bit 6 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 1 for Latitude Scalers P6 and N6.

4VDL

Delayed Vertical Timing Signal 4 is hardware-generated at pin 9 of latch L8 in the Vertical Sync Chain. 4VDL is derived from 4V after a delay by $\overline{HBLANK}$*. 4VDL is address bit 7 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 2 for Latitude Scalers P6 and N6.

8VDL

Delayed Vertical Timing Signal 8 is hardware-generated at pin 6 of latch L8 in the Vertical Sync Chain. 8VDL is derived from 8V after a delay by $\overline{HBLANK}$*. 8VDL is address bit 8 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 3 for Latitude Scalers P6 and N6.

16VDL

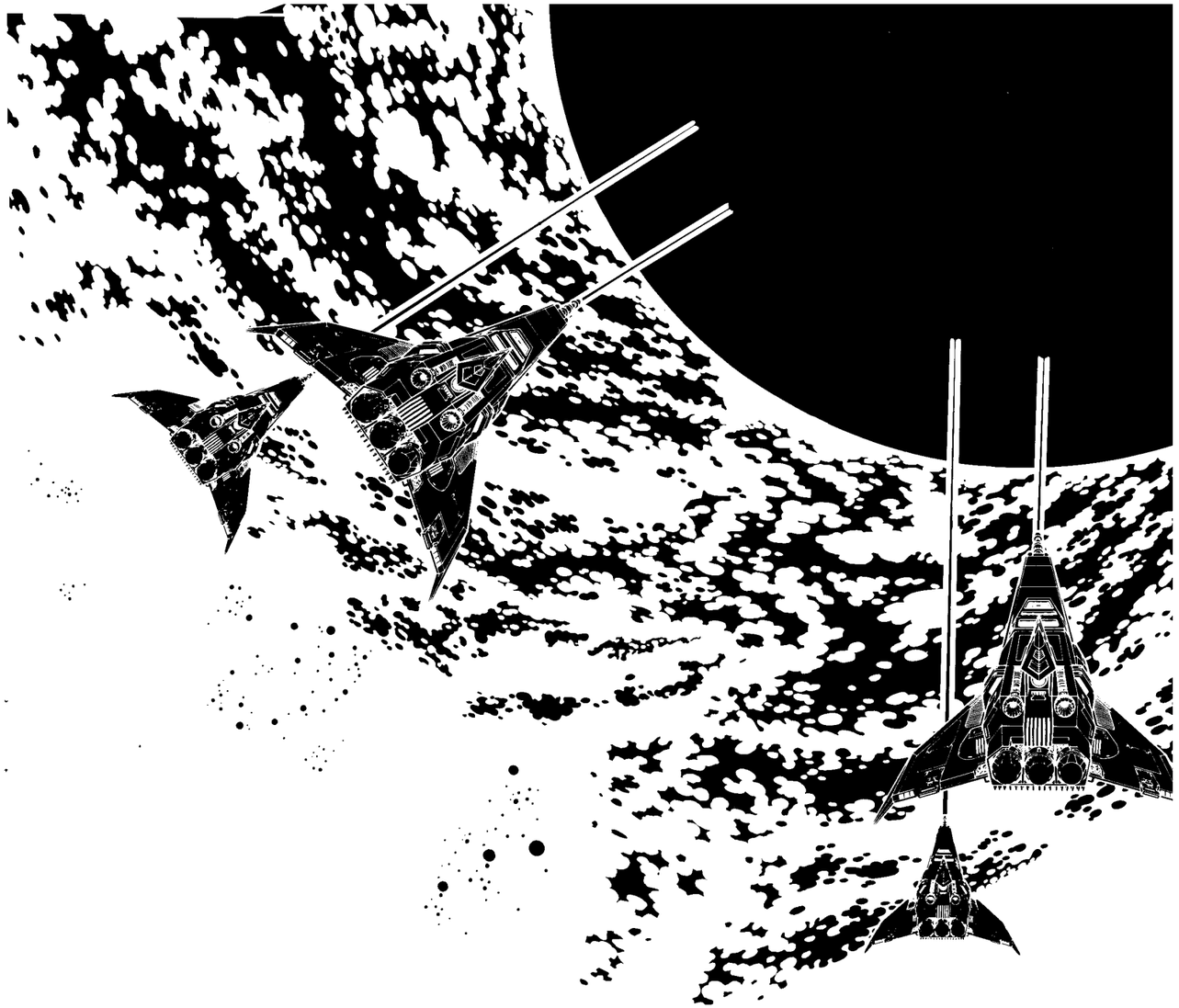
Delayed Vertical Timing Signal 16 is hardware-generated at pin 2 of latch L8 in the Vertical Sync Chain. 16VDL is derived from 16V after a delay by $\overline{HBLANK}$*. 16VDL is address bit 9 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 4 for Latitude Scalers P6 and N6.

32VDL

Delayed Vertical Timing Signal 32 is hardware-generated at pin 19 of latch L8 in the Vertical Sync Chain. 32VDL is derived from 32V after a delay by $\overline{HBLANK}$*. 32VDL is address bit 10 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 5 for Latitude Scalers P6 and N6.

$\overline{64VDL}$

Delayed Vertical Timing Signal 64 is hardware-generated at pin 12 of latch L8 in the Vertical Sync Chain. $\overline{64VDL}$ is derived from $\overline{64V}$ after a delay by $\overline{HBLANK}$*. 64VDL is address bit 11 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 6 for Latitude Scalers P6 and N6. □



Liberator™ PCB Signal Name Descriptions

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Liberator™ Troubleshooting with the CAT Box

Table of Contents

Troubleshooting with the Read/Write Controller

A. CAT Box Preliminary Set-Up

1. Remove the electrical power from the game and the CAT Box.
2. Remove the wiring harness from the game PCB.
3. Remove the game PCB from the game cabinet.
4. Remove Microprocessor C2 from the game PCB.
5. Connect the harness from the game to the game PCB.
6. Connect together the Φ0 and Φ2 test points on the game PCB with the shortest possible jumper.
7. Connect the $\overline{\text{WDDIS}}$ test point to ground.
8. Connect the CAT Box flex cable to the game PCB edge test connector.
9. Apply power to the game and to the CAT Box.
10. Set CAT Box switches as indicated:
    a. TESTER SELF-TEST: OFF
    b. TESTER MODE: R/$\overline{\text{W}}$
11. Press TESTER RESET.
12. Connect the DATA PROBE to the CAT Box. Connect the DATA PROBE ground clip to a game PCB ground test point.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

B. Checking the Address Lines

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
    a. BYTES: 1
    b. PULSE MODE: UNLATCHED
    c. R/$\overline{\text{W}}$ MODE: (OFF)
    d. R/$\overline{\text{W}}$: READ
3. Key in the address pattern given in Table 1 *(use AAAA to start)* with the CAT Box keyboard.
4. Set R/W MODE to STATIC.
5. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 1 lights up. Repeat this step for each address line listed in Table 1.
6. Repeat parts 2-c through 5 using address *5555* in part 3.

Table 1 Address Lines

LOGIC STATE FOR ADDRESS *AAAA*	IC-PIN	LOGIC STATE FOR ADDRESS *5555*
1	T2-3	0
0	T2-2	1
1	B1-11	0
0	B1-13	1
1	B1-9	0
0	B1-7	1
1	B1-5	0
0	B1-3	1
1	E1-7	0
0	E1-9	1
1	E1-5	0
0	E1-3	1
1	E1-12	0
0	E1-14	1
1	E1-16	0
0	E1-18	1

C. Checking the Data Lines

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
    a. BYTES:1
    b. R/$\overline{\text{W}}$ MODE: (OFF)
    c. R/$\overline{\text{W}}$: WRITE
3. Key in address *0000* with the keyboard.
4. Press DATA SET. Key in data *AA* with the keyboard.
5. Set R/$\overline{\text{W}}$ MODE to PULSE and back to (OFF).
6. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 2 lights up. Repeat this check for each IC-pin in Table 2.
7. Repeat parts 4 through 6 using data *55* in part 4.

Table 2 Data Lines

LOGIC STATE FOR DATA *AA*	IC-PIN	LOGIC STATE FOR DATA *55*
1	E2-11	0
0	E2-12	1
1	E2-13	0
0	E2-14	1
1	E2-15	0
0	E2-16	1
1	E2-17	0
0	E2-18	1
1	E2-9	0
0	E2-8	1
1	E2-7	0
0	E2-6	1
1	E2-5	0
0	E2-4	1
1	E2-3	0
0	E2-2	1

D. Checking the RAM

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
    a. DBUS SOURCE: ADDR
    b. BYTES:1024
    c. R/$\overline{\text{W}}$ MODE: (OFF)
    d. R/$\overline{\text{W}}$: WRITE
3. Enter address *0003* with the keyboard.

NOTE

Addresses *0000, 0001,* and *0002* are special RAM locations for bit mode operation that cannot be verified by this RAM test.

Continued on back of sheet

Liberator™ PCB Troubleshooting

4. Set the CAT Box switches as indicated:
   a. R/$\overline{W}$ MODE to PULSE and back to (OFF)
   b. R/$\overline{W}$ to READ
   c. R/$\overline{W}$ MODE to PULSE and back to (OFF)
5. If the CAT Box reads an address that doesn't compare with that written, the COMPARE ERROR LED will light up. The ADDRESS/SIGNATURE display of the CAT Box will show the failing address location and the ERROR DATA DISPLAY switch is enabled. Using this switch, determine if the error is in the high-order or low-order RAM.
6. Repeat parts 2-d through 4 using addresses *0400, 0800, 0C00, 1000, 1400, 1800, 1C00, 2000, 2400, 2800, 2C00, 3000, 3400, 3800,* and *3C00.*
7. Repeat this test with DBUS SOURCE set to $\overline{ADDR}$.

E. Checking the Custom Audio I/O Chips

> ***NOTE***
>
> Liberator has two custom audio I/O chips. Each must be tested separately. There are several ways to test these chips:
> - Perform the self-test.
> - Substitute a known good part for a suspected defective part.
> - Use the following procedure.

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{W}$: WRITE
   c. R/$\overline{W}$ MODE: (OFF)
3. Enter the address from Table 3 with the keyboard.
4. Press DATA SET and enter the data from Table 3 with the keyboard.
5. Set R/$\overline{W}$ MODE to PULSE and back to (OFF).
6. Repeat parts 3 through 5 for each address and data listed in Table 3. Check for the response indicated.

Table 3 Custom Audio I/O Chips

ADDRESS	DATA	TEST RESULTS
780F	*00*	
780F	*03*	
7800	*55*	
7801	*AF*	Custom Audio I/O Chip B3 channel 1 produces pure tone.
7801	*00*	Custom Audio I/O Chip B3 channel 1 off.
7802	*55*	
7803	*AF*	Custom Audio I/O Chip B3 channel 2 produces pure tone.
7803	*00*	Custom Audio I/O Chip B3 channel 2 off.
700F	*00*	
700F	*03*	
7000	*55*	
7001	*AF*	Custom Audio I/O Chip C/D3 channel 1 produces pure tone.
7001	*00*	Custom Audio I/O Chip C/D3 channel 1 off.
7002	*55*	
7003	*AF*	Custom Audio I/O Chip C/D3 channel 2 produces pure tone.
7003	*00*	Custom Audio I/O Chip C/D3 channel 2 off.

F. Checking the Player Switch, Option Switch, and Trak-Ball™ Inputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{W}$: WRITE
   c. R/$\overline{W}$ MODE: (OFF)
3. Enter address *6C04* with the keyboard.
4. Press DATA SET and enter data *00* with the keyboard.
5. Set R/$\overline{W}$ MODE to PULSE and back to (OFF). The $\overline{CTRLD}$ signal is now set to the low state.
6. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{W}$: READ
7. For each address listed in Table 4, do the following:
   a. Set R/$\overline{W}$ MODE to (OFF).
   b. Enter the address with the keyboard.
   c. Set R/$\overline{W}$ MODE to STATIC.
   d. Activate the input switch indicated in Table 4 for the address and check the test result.
8. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{W}$: WRITE
   c. R/$\overline{W}$ MODE: (OFF)
9. Enter address *6C02* with the keyboard.
10. Press DATA SET and enter data *00* with the keyboard.
11. Set R/$\overline{W}$ MODE to PULSE and back to (OFF). The $\overline{TBSWP}$ signal is now set to the low state.
12. Enter address *6C04* with the keyboard.
13. Press DATA SET and enter data *01* with the keyboard.
14. Set R/$\overline{W}$ MODE to PULSE and back to (OFF). The $\overline{CTRLD}$ signal is now set to the high state.
15. Set R/$\overline{W}$ to READ.
16. Set R/$\overline{W}$ MODE to (OFF).
17. Enter address *5000* with the keyboard.
18. Set R/$\overline{W}$ MODE to STATIC and check for the result shown in Table 5.

Table 4 Player and DIP Switch Inputs (with $\overline{CTRLD}$ Low)

ADDRESS	INPUT SWITCH	TEST RESULTS
5000	Slam, Right coin switch, Left coin switch, Self-Test switch, Auxillary coin switch.	DATA display changes when any coin or self-test switch is activated.
5001	FIRE 1, SHIELD 1, FIRE 2, SHIELD 2, START 1, START 2	DATA display changes when any of these switches is activated. (Note that display changes also without activating a switch because of VBLANK).

Table 5 TRAK-BALL™ Inputs (with $\overline{CTRLD}$ High and $\overline{TBSWP}$ Low)

ADDRESS	TRAK-BALL	TEST RESULT
5000	TRAK-BALL	Data display changes when TRAK-BALL is rolled.

G. Checking the LED and Coin Counter Outputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. BYTES: 1
   c. R/$\overline{W}$: WRITE
   d. R/$\overline{W}$ MODE: (OFF)

> ***CAUTION***
>
> If you write ON data to activate a solenoid, *deactivate the solenoid immediately* by writing the OFF data. If you leave a solenoid activated for more than 10 seconds, you may have to replace the solenoid and/or its driver, due to overheating.

3. For each address listed in Table 6, do the following:
   a. To activate the output:
      - Press DATA SET.
      - Enter data *00* with the keyboard.
      - Set R/$\overline{W}$ MODE to STATIC and back to (OFF).
   b. To deactivate the output:
      - Press DATA SET.
      - Enter data *FF* with the keyboard.
      - Set R/$\overline{W}$ MODE to STATIC and back to (OFF).

Continued on next sheet

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Liberator™ PCB Troubleshooting

Table 6 LED and Coin Counter Outputs

ADDRESS	DATA (0)	DATA (FF)	OUTPUT DEVICE
6C00	ON	OFF	Player 1 LED
6C01	ON	OFF	Player 2 LED
6C04	LOW	HIGH	$\overline{\text{CTRLD}}$
6C05	ON	OFF	Coin Counter Right
6C06	ON	OFF	Coin Counter Left
6C07	ON	OFF	PLANET

Troubleshooting with Signature Analysis

A. Checking the Address Lines and Address Decoders

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. BYTES: 1
   c. R/$\overline{W}$: WRITE
   d. R/$\overline{W}$ MODE: (OFF)
3. Enter address *0000* with the keyboard.
4. Press DATA SET and enter data *08* with the keyboard.
5. Set R/$\overline{W}$ MODE to STATIC and back to (OFF).
6. Enter address *0001* with the keyboard.
7. Press DATA SET and enter data *00* with the keyboard.
8. Set R/$\overline{W}$ MODE to STATIC and back to (OFF).
9. Connect the three BNC-to-EZ clip cables supplied with the CAT Box to the SIGNATURE ANALYSIS CONTROL START, STOP, and CLOCK jacks of the CAT Box.
10. Connect the three black EZ clips to a game PCB ground test point.
11. Ground pin 4 of IC H4 (the DISDAT signal) on the game PCB.
12. Set the CAT Box switches as indicated:
    a. TESTER MODE: SIG
    b. TESTER SELF-TEST: OFF
    c. PULSE MODE: LATCHED
    d. START: Negative-going edge trigger
    e. STOP: Negative-going edge trigger
    f. CLOCK: Negative-going edge trigger
13. Press TESTER RESET on the CAT Box.
14. Connect the CAT Box Signature Analysis probe tips as indicated:
    a. START: Pin 3 of IC T2
    b. STOP: Pin 3 of IC T2
    c. CLOCK: Φ2 test point
15. Verify the set-up connections by connecting the DATA PROBE to a game PCB ground test point. The CAT Box ADDRESS/SIGNATURE display should show *0000*. Now connect the DATA PROBE to a +5V test point. The ADDRESS/SIGNATURE display should show *0001*.
16. Probe the IC-pin listed in Table 7 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC-pin listed.

Table 7 Address Bus Signatures

IC-PIN	SIGNAL NAME	SIGNATURE
E1-18	AB0	*UUUU*
E1-16	AB1	*5555*
E1-14	AB2	*CCCC*
E1-12	AB3	*7F7F*
E1-3	AB4	*5H21*
E1-5	AB5	*0AFA*
E1-9	AB6	*UPFH*
E1-7	AB7	*52F8*
B1-3	AB8	*HC89*
B1-5	AB9	*2H70*
B1-7	AB10	*HPP0*
B1-9	AB11	*1293*
B1-13	AB12	*HAP7*
B11-11	AB13	*3C96*
T2-2	A14	*3827*
R2-3	A15	*755U*

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

17. Probe the IC-pin listed in Table 8 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC-pin listed.

Table 8 Decoder Signatures

IC-PIN	SIGNAL NAME	SIGNATURE
E4-0	$\overline{\text{BITMD}}$	*4001*
E4-8	BITMD	*4000*
E4-5	YCOORD	*8001*
E4-4	XCOORD	*0000*
E4-12	$\overline{\text{EARD}}$	*6FHH*
E4-11	$\overline{\text{IN0}}$	*57HH*
E4-10		*96F8*
E4-9	$\overline{\text{IOS}}$	*546U*
E4-4	$\overline{\text{RAM}}$	*5FU8*
T3-12	$\overline{\text{ROM0}}$	*CA11*
T3-11	$\overline{\text{ROM1}}$	*H759*
T3-10	$\overline{\text{ROM2}}$	*A3UH*
T3-9	$\overline{\text{ROM3}}$	*AA6A*
H4-8	ROM	*755U*
T2-12	$\overline{\text{ROM4}}$	*A711*
T2-11	$\overline{\text{ROM5}}$	*54F5*
P3-8	$\overline{\text{ROM6}}$	*P255*

B. Checking the Planet-Generating Circuitry

1. Perform steps 1 through 7 of the CAT Box preliminary set-up.
2. Connect the CAT Box Signature Analysis probe tips where indicated:
   a. START: Pin 11 of IC E9
   b. STOP: Pin 11 of IC E9
   c. CLOCK: Pin 8 of IC B8
3. Connect the ground clips of the CAT Box Signature Analysis and DATA probes to a game PCB ground test point.
4. Set the CAT Box switches as indicated:
   a. TESTER MODE: SIG
   b. TESTER SELF-TEST: OFF
   c. PULSE MODE: UNLATCHED
   d. START: Positive-going edge trigger
   e. STOP: Positive-going edge trigger
   f. CLOCK: Positive-going edge trigger
5. Turn on the game and the CAT Box.
6. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for *A70F*.
7. Test the signatures designated by (XXXX)1 printed in color on the schematic diagrams of the game PCB. To test for a signature, use the CAT Box DATA PROBE to probe the appropriate location on the game PCB. Then check the ADDRESS/SIGNATURE display for the appropriate signature.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

8. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated by (XXXX)1↓ on the schematics.
9. Connect the CAT Box Signature Analysis probe tips to:
   a. START: Pin 11 of IC F9
   b. STOP: Pin 11 of IC F9
10. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for *1308*.
11. Set the CAT Box CLOCK switch for a positive-going edge trigger and test the signatures designated on the schematics by (XXXX)2.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

12. Connect the CAT Box Signature Analysis probe tips to:
    a. START: Pin 11 of IC J8
    b. STOP: Pin 11 of IC J8
13. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for *H57U*.
14. Test the signatures designated on the schematics by (XXXX)3.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

15. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated on the schematics by (XXXX)3↓.
16. Remove the electrical power from the game and the CAT Box.
17. Connect the CAT Box flex cable to the game PCB edge test connector and connect the game PCB PSIG1 test point to ground.
18. Apply power to the game and the CAT Box.

Continued on back of sheet

Liberator™ PCB Troubleshooting

19. Set the CAT Box switches as indicated:
    a. TESTER MODE: R/$\overline{W}$
    b. BYTES: 1
    c. R/$\overline{W}$: WRITE
    d. R/$\overline{W}$ MODE: (OFF)
20. Press TESTER RESET.
21. Enter address *6800* with the keyboard.
22. Press DATA SET and enter data *00* with the keyboard.
23. Set R/$\overline{W}$ MODE to PULSE and back to (OFF).
24. Enter address *6C07* with the keyboard and repeat steps 22 and 23.
25. Set the CAT Box switches as indicated:
    a. TESTER MODE: SIG
    b. START: Negative-going edge trigger
    c. STOP: Negative-going edge trigger
    d. CLOCK: Positive-going edge trigger
26. Connect the CAT Box Signature Analysis probe tips to:
    a. START: Pin 12 of IC L8
    b. STOP: Pin 12 of IC L8
    c. CLOCK: Pin 10 of IC A8
27. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for *FP96*.
28. Test the signatures designated on the schematics by (XXXX)4.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

29. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated on the schematics by (XXXX)4↓.
30. Set TESTER MODE to R/$\overline{W}$ and enter address *6800* with the keyboard.
31. Press DATA SET and enter data *7F* with the keyboard.
32. Set R/$\overline{W}$ MODE to PULSE and back to (OFF).
33. Set the CAT Box switches as indicated:
    a. TESTER MODE: SIG
    b. START: Positive-going edge trigger
    c. STOP: Negative-going edge trigger
    d. CLOCK: Positive-going edge trigger
34. Connect the CAT Box Signature Analysis probe tips to:
    a. START: Pin 2 of IC M4
    b. STOP: Pin 2 of IC M4
35. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for *FP96*.
36. Test the signatures designated on the schematics by (XXXX)5.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

37. Connect pin 8 of IC P4 and connect test point $\overline{PSIG2}$ to a game PCB ground test point.
38. Set TESTER MODE to R/$\overline{W}$ and enter address *6000* with the keyboard.
39. Press DATA SET and enter data *00* with the keyboard.
40. Set R/$\overline{W}$ MODE to PULSE and back to (OFF).
41. Repeat steps 38 through 40 for addresses *6001, 6002, 6003, 6004, 6005, 6006, 6007, 6008, 6009, 600A, 600B, 600C, 600D, 600E, 600F,* and *6800*.
42. Set TESTER MODE to SIG.
43. Connect the CAT Box CLOCK probe tip to pin 8 of IC C8.
44. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for *FP96*.
44. Test the signatures designated on the schematics by (XXXX)6A.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

45. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated on the schematics by (XXXX)6A↓.
46. Remove the ground connection from pin 8 of IC P4 and from test point $\overline{PSIG2}$.
47. Connect the CAT Box CLOCK probe tip to pin 14 of IC E9 and set the CLOCK switch for a positive-going edge trigger.
48. Test the signatures designated on the schematics by (XXXX)6B.

Troubleshooting with Checksums

NOTE

This procedure can only be done with those CAT Boxes equipped with a Checksum Switch.

CAUTION

While testing with checksums, adding 100 pF capacitors to A14 and A15 may be necessary.

1. Perform the CAT Box preliminay set-up.
2. Set the CAT Box switches as indicated:
    a. BYTES: 256
    b. DBUS SOURCE: DATA
    c. R/$\overline{W}$ MODE: OFF
    d. CHECKSUM SWITCH: ON
3. Key in the address pattern given in Table 9 *(use 8000 to start)*.
4. Set the R/$\overline{W}$ MODE switch to PULSE and then back to (OFF).
5. Check the CAT Box ADDRESS/SIGNATURE display for the appropriate checksum.
6. Repeat parts 3 through 5 for each address listed in Table 9.

Table 9 ROM Checksums

ADDRESS	ROM TESTED	CHECKSUM
8000	ROM0	*2D29*
9000	ROM1	*EFDD*
A000	ROM2	*8265*
B000	ROM3	*17AB*
C000	ROM4	*E41F*
D000	ROM5	*55A7*
E000	ROM6	*BBE7*

Troubleshooting the Watchdog Circuit

The Watchdog circuit will send continuous reset pulses to the microprocessor if a problem exists within the microprocessor circuit. If the self-test fails to run, it is a good practice to check the reset line.

$\overline{RESET}$ is a microprocessor input (pin 40). In a properly operating game, reset should occur during power-up or when the RESET test point is grounded. A pulsing $\overline{RESET}$ line indicates that something is causing the microprocessor to lose its place within the program. Typical causes are:

1. Open or shorted address or data bus lines.
2. Bad microprocessor chip.
3. Bad bus buffers.
4. Bad ROM.
5. Bad RAM.
6. Any bad input or output that causes an address or data line to be held in a constant high or low state.

A pulsing $\overline{RESET}$ signal indicates a problem exists somewhere within the microprocessor circuitry rather than within the analog vector-generator. To aid in troubleshooting, the $\overline{WDDIS}$ test point can be connected to a ground test point to prevent resets. This will sometimes allow the Self-Test to be used to diagnose the failure during a RESET condition. □

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SP-209 Sheet 13B
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Waveform

A IC401 8 — 7.5Vp-p V

I IC401 17 — 4.5Vp-p H

B IC401 5 — 0.05Vp-p V

J IC401 15 — 2.5Vp-p H

C IC401 3 — 2Vp-p V

K IC401 14 — 5Vp-p H

D R451~R452 — 0.5Vp-p V

L IC401 12 — 5.6Vp-p H

E Q452 B — 1.3Vp-p H

M Q501 B — 0.7Vp-p H

F Q451 E — 90Vp-p V

N Q501 C — 700Vp-p H

G IC401 1 — 0.4Vp-p H

O — 1.3Vp-p H

H IC401 18 — 1.4Vp-p V

P — 900Vp-p H

NOTE

1 RESISTOR
All resistors are carbon 1/4W resistor unless otherwise noted the following marks unit of resistance is OHM 1K = 1,000 M = 1,000,000
- Solid
- Wire Wound
- Non Flame
- Cement
- Metal Oxide
- Thermistor
- Fuse

2 CAPACITOR
All capacitors are ceramic 50V capacitor unless otherwise noted the following marks unit of capacitance is P unless otherwise noted
- Electrolytic
- Bipolar
- Z type
- Dipped Tantalum
- Safety Vert
- Titanium Dioxide
- Temp Compensation
- Polystyrene
- Polypro pylene
- Polyester

3 COIL
Unit of inductance μH

4 TEST POINT
Test pin no position

J PRINT TNP 56507ZA DEGAUSS

TLK1507Z DEGAUSSING COIL

J3

Q801 2SD692 or 2SC1629A AVR

IC401 EN1235 H-OSC H-PREDRIVE V-OSC DRIVE

6P CONNECTOR AMP 640386-6 — RED, GREEN, BLUE, GND, SYNC

N PRINT TNP4513IZA VIDEO AMP

Q303~311 2SC1685(Q) or 2SD637(Q)

R-CONTRAST, G-CONTRAST, B-CONTRAST, BRIGHT

D PRINT TNP66356

V-POSITION, H-POSITION, H-SIZE

MAIN PRINT TNP61869LC

CHASSIS METAL

SW301 ESD7022

Q451 2SC1683(L,B)P,Q V-OUT

Q452 2SC1683(L,B)P,Q V-OUT

Q501 2SC1905-B,LB or 2SC1505(I) H-DRIVE

Q551 2SD649Q H-OUT

Q552 2SC1226-P,Q,R 12V REG

Q553 2SD637-Q or 2SC1685-Q or 2SC945A H OSC DISABLE AMP

Q554 2SB642-Q or 2SA564A-Q H OSC DISABLE OUT

Q802 2SC1473NC or 2SC1573 or 2SC1941 REF AMP

T501 TLH6434

T551 TLF6041F FBT

L551 TSC909, L552 TSC909

L555 TLH6698P, L556 TLH6698P

L554 TLP408C

D401 MA162

D420 RM12M

D803 RM12M or 8J202 or 8Q102

F801 4A 125V

F802 LSA 125V

TJF1388 MOLEX CONNECTOR

FROM FOCUS CONTROL

SCREEN

180V LINE

PICTURE TUBE S10ITP22AW

FROM EHT

Q352 2SC2923 G-OUT

Q351 2SC2923 B-OUT

Q353 2SC2923 R-OUT

B-DRIVE, R-DRIVE, LOW LIGHT

TNP11998ZA C.R.T. PRINT

FOCUS BLOCK EVM8RG 2K5T8

To R536, To R534, To CRT ANODE, To R207

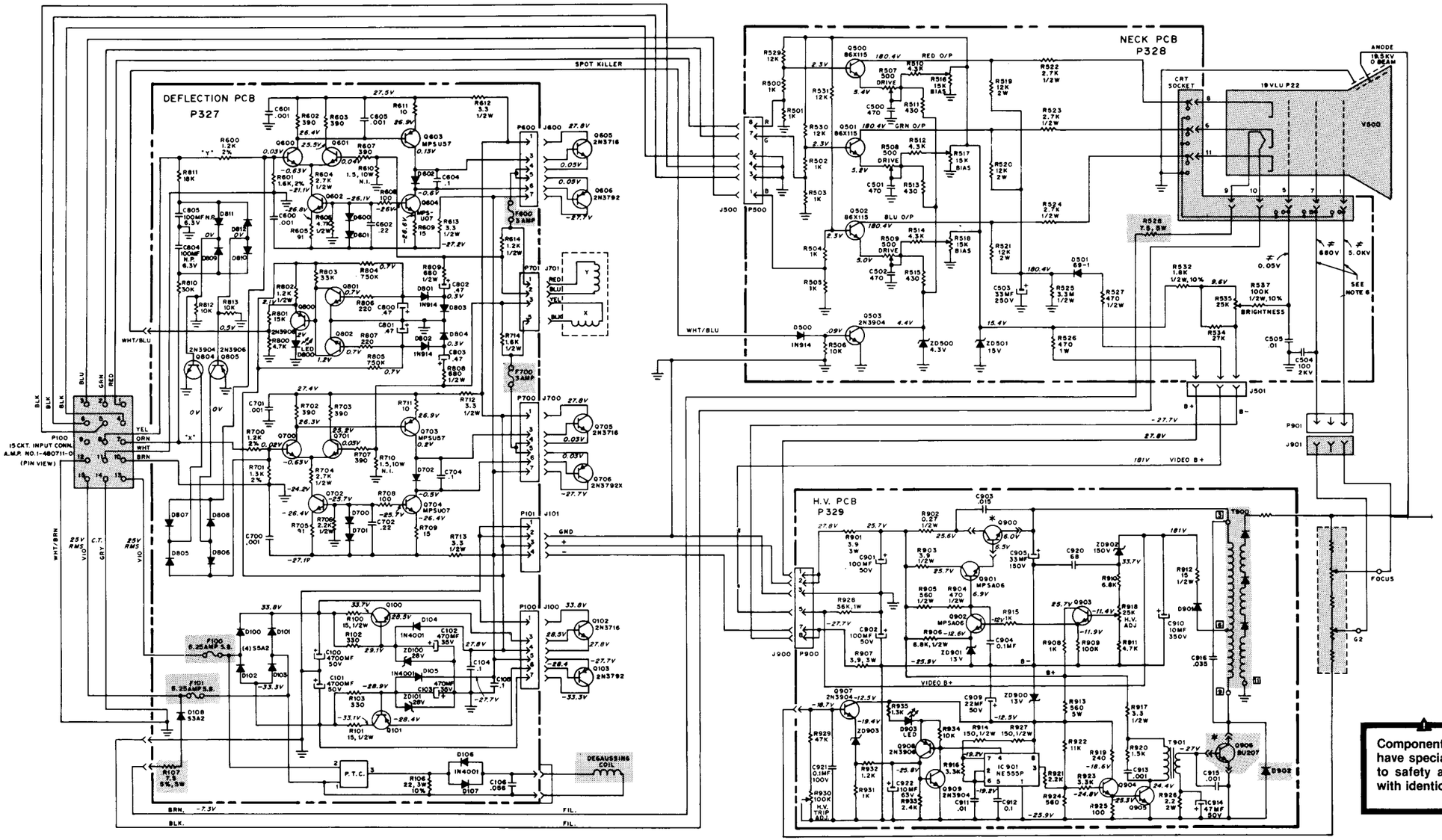
+20V, 80V, HEATER

DEFLECTION YOK TLY5328P

WARNING

Components identified by shading have special characteristics important to safety and must be replaced only with identical parts.

Matsushita Color Raster Display Schematic

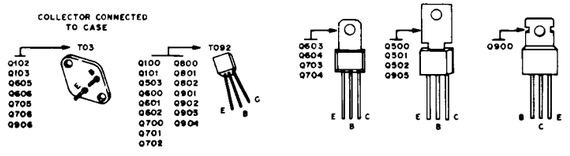


WARNING

Components identified by shading have special characteristics important to safety and must be replaced only with identical parts.

GENERAL NOTES:

1. RESISTANCE VALUES IN OHMS 1/4 WATT, 5% UNLESS OTHERWISE NOTED. K=1,000, M=1,000,000
2. CAPACITANCE VALUE OF 1 OR LESS IN MICROFARADS, ABOVE 1 IN PICOFARADS UNLESS OTHERWISE NOTED.
3. * Q900 AND Q908 ARE NOT ON H.V.P.C.B.
4. ALL D.C. VOTAGES ±10% MEASURED FROM POINT INDICATED TO GROUND USING A HIGH IMPEDANCE METER. VOLTAGES ARE MEASURED WITH NO SIGNAL INPUT AND CONTROLS ARE IN A NORMAL OPERATING POSITION
5. CIRCLED NUMBERS INDICATE LOCATION OF WAVE-FORM READING.
6. USE A 1,000:1 PROBE WHEN MEASURING SCREEN OR FOCUS VOLTAGE.
7. ≠ VOLTAGES VARY WITH CONTROL SETTINGS.



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Wells-Gardner Color Raster Display Schematic

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SP-209 Sheet 14B

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Electrohome 19-Inch Color Raster-Scan Video Display Schematic Diagram

Schematic Notes

Unless otherwise specified
Resistance: (Ω) (K→KΩ, M→MΩ), 1/4 (W) carbon resistor
Capacitance: 1 or higher→ (pF), less than 1→ (μF)
working voltage→ 50 (V)
ceramic capacitor
Inductance: (μH)
Electrolytic Cap: Capacitance Value (μF)/working voltage (V),
NP → non-polar (or bipolar) electrolytic cap.
Refer to the parts list for additional component information.

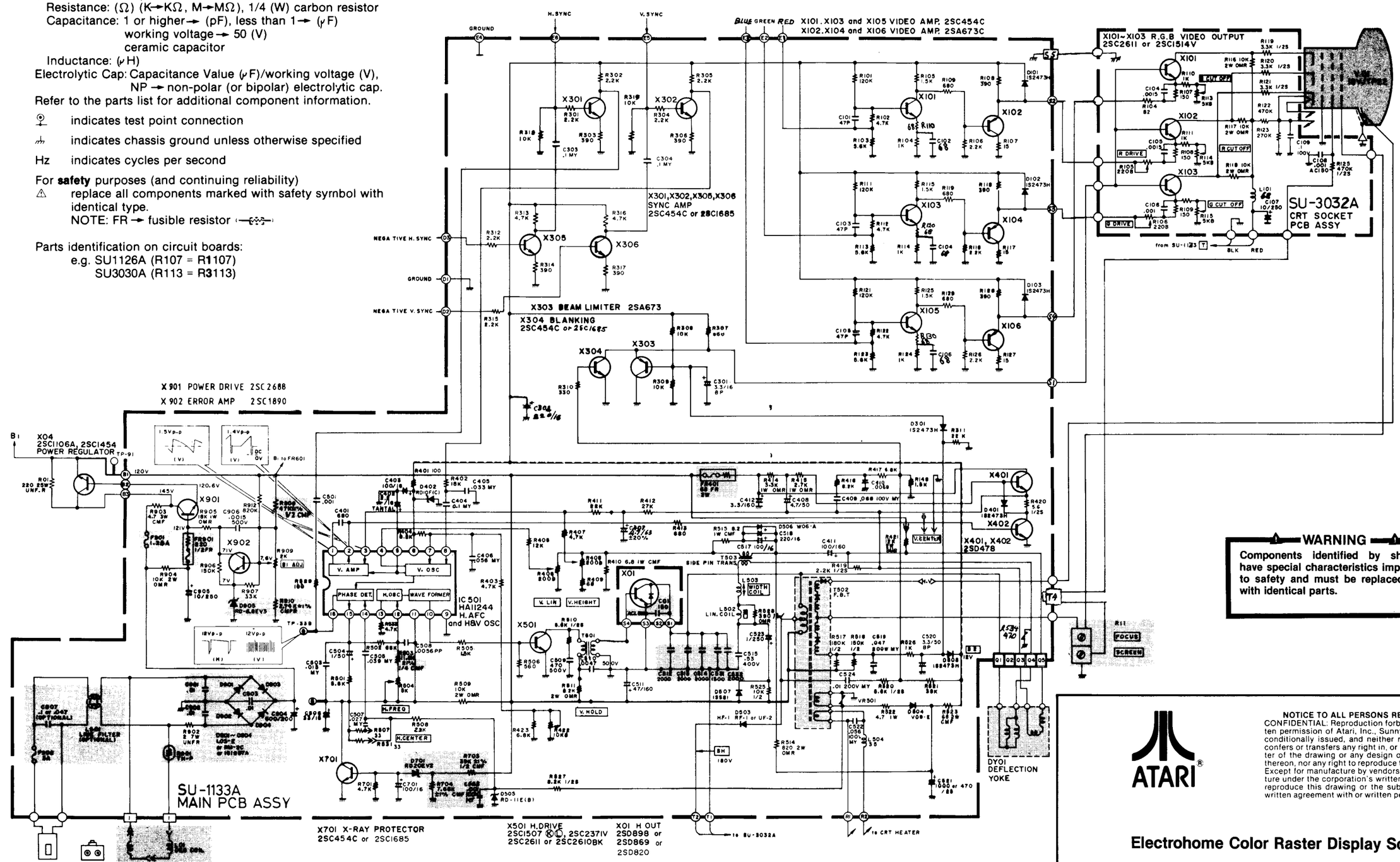
⊙ indicates test point connection

⏚ indicates chassis ground unless otherwise specified

Hz indicates cycles per second

For **safety** purposes (and continuing reliability)
⚠ replace all components marked with safety symbol with identical type.
NOTE: FR → fusible resistor

Parts identification on circuit boards:
e.g. SU1126A (R107 = R1107)
SU3030A (R113 = R3113)



WARNING

Components identified by shading have special characteristics important to safety and must be replaced only with identical parts.

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Electrohome Color Raster Display Schematic

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