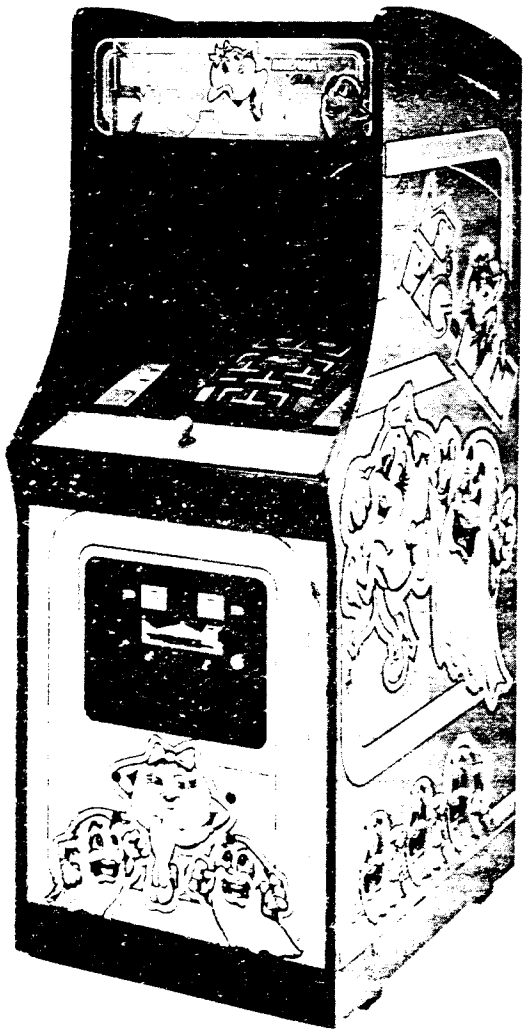
MIDWAY'S

PAC-MAN & MS. PAC-MAN™

TROUBLE SHOOTING LOGIC BOARD
PART II



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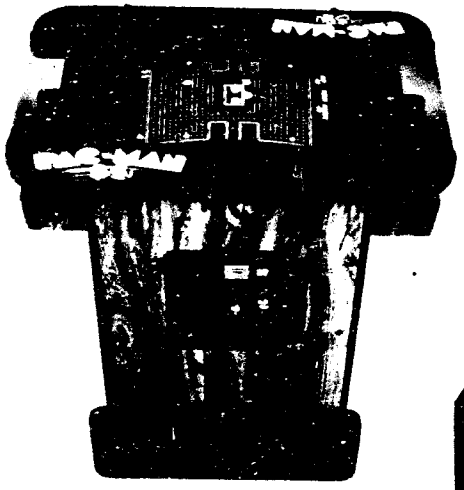

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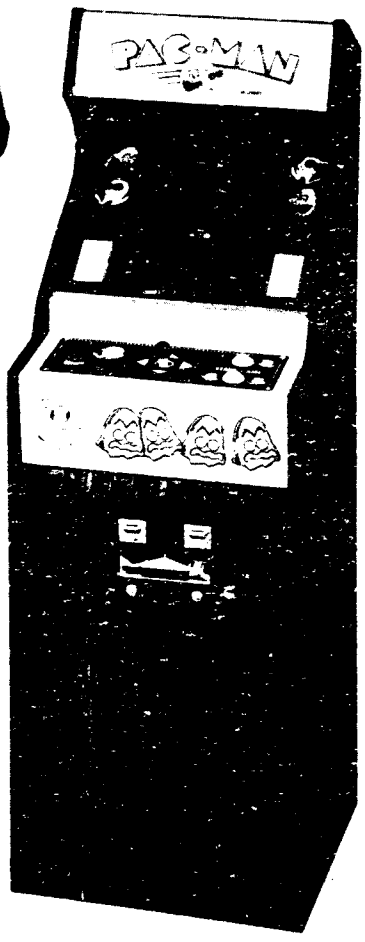

MINI #934

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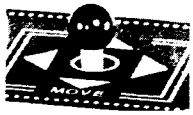
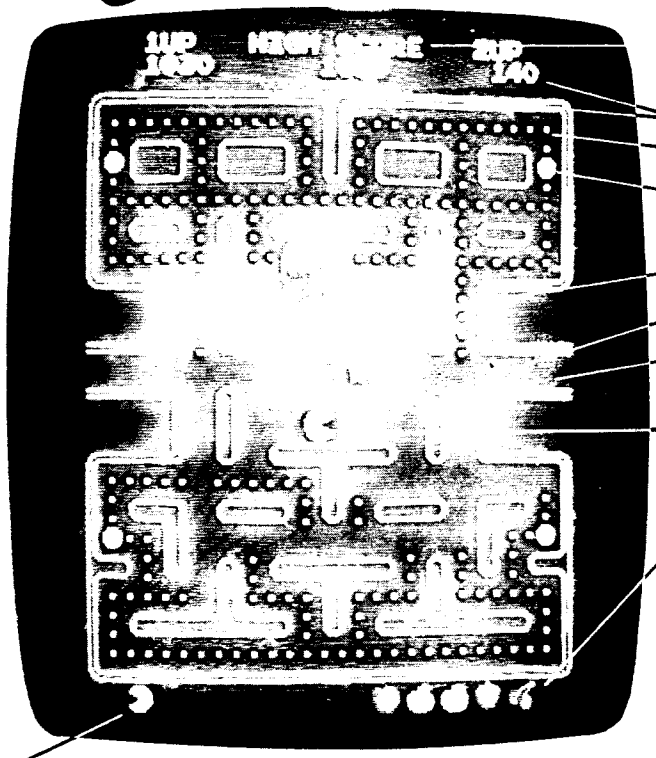
PAC-MAN

A sensational, full color video game for 1 or 2 players that tickles vision and challenges reflexes. Adding to the fun are musical refrains, chomping and action sounds along with amusing cartoon shows between racks.



The player, using a single handle control guides the PAC-MAN about the maze, scoring points by munching up the Dots in his path. Four Ghost Monsters—Inky, Blinky, Pinky and Clyde— chase after the PAC-MAN trying to capture and deflate him. The PAC-MAN can counterattack by eating the big, Power Capsule that enables him to overpower the Monsters for additional score. After all the Dots are gobbled up, the screen is cleared, and PAC-MAN continues for another round. Each rack features a special Fruit Target in the maze, which if eaten, earns Bonus Points. Players start with three PAC-MEN. An additional PAC-MAN is awarded for 10,000 points.



HIGH SCORE — Retained and displayed daily.

PLAYERS' SCORE

DOTS — 10 Points Each.

POWER CAPSULE — 50 Points Each.

GHOST MONSTERS

PAC-MAN — The 'main' man.

ESCAPE 'Warp' TUNNEL — Out one side– reappear on other.

BONUS FRUIT TARGET — Appear below Monster's Den twice during each rack.

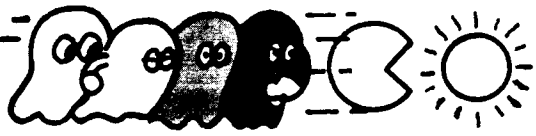
NUMBER OF SCREENS CLEARED — Fruit indicates how many times player has cleared the screen of dots.

- Screen cleared once.
- Screen cleared twice.
- Screen cleared 3 times.
- ? Screen cleared 4 times.
- ? Screen cleared 5 times.

— etc. —

PAC-MAN REMAINING

1 Quick, eat the flashing Power Capsule.



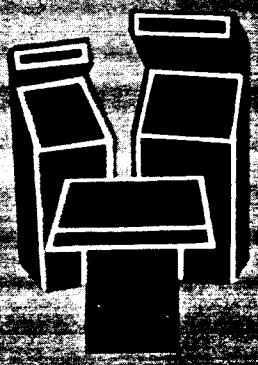
Inky Blinky Pinky Clyde

2 When the PAC-MAN powers up, the Monsters start to run away.

3 Points double for each Monster caught.

1600 800 400 200

PAC-MAN is available in 3 Midway models: New Mini-Myte, Cocktail Table and Standard Arcade.



58½" 149 cm	19½" 49.5 cm	24" 61 cm
29" 74 cm	32" 81.25 cm	22" 56 cm
73" 185.5 cm	26½" 67.25 cm	34" 86.25 cm

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NOTES

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INTRODUCTION

Midway's new games, Pac-Man and Ms. Pac-Man, promises to be two of the hottest new games on the market today. As with any high production product, there will be a need for servicing from time to time. Therefore, since necessity is the mother of invention, this manual is being written to satisfy that need and to simplify trouble-shooting.

So use this manual to its fullest potential, GOOD LUCK!

PAC-MAN & MS. PAC-MAN

OPTION SWITCH SETTINGS

METHOD OF PLAY

	SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8
FREE PLAY	ON	ON						
1 COIN 1 PLAY	OFF	ON						
1 COIN 2 PLAYS	ON	OFF						
2 COINS 1 PLAY	OFF	OFF						

NUMBER OF MS. PAC-MEN PER GAME

	SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8
1 MS. PAC-MAN	ON	ON						
2 MS. PAC-MEN	OFF	ON						
3 MS. PAC-MEN	ON	OFF						
5 MS. PAC-MEN	OFF	OFF						

BONUS MS. PAC-MEN

	SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8
BONUS MS. PAC-MAN AT 10,000 POINTS	ON	ON						
BONUS MS. PAC-MAN AT 15,000 POINTS	OFF	ON						
BONUS MS. PAC-MAN AT 20,000 POINTS	ON	OFF						
NO BONUS	OFF	OFF						

SPECIAL FUNCTIONS

	SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8
AUTOMATIC RACK ADVANCE	ON	OFF						
FREEZE VIDEO (MONITOR PRESENTATION STOPS MOVING)	OFF	ON						
GAME OPERATES NORMALLY	OFF	OFF						

Troubleshooting

Introduction

The most common problems occur in harness components such as the coin acceptor, player controls, interconnecting wiring, etc. The TV monitor and PCB computer cause their share of problems too, but not as much as the harness and its component parts. TV monitor troubleshooting will not be covered here because it is covered in that section of this manual.

As you already know, the PCB computer is a complex device with a number of different circuits. Some circuits remain basically the same among games, but overall there are a great many differences between them. PCB troubleshooting procedures, therefore, can be lengthy and will differ greatly among games. However, some basic Z-80 CPU information is involved in this section.

General Suggestions

The first step in any troubleshooting procedure is correctly identifying the malfunction's symptoms. This includes not only the circuits or features malfunctioning, but also those still operational. A carefully trained eye will pick up other clues as well. For instance, a game in which the computer functions fail completely just after money was collected may have a quarter shorting the PCB traces. Often, an experienced troubleshooter will be able to spot the cause of the problem even before opening the cabinet.

After all the clues are carefully considered, the possible malfunctioning areas can be narrowed down to one or two good suspects. Those areas can be examined by a process of elimination until the cause of the malfunction is discovered.

Harness Component Troubleshooting

Typical problems falling in this category are coin and credit problems, power problems and failure of individual features.

NO GAME CREDIT

For example, your prospective player inserts his quarter and is not awarded a game. The first item to check is if the quarter is returned. If the quarter is returned, the malfunction most certainly lies in the coin acceptor itself. First, use a set of test coins (both old and new) to ascertain that the player's coin is not undersize or underweight. If your test coins are also returned, coin acceptor servicing is indicated. Generally, the cause of this particular problem is a maladjusted magnet gate. Normally, this will mean slightly closing the magnet gate a little by turning the adjusting screw out a bit (see section on coin acceptor for more details).

If the quarter is not returned and there is no game credit, the cause of the malfunction may be in one of several areas. First try operating the coin return button; if the coin is returned, the problem is most likely in the magnet gate. Enlarge the gap according to the coin acceptor service procedures. If this does not cure the problem, remove the coin acceptor, clean it and perform the major adjustment procedure.

If the trapped coin is not returned when the wiper lever is actuated, you may have an acceptor jammed by a slug, gummed up with beer, a jammed coin chute, or mechanical failure of the acceptor mechanism. In this case, first check for the slug that will generally be trapped against the magnet. If so, simply remove the slug and test the acceptor. If the chute is blocked, remove the acceptor and remove the jammed coins. If there is actual failure of the acceptor, remove the unit and repair as indicated in the coin acceptor service procedures.

If the coin is making its way through the acceptor (that is, falling into the coin box), yet there is still no game credit, you either have a mechanical failure of the coin switch or electrical failure of the coin and credit circuits. The first place to begin is by checking the coin switch. Most of these switches are the make/break variety of micro switch, which is checked by testing for continuity between the NO, NC, and C terminals. When not actuated, the NC and C terminals should be continuous and the NO terminal open. When operated, the NO and C terminals should close and the NC should be open. If the coin switch checks out, examine the connections to the terminals to make sure there is good contact. If necessary, use the continuity tester and check from the terminal lug on the switch to the associated PCB trace. This will tell you if there is a continuous line all the way to the credit circuit.

If the coin switch wires do not check out, the problem is in the computer — most likely in the coin and credit circuitry.

If you do get game credit when a coin is deposited, but the game will not start when the start switch is pressed, you may have a problem in the start switch, the interconnecting wiring or in the computer. First check the switch. If the switch is OK, proceed to check the wiring. Again, make sure you go from the terminal lug on the switch to the PCB trace. This way, you will check the terminal contact as well as PCB edge connector contact. If the wiring is continuous, proceed to check the PCB credit circuit. If not, check each section of the wiring, until the discontinuity is located. If the wiring is OK, the problem must lie in the computer.

Transformer and Line Voltage Problems

Your machine must have the correct line voltage to operate properly. If the line voltage drops too low, a circuit in the computer will disable game credit. The point at which the computer will fail to work will vary some from game to game, but no game will work on line voltage that drops below 105 VAC.

Low line voltage may have many causes. Line voltage normally fluctuates a certain amount during the day as the total usage varies. Peak usage times occur mainly at dawn or dusk, so if your machine's malfunction seems to be related to the time of day, this may be a factor. A large load connected to the same line as the game (such as a large air conditioner or other device with an exceptionally large motor) may drop the line voltage significantly when starting up. This drop can result in an intermittent credit problem. In addition, poor connections in the location wiring, plug, or line cord may also cause a significant drop in power. Cold solder joints in the game's harness, especially in areas like the transformer connections, interlock switch, or fuse block, may also produce the same results, although probably on a more permanent basis.

Sometimes location owners (especially in bars) replace light switches with dimmer rheostats, and the game is sometimes on the same line. Obviously, the voltage available to the game is going to drop dramatically when the dimmer is turned.

In any case, the way to check for correct line voltage is with your VOM. Set the VOM to 250 VAC and stick the probes in the wall receptacle. If it's OK here, check the transformer primary connections. If you do not get 117 VAC, examine the solder joints on the transformer, fuse block, and interlock switch. If you do get 117 VAC, the problem must be either in the transformer, harness connections, or in the PCB power supply.

If you suspect the transformer, check its secondaries with the VOM set to 50 VAC and correlate the readings with the legend on the side of the transformer. The transformer must also be correctly grounded, so check the ground potential as well, especially if there is a hum bar rolling up or down the TV screen.

HARNESS PROBLEMS

Other harness problems include blowing fuses and malfunctioning controls. The repeating blown-fuse problem can sometimes be quite exasperating to solve, for short circuits have the tendency to occur in areas almost impossible to find. First, try inserting a new fuse, as old fuses age and blow without cause. If the new one also blows, you definitely have a short.

The best way to approach this problem is by turning the power off and disconnecting devices that may be causing the problem, such as the TV, transformer, and PCB. Disconnect the devices by pulling off their connectors, but do not allow them to touch. If necessary, insulate them with small pieces of electrical tape. Then, connect your VOM across the terminals of the fuse block (all electrical power shut off), and set it to one of the resistance scales. This will save blowing a fuse each time you want to check the circuit.

If the VOM reveals that disconnecting the devices removed the short, reconnect the devices one by one until the short returns. The last device connected is the one that is at fault. If the VOM reads a short even after the devices are disconnected, the fault must lie in the harness itself, and only patient exploration will reveal its location. First, carefully examine all the wiring, looking for terminals that may be touching, metal objects such as coins shorting connections or burned insulation. If necessary, use the VOM to check each suspected wire.

MALFUNCTIONING CONTROLS

One of the most common problems here is a bad potentiometer. Typically, a bad pot will cause the image to jump as it reaches a certain point. The only cure for this one is to install a new pot.

If a feature that is operated by a switch (for example, joysticks, foot pedals, control panel buttons) does not operate at all, check the switch with a VOM or continuity tester to verify its operation. If the switch does not check out, replace it. If the switch is OK, you should suspect the input to the switch from the PCB. In this case, get out the harness and logic schematics and check to see what kind of input it is. In many cases, the input will be +5 VDC. If so, use the VOM to check its presence. Normally, the switch is used to pull a +5 VDC line LOW to GND or to pull a LOW line HIGH. If the PCB output is missing, check the wire length from the PCB. If you find the signal at the PCB trace, the wire length or connection is at fault. If not, begin exploring the PCB using the logic schematics.

A Glossary of Microprocessor Terms

MICROPROCESSOR — one or several microcircuits that perform the function of a computer's CPU. Sections of the circuit have arithmetic and comparative functions that perform computations and executive instructions.

CPU — central-processing unit. A computing system's "brain", whose arithmetic, control and logic elements direct functions and perform computations. The microprocessor section of a microcomputer is on one chip or several chips.

PROM — programmable read-only memory. User permanently sets binary on-off bits in each cell by selectively fusing or not fusing electrical links. Nonerasable. Used for low-volume applications.

EPROM — erasable, programmable, read-only memory. Can be erased by ultraviolet light bath, then reprogrammed. Frequently used during design and development to get programs debugged, then replaced by ROM for mass production.

ROM — read-only memory. The program, or binary on-off bit pattern, is set into ROM during manufacture, usually as part of the last metal layer put onto the chip. Nonerasable. Typical ROM's contain up to 16,000 bits of data to serve as the microprocessor's basic instructions.

RAM — random-access memory. Stores binary bits as electrical charges in transistor memory cells. Can be read or modified through the CPU. Stores input instructions and results. Erased when power is turned off.

LSI — large scale integration. Formation of hundreds or thousands of so-called gate circuits on semiconductor chips. Very large scale integration (VLS) involves microcircuits with the greatest component density.

MOS — metal-oxide semiconductor. A layered construction technique for integrated circuits that achieves high component densities. Variations in MOS chip structures create circuits with speed and low-power requirements, or other advantages (static will damage a MOS chip).

Introduction to the Z-80 CPU

The term "microcomputer" has been used to describe virtually every type of small computing device designed within the last few years. This term has been applied to everything from simple "microprogrammed" controllers constructed out of TTL MSI up to low end minicomputers with a portion of the CPU constructed out of TTL LSI "bit slices." However, the major impact of the LSI technology within the last few years has been with MOS LSI. With this technology, it is possible to fabricate complete and very powerful computer systems with only a few MOS LSI components.

The Zilog Z-80 family of components can be configured with any type of standard semiconductor memory to generate computer systems with an extremely wide range of capabilities. For example, as few as two LSI circuits and three standard TTL MSI packages can be combined to form a simple controller. With additional memory and I/O devices a computer can be constructed with capabilities that only a minicomputer could previously deliver.

New products using the MOS LSI microcomputer are being developed at an extraordinary rate. The Zilog Z-80 component set has been designed to fit into this market through the following factors:

1. The Z-80 is fully software compatible with the popular 8080A CPU.
2. Existing designs can be easily converted to include the Z-80.
3. The Z-80 component set is at present superior in both software and hardware capabilities to any other microcomputer system on the market today.
4. For increased throughput the Z80A operating at a 4 MHZ clock rate offers the user significant speed advantages.

Microcomputer systems are extremely simple to construct using Z-80 components. Any such system consists of three parts:

1. **CPU (Central Processing Unit)**
2. **Memory**
3. **Interface Circuits to peripheral devices**

The CPU is the heart of the system. Its function is to obtain instructions from the memory and perform the desired operations. The memory is used to contain instructions and in most cases data that is to be processed. For example, a typical instruction sequence may be to read data from a specific peripheral device, store it in a location in memory, check the parity and write it out to another peripheral device. Note that the Zilog component set includes the CPU and various general purpose I/O device controllers, while a wide range of memory devices may be used from any source. Thus, all required components can be connected together in a very simple manner with virtually no other external logic.

General Purpose Registers

There are two matched sets of general purpose registers, each set containing six 8-bit registers that may be used individually as 8-bit registers or as 16-bit register pairs by the programmer. One set is called BC, DE and HL while the complementary set is called BC', DE' and HL'. At any one time the programmer can select either set of registers to work with through a single exchange command for the entire set. In systems where fast interrupt response is required, one set of general purpose registers and an accumulator/flag register may be reserved for handling this very fast routine. Only a simple exchange command need be executed to go between the routines. This greatly reduces interrupt service time by eliminating the requirement for saving and retrieving register contents in the external stack during interrupt or subroutine processing. These general purpose registers are used for a wide range of applications by the programmer. They also simplify programming, especially in ROM based systems where little external read/write memory is available.

Arithmetic & Logic Unit (ALU)

The 8-bit arithmetic and logical instructions of the CPU are executed in the ALU. Internally the ALU communicates with the registers and the external data bus on the internal data bus. The type of functions performed by the ALU include:

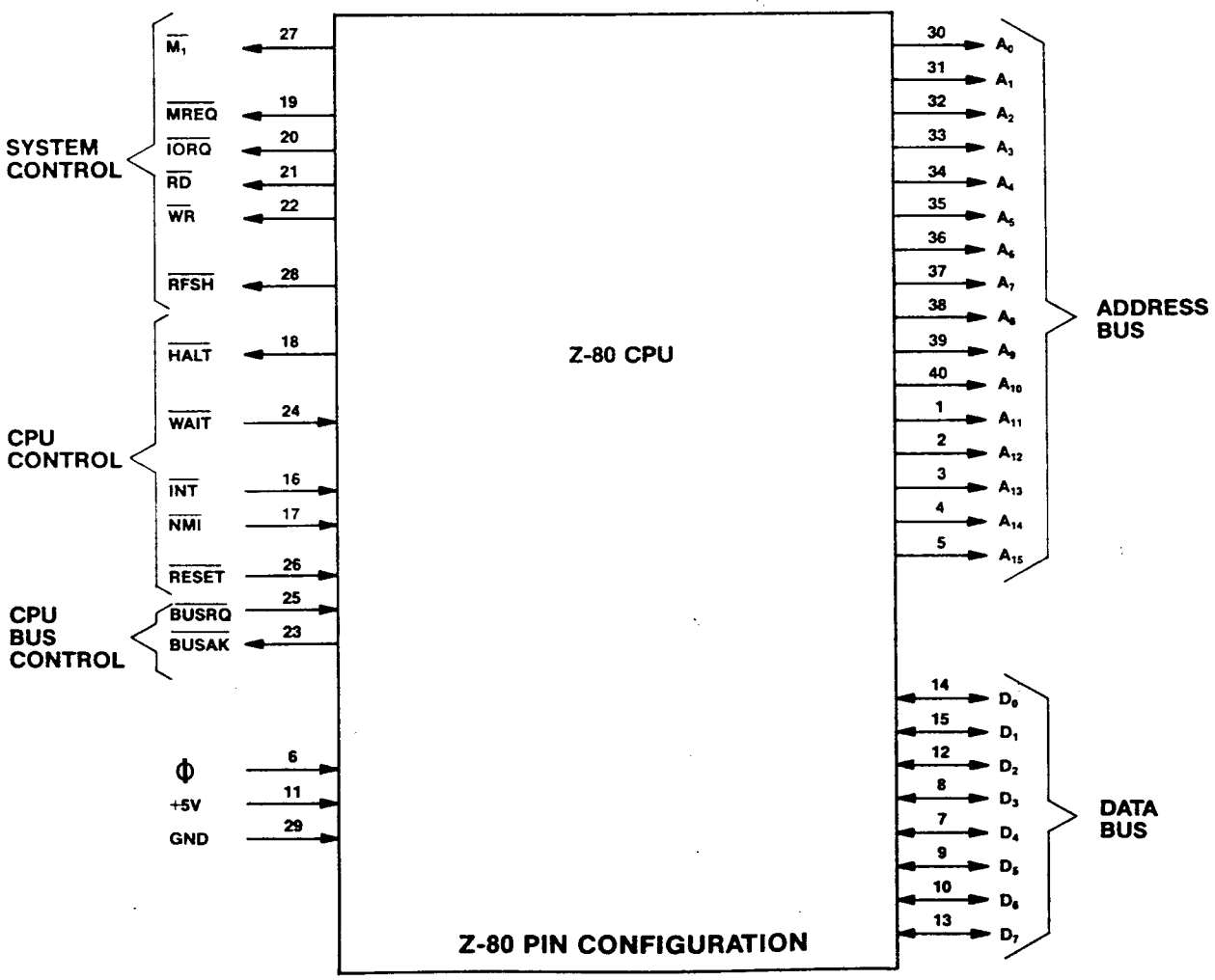
Add	Left or right shifts or rotates (arithmetic and logical)
Subtract	Increment
Logical AND	Decrement
Logical OR	Set bit
Logical Exlusive OR	Reset bit
Compare	Test bit

Instruction Register and CPU Control

As each instruction is fetched from memory, it is placed in the instruction register and decoded. The control sections performs this function and then generates and supplies all of the control signals necessary to read or write data from or to the registers, control the ALU and provide all required external control signals.

Z-80 CPU Pin Description

The Z-80 CPU is packaged in an industry standard 40 pin Dual In-Line Package. The I/O pins are shown in the below figure and the function of each is described.



A_0-A_{15}
(Address Bus)
Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to directly select up to 256 input or 256 output ports. A_0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.

D_0-D_7
(Data Bus)
Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

M_1
(Machine Cycle one)
Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes, $\overline{M1}$ is generated as each op code byte is fetched. These two byte op-codes always begin with CBH, DDH, EDH or FDH. $\overline{M1}$ also occurs with $\overline{IORQ}$ to indicate an interrupt acknowledge cycle.

MREQ
(Memory Request)
Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

IORQ
(Input/Output Request)
Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated with an $\overline{M1}$ signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during M_1 time while I/O operations never occur during M_1 time.

RD
(Memory Read)
Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

WR
(Memory Write)
Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

RFSH
(Refresh)
Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current MREQ signal should be used to do a refresh read to all dynamic memories.

HALT
(Halt state)
Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

WAIT
(Wait)
Input, active low. $\overline{WAIT}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.

INT
(Interrupt Request)
Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the $\overline{BUSRQ}$ signal is not active. When the CPU accepts the interrupt, an acknowledge signal ($\overline{IORQ}$ during M_1 time) is sent out at the beginning of the next instruction cycle. The CPU can respond to an interrupt in three different modes that are described in detail in section 5.4 (CPU Control Instructions).

NMI
(Non-Maskable Interrupt)
Input, negative edge triggered. The non maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066_H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous $\overline{WAIT}$ cycles can prevent the current instruction from ending, and that a $\overline{BUSRQ}$ will override a $\overline{NMI}$.

RESET
Input, active low. RESET forces the program counter to zero and initializes the CPU. The CPU initialization includes:

1) Disable the interrupt enable flip-flop

2) Set Register I = 00_H

3) Set Register R = 00_H

4) Set Interrupt Mode 0

During reset time, the address bus and data bus go to a high impedance state and all control ouput signals go to the inactive state.

BUSRQ
(Bus Request)

Input, active low. The bus request signal is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these buses. When BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated.

BUSAK
(Bus Acknowledge)

Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

CLK
(Clock)

Single phase TTL level clock which requires only a 330 ohm pull-up resistor to +5 volts to meet all clock requirements.

PAC - MAN

TROUBLE SHOOTING
PC A082-91375-A000

NOTE: All I.C. trouble shooting information is with the I.C. removed from circuit.

POSITION	CHIP	POSSIBLE TROUBLE
1-E	74LS161	All Characters are at top of screen - Characters move horizontally only.
1-F	74LS283	Lines and Squares entire screen - Effects Self Test.
1-H	74LS283	Horizontal lines across screen in color.
1-K	74LS283	No Sounds - Game plays normal.
1-L	74LS174	Same as 1-K
1-M	5623 (Prom)	Same as 1-K
1-N	CD 4066	Same as 1-K
2-A	93415 (Ram)	Effects Color of all Characters - Game plays.
2-B	93415 (Ram)	Same as 2-A
2-C	93415 (Ram)	Same as 2-A
2-D	93415 (Ram)	Effects Color of the Characters - Eyes only two Characters.
2-E	74LS161	Characters top of screen - Characters move horizontally - Effects Game Play - Color & Sound OK.
2-F	74LS283	Effects Self Test - Row of Characters horizontally across screen. Effects Game Play - Color & Sound OK.
2-H	74LS86	All Characters are Squares - Effects Self Test - Horizontal Color Bars across screen.
2-K	74LS89	Effects all Sounds - Game plays & color OK.
2-L	74LS89	Same as 2-K
2-M	74LS273	Same as 2-K
2-P	74LS02	Effects Sync - No Video - No Sound - Moving Diagonal Lines.
2-R	74LS161	Vertical short lines in color - Effects Game Play.
2-S	74LS161	Horizontal Color Bars across screen - Effects Game Play.

POSITION	CHIP	POSSIBLE TROUBLE
3-A	74LS158	No Characters in maze.
3-B	74LS157	No Video (Dead)
3-D	74LS75	Characters missing in maze - Game plays without seeing Characters.
3-E	74LS20	No Video (Dead)
3-F	74LS89	Same as 3-D
3-H	74LS89	All Characters move jerking - Characters do not stay in maze.
3-K	74LS158	No Sounds - Game Plays.
3-L	74LS157	Same as 3-K
3-M	1M5623	Same as 3-K
3-N	74LS74	Effects Sync - Color Diagonal Lines.
3-P	74LS10	No Video (Dead)
3-R	74LS161	No Video (Dead)
3-S	74LS161	Effects Sync - Diagonal Lines.
4-A	1M5623 (Prom)	No Video (Dead)
4-B	74LS377	Distorted Letters - No Color - Maze is White - Effects Game Play.
4-C	74LS00	No Video (Dead)
4-D	74LS273	No Maze - Screen covered with Number Fives - No Letters - Characters moving about.
4-E	74LS157	Distorted Maze - Letters Upside Down - Characters Distorted.
4-F	74LS86	Distorted Characters - Letters and Sound.
4-H	74LS245	Flashing White Dots - No Color.
4-K	2114 (Ram)	All White Zeros on screen.
4-L	2114 (Ram)	Flashing Numbers and Letters in Color.
4-M	2114 (Ram)	Blank screen with a Single Zero at top of screen - Two Red Characters Only.
4-N	2114 (Ram)	Same as 4-K
4-P	2114 (Ram)	Flashing Self Test - Flashes continuous.

POSITION	CHIP	POSSIBLE TROUBLE
4-R	2114 (Ram)	Screen is blank with a Number One flashing - A single Character can be seen.
5-A	74LS157	Blue Screen - All Characters are Squares - No Letters or Numbers.
5-B	74LS194	Color Squares around each Character - All maze dots are blue.
5-C	74LS194	Effects Maze - Characters have Squares around them - Self Test in Red.
5-E	9332 (Prom)	Blue screen with Horizontal Squares - No Maze - No Letters or Numbers random Characters.
5-F	9332 (Prom)	Effects Characters in Maze which are Squares - Everything else normal.
5-L	74LS139	Red screen flashing with all Letter F's.
5-M	74LS74	Screen covered with Garbage in Color.
5-N	74LS08	Effects Sync - Moving Diagonal Lines in Color.
5-S	NVC 284 (Custom)	Flashing White Dots - Game plays.
6-B	Z80 CPU	Screen covered with Garbage in Color.
6-D	NVC 285 (Custom)	Same as 6-B
6-E	9332-B (Prom)	Flashing blue Zeros and Garbage - Continuous Meter Pulses.
6-F	9332-B (Prom)	Blank screen with a Flashing Number One - Bad Rom One.
6-H	9332-B (Prom)	Screen covered with Garbage.
6-J	9332-B (Prom)	Blank screen with random Characters.
6-R	74LS367	Screen flashing with Garbage in Color.
6-S	74LS367	Same as 6-R
7-F	7603	No Video (Dead)
7-H	74LS08	Eleven Horizontal rows of Zeros across screen.
7-J	74LS138	No Video (Dead)
7-K	74LS138	No Video (Dead)
7-L	74LS02	Same as 7-J
7-M	74LS139	Screen covered with Garbage in Color.
7-N	74LS42	Same as 7-J

POSITION	CHIP	POSSIBLE TROUBLE
8-A	74LS107	No Video (Dead)
8-B	74LS368	Same as 8-A
8-C	74LS74	Effects Sync - Diagonal Lines flashing.
8-D	74LS367	Effects Dip Switch settings.
8-E	74LS367	No Coin - No Up & Down Controls - 1st Player.
8-F	74LS367	No Controls - 2nd Player.
8-H	74LS367	No Test Switch - 1 & 2 Player Select.
8-K	74LS259	Stays in Self Test - Shows Memory OK.
9-C	74LS161	Screen covered with Garbage in Color.
11-A	LM377 — LM1877	No Sounds.

ADDITIONAL DEVICES

10-A	Dip Switch	Effects Coin Play - Number of Pac-Man Bonus Pac-Man.
B-7	Crystal (18.432)	No Video (Dead)
P-8 (IR1)	78GVIC (Regulator)	Effects +5 VDC
R-9	D44VM4	Pass Transistor - Effects +5 VDC
L-9	D40K1	Transistor - Effects Coin Counter
C-9	2N3391	Transistor - Effects Power Reset

SELF-TEST DISPLAY
AND BOARD LOCATION COORDINATES

MEMORY OK or (M-Rom-1 / Bad C Ram-0 / Bad W Ram-1 / etc.)

*1 COIN *1 CREDIT
BONUS *15000
MS. PAC-MAN *3
UPRIGHT or (TABLE)

* = switch selectable

If a bad ROM or Ram chip is found by the games internal check system during the Self-Test, the game indicates this to you by showing the location code of the bad chip(s) in place of the "MEMORY OK" message. The following table translates the chip location codes into actual positions on the game logic P.C. Board.

DISPLAY	DESCRIPTION
MEMORY OK	All RAMs are good.
BAD V RAM-0	RAM located on Logic PC board at position 4K is bad.
BAD V RAM-1	RAM located on Logic PC board at position 4N is bad.
BAD C RAM-0	RAM located on Logic PC board at position 4L is bad.
BAD C RAM-1	RAM located on Logic PC board at position 4P is bad.
BAD W RAM-0	RAM located on Logic PC board at position 4M is bad.
BAD W RAM-1	RAM located on Logic PC board at position 4R is bad.
MEMORY OK	All ROMs are good.
M-ROM-0	ROM located on Logic PC board at position 6E is bad.
M-ROM-1	ROM located on Logic PC board at position 6F is bad.
M-ROM-2	ROM located on Logic PC board at position 6H is bad.
M-ROM-3	ROM located on Logic PC board at position 6J is bad.

The detection of bad components on the Auxiliary Logic PC Board is not quite as simple as is the case for the Main Logic PC Board. The following table lists the components that are on this Auxiliary PC Board and what symptoms they will cause to appear on the monitor when each is bad.

---BAD COMPONENT/SYMPTON TABLE---

BAD COMPONENT	SYMPTOM DISPLAYED ON MONITOR (**GAME IS NOT IN SELF-TEST**)
Z-80 CPU	**STATIONARY** color garbage (parts of pictures) CPU located on Auxiliary PC board at position U4
E-ROM-0	Game goes through warm-up routine over & over & over--- ROM located on Auxiliary PC board at position U5
E-ROM-1	Game goes through warm-up routine over & over & over--- ROM located on Auxiliary PC board at position U6
E-ROM-2	**FLASHING** color garbage (parts of pictures) ROM located on Auxiliary PC board at position U7

---BAD COMPONENT/SYMPTON TABLE CONTINUED---

BAD COMPONENT	SYMPTOM DISPLAYED ON MONITOR (**GAME IS NOT IN SELF-TEST**)
CUSTOM CHIP CG-820	Monitor screen reads out "ROM 0" With game in Self-Test — Screen reads "BAD ROM-0" CG-820 located on Auxiliary PC board at position U0
CUSTOM CHIP CG-821	Monitor screen displays **FLASHING** color garbage (parts of pictures) CG-821 located on Auxiliary PC board at position U1
CUSTOM CHIP CG-822	Screen display is same as for CG-821. With game in Self-Test — Screen reads out **UPSIDEDOWN** "BAD W RAM-0" CG-822 located on Auxiliary PC board at position U2
CUSTOM CHIP CG-823	Screen display is same as for CG-821 CG-823 located on Auxiliary PC board at position U3

To check your game function switches and buttons (coin counter switches, TEST CREDIT button, 1 PLAYER and 2 PLAYER buttons): active each one while the game is in the Self-Test mode. You should hear a game sound for each activation. If you do not hear it, the switch/button is either not working, miswired, or disconnected. Check it out thoroughly.

When finished with the Self-Test mode, slide the Self-Test switch back to the "OFF" position.

- A cross hatch pattern appears on the monitor screen for about 1 to 2 seconds.
- If you wish to keep this test pattern on the monitor screen for further use, slide Self-Test switch to the "ON" position **after** the cross hatch pattern appears and **before** it disappears.
- When finished with the cross hatch pattern, set the Self-Test switch to the "OFF" position.
- Normal game functions will now return to the monitor screen.

OPTION SWITCH SETTINGS:

To change the option switch settings, you DO NOT have to take the Main Game Logic Board out of the game. They can be easily reached through the rear access door on the Upright and Mini models. On the Cocktail Table model, you do have to open the table top to reach them.

When changing any options, ALWAYS put the game into the Self-Test mode, make your changes, check the results on the monitor screen, take the game out of the Self-Test mode, and play the game to be sure the switches have worked properly and that no switches were accidentally moved that were not meant to be. (These switches are small and this can happen.)

The option switch settings and what they will make the game do, are shown in the following Figure.

PAC - MAN

TROUBLE SHOOTING LOGIC BOARD PC A082-91375-A000

1. CHECK +5VDC AT CPU AND ROMS.
2. RESET LINE PIN #26 OF CPU NORMALLY HIGH AND GOES LOW WITH RESET.
3. 6MHZ CLOCK FREQUENCY AT PIN #13 OF 8-B AND 3MHZ AT PIN #6 OF CPU.
4. CHECK ROM TEST FOR A MEMORY FAILURE.
5. CHECK ALL ADDRESS AND DATA LINES AT CPU.
6. CHECK ALL ADDRESS AND DATA LINES AT 4-A AND 7-F COLOR PROMS.
7. CHECK ALL ADDRESS AND DATA LINES AT 5-E AND 5-F CHARACTER ROMS.
8. WHEN CHARACTER ROM 5-E IS REMOVED GAME PLAYS BUT MAZE IS MISSING.
9. WHEN CHARACTER ROM 5-F IS REMOVED GAME PLAYS BUT PAC - MAN AND GHOST MONSTERS ARE BLOCKS OF COLOR.
10. WHEN ALL PROGRAM ROMS ARE REMOVED THE SCREEN WILL BE ROWS OF BLUE DIAGONAL LINES.
11. CHECK SOUNDS AND SWITCHES USING TEST SWITCH.
12. SWITCHES #7 AND #8 MUST BE OFF FOR NORMAL GAME PLAY.
13. SWITCH #7 ON WILL TEST RACKS.
14. GOOD LUCK!

NOTES

This space is provided for personal notes

POWER SUPPLY SECTION

The 12VAC and 12VCT lines are rectified to DC voltage by diodes D3 and D4. The Waveform Drawings may help to explain how this is done.

AC voltage is constantly alternating polarity. At one moment the 12VAC line at pin W is positive and the 12VAC line at pin X is negative when measured from 12VCT. The next moment pin X becomes positive and pin W negative. Between the *(asterick) marks on Waveform Drawing Number 1 is one complete cycle. During the (A) half of the cycle, pin W is positive in respect to the 12VCT line so current flows from 12VCT through the 78GUIC regulator and then back through D3 to the transformer. During the (B) half of the cycle, pin X is positive and current flows from 12VCT through the regulator, then through D4 back to the transformer.

Now we have DC voltage but as seen in Waveform Drawing Number 2 it is very wavy. This is called ripple. Excessive ripple may show up as a hum in the speaker, a wavy picture or the game may not operate at all.

This is where capacitors C29 and C5 are used to filter out the ripple. Since a capacitor can store an electron charge for a short period of time, we connect these capacitors from center-tap or logic ground to the positive DC voltage line. See Waveform Drawing Number 3. At point (A) the capacitors are charged. As the DC voltage tries to drop to point (B) the capacitors discharge and hold the line high. This is repeated for every cycle and the end result is nearly a straight line of DC voltage. As the drawing shows, the line is not perfectly straight because some ripple remains. As long as the ripple is less than .2 volts, the game should operate normally.

The reason for using a tantalum capacitor at C5 is because electrolytic capacitors act like inductors at high frequencies. Tantalum capacitors have a fairly constant reactance over the frequency spectrum and are better for filtering out noise or radio frequencies that may enter the line.

After the 12 VAC has been converted to DC voltage and filtered by C29 and C5,

the end result is approximately 16VDC at pin number 3 of the 78GUIC regulator. This 16VDC is also used to power the audio amplifier at location 11A. If this circuit is operating properly, pin number 2 of the regulator will read +6VDC.

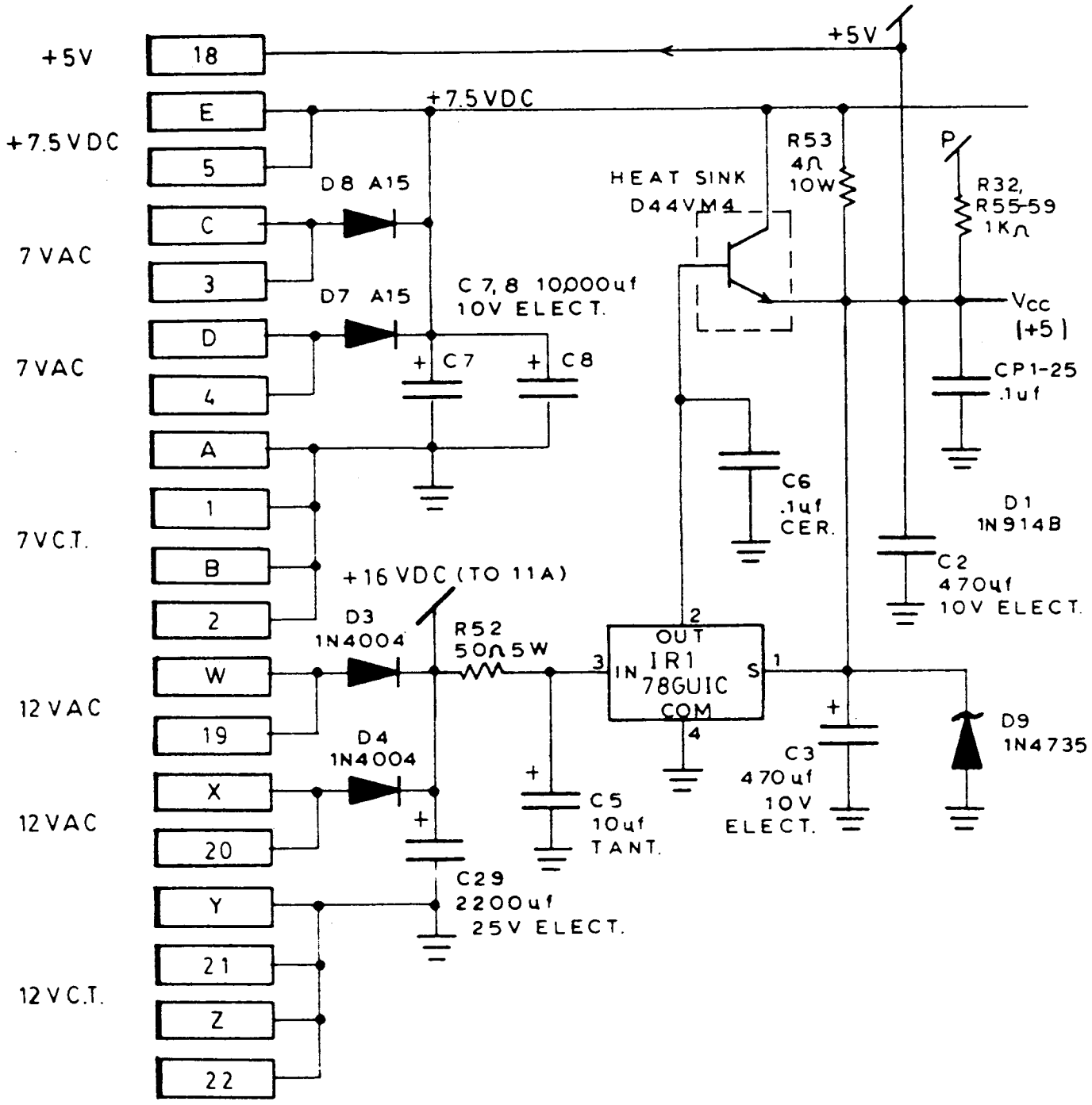
The 7VAC and 7VCT lines are converted to DC voltage by diodes D7 and D8 and filtered by capacitors C7 and C8 to end with +7.5VDC at pin E of the connector. This +7.5VDC is then fed to the collector pin of the D44VM4 pass transistor. A TIP31 transistor may be used as a substitute.

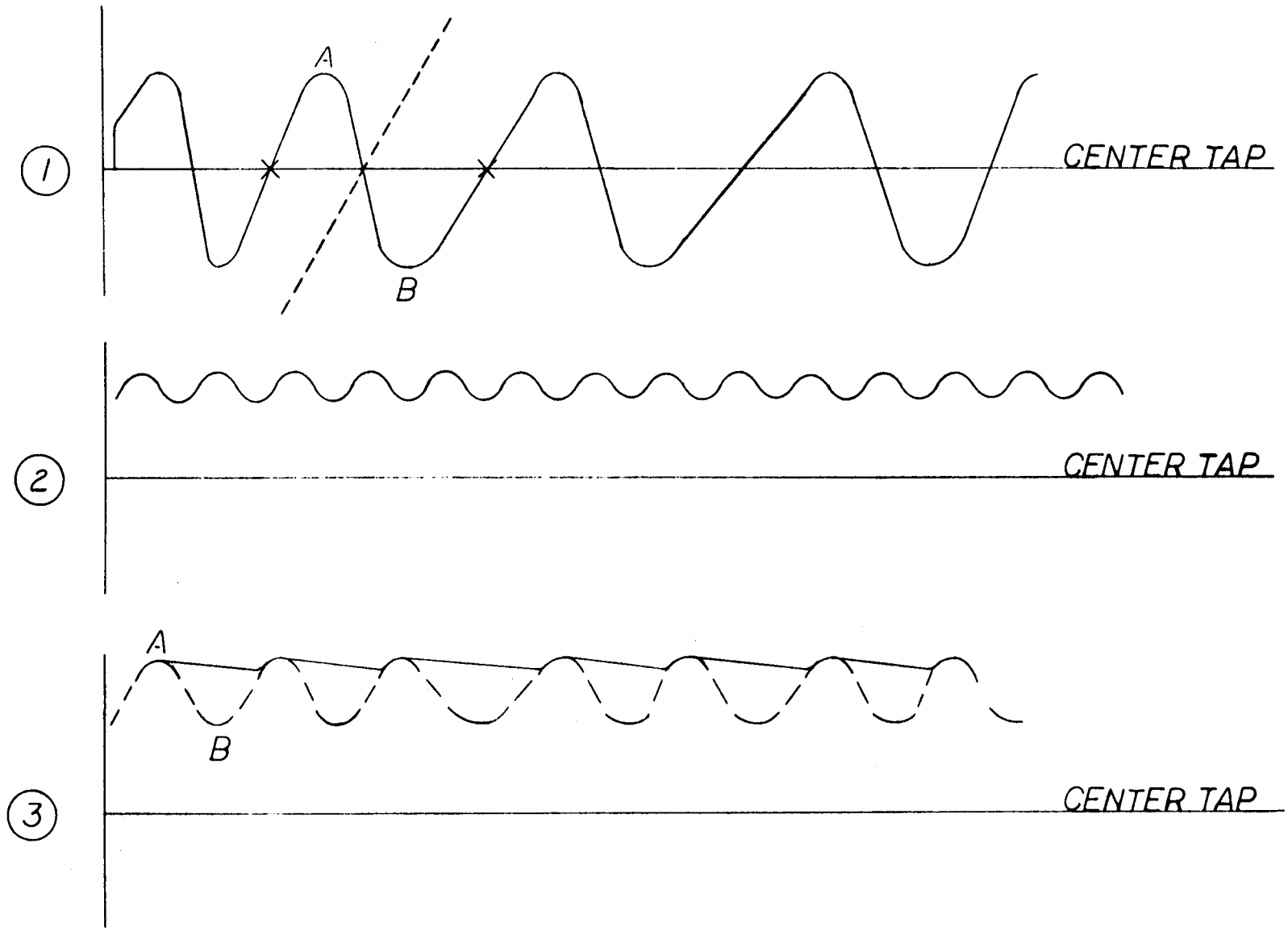
The +6VDC from pin number 2 of the regulator is fed to the base pin of the pass transistor to turn it on. If the circuit is working properly, the emitter pin of the transistor will present +5VDC to the rest of the logic board. You will see that although the 78GUIC regulates the +5VDC, the pass transistor supplies the current.

Zener diode D9 protects the logic circuitry. If for any reason the emitter of the pass transistor exceeds +5VDC, D9 will shunt the line to ground. This is an important feature because TTL logic circuitry can be damaged by voltages over +5.25VDC.

Occasionally a component in the logic circuitry will be defective in such a way that it pulls the +5VDC down to +3VDC or lower, even though the power supply circuit is functioning properly. The faulty logic component will usually be very hot, but not always. To isolate the +5VDC from the logic circuitry, remove the jumper wire next to R52 near the black heat sink.

POWER SUPPLY CIRCUITS





DIM. TOLERANCES UNLESS OTHERWISE SPEC.	FIRST USED ON			
CONCENTRICITY T.I.R. 002	DRN SBL	DATE 4-16-'82	SCALE NONE	MIDWAY MFG. CO. FRANKLIN PK., IL. 60131 A BALLY CO.
FRACTIONAL . . . . . ± .1/64	MECH CHK	MAT'L		WAVE FORM DRAWING
DECIMAL . . . . . ± .005	ELEC. CHK	FINISH		
HOLE DIA. . . . . +.002—.000				REVISIONS
ANGLE . . . . . ± 1/2°				PART NO. . . . – . . . . – . . . .
DO NOT SCALE DWG				

CONTROL INPUT CIRCUITS

Troubleshooting the control input circuits on the logic board is easy since all controls (coins, left, up, start, etc.) are handled the same way. For example, take the "move left" input. The left movement switch on the joy stick is normally open with one terminal connected to common or logic ground. The other terminal is connected to pin M on the logic board edge connector.

If the circuit is working properly, pin M will measure +5 volts and will drop to 0 volts when the left movement switch is closed. If pin M remains at +5 volts when the left movement switch is closed, the problem is either the switch or a loose connection because the signal is not reaching the logic board. If pin M measures correctly but the PAC-MAN won't move left or if pin M is stuck low (0 volts) the problem is on the logic board.

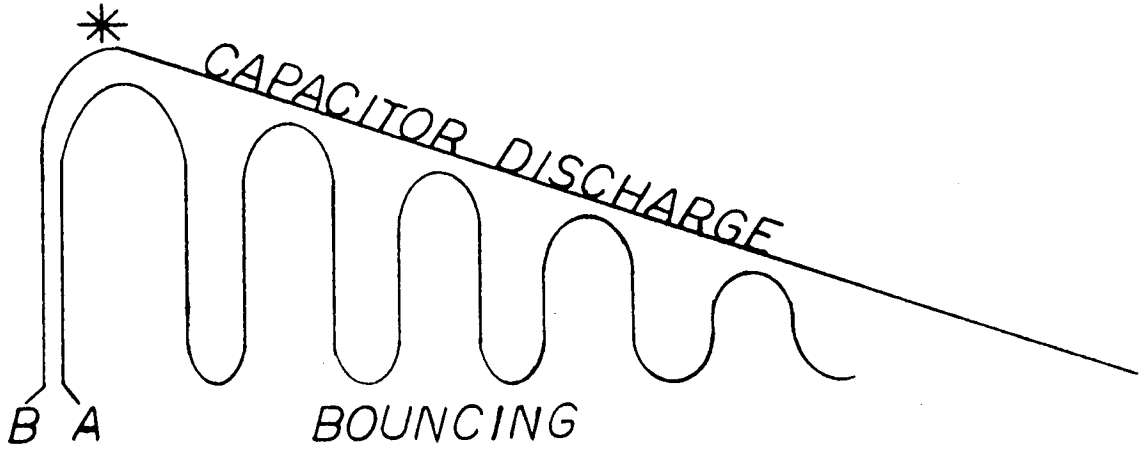
Once we are sure that the logic board is at fault, it may be easier to work backwards.

If resistor R47 was broken or burnt the signal at pin M would not reach pin number 4 of the buffer at location 8E, so you may prefer to start at the buffer. There are two components in this circuit that might hold the signal low. Capacitor C22 could be shorted allowing ground to pass through to the line or the buffer could be bad. It is easier to remove C22 first, then if the problem remains, change the buffer.

The RRC network comprised of RM8, R47 and C22 conditions the signal. RM8 pulls the line up so that it reads +5 volts when the move left switch is open. R47 limits the current into the circuit. C22 debounces the signal.

When a mechanical switch is first closed, it bounces a few times before coming to rest in the closed position. In movement circuits this may not matter but for coin circuits to yield half a dozen bounces for one quarter could cause a problem.

(4)



24

THIS DWG. IS CONFIDENTIAL & PROPERTY OF MIDWAY MFG. CO.

DIM. TOLERANCES UNLESS OTHERWISE SPEC. CONCENTRICITY T.I.R. . . . .002 FRACTIONAL . . . . . ±.1/64 DECIMAL . . . . . ±.005 HOLE DIA. . . . . +.002—.000 ANGLE . . . . . ±1/2° **DO NOT SCALE DWG**	FIRST USED ON		
	DRN SBL	DATE 4-16-'82	SCALE NONE
	MECH CHK	MAT'L.	
	ELEC. CHK.	FINISH	

MIDWAY MFG. CO.
FRANKLIN PK., IL. 60131 A BALLY CO.

WAVE FORM DRAWING

REVISIONS

PART NO. . . . – . . . . – . . .

To eliminate this bouncing we use a capacitor connected between the line and ground. See Waveform Drawing Number 4. The waveform drawing shows two signals. (A) is the switch bouncing. (B) is the capacitor discharging. When the move left switch is closed, the capacitor discharges. You will see the value of the capacitor is chosen so that it finishes discharging after the bouncing has stopped. The circuit will see only a single smooth pulse.

Pin R on the logic board edge connector is only used in table models. When it is connected to ground it causes the image on the screen to flip for the second player. Also movement controls on pins V, 13, P and 12 are only used in table models. Although the schematic shows two circuits for COIN only pin J is used because the coin switches are connected in parallel.

Besides a bad capacitor or buffer causing loss of a control, resistor packs RM7 and RM8 can cause unusual problems. Each pack contains 8 resistors and it is possible that two resistors in a pack will "cross talk".

In one example, the game would add a free credit every time the joystick was moved to the right. It turned out that when pin 11 of the edge connector was low, the pull up resistor in RM8 would cross-talk or leak to the pull up resistor for the COIN 1 circuit. This would force pin number 12 of the buffer 8E low and the game would add a credit.

In another example, pressing the player 1 button would throw the game into test, so RM7 was changed.

Studying the option switches at location 9D, you will find that switches 1 thru 7 are handled like control inputs. The current limit resistors and debounce capacitors are absent because the switches will not see continuous duty and bouncing only occurs after a switch is first closed.

Dip switches 1 and 2 are for price setting, 5 and 6 for setting the number of points required to earn the bonus PAC-MEN and switches 3 and 4 determine the number of PAC-MEN that starts the game.

The two sets of pads can be shorted with wire and soldered to connect pins 10 and 14 of buffer 8D low. When the halves of pad A are shorted, the character nicknames become AAAA, BBBB, CCCC and DDDD. When pad B is shorted, the game becomes slightly more difficult to play. There are other sets of pads on the board but only pad B is useful.

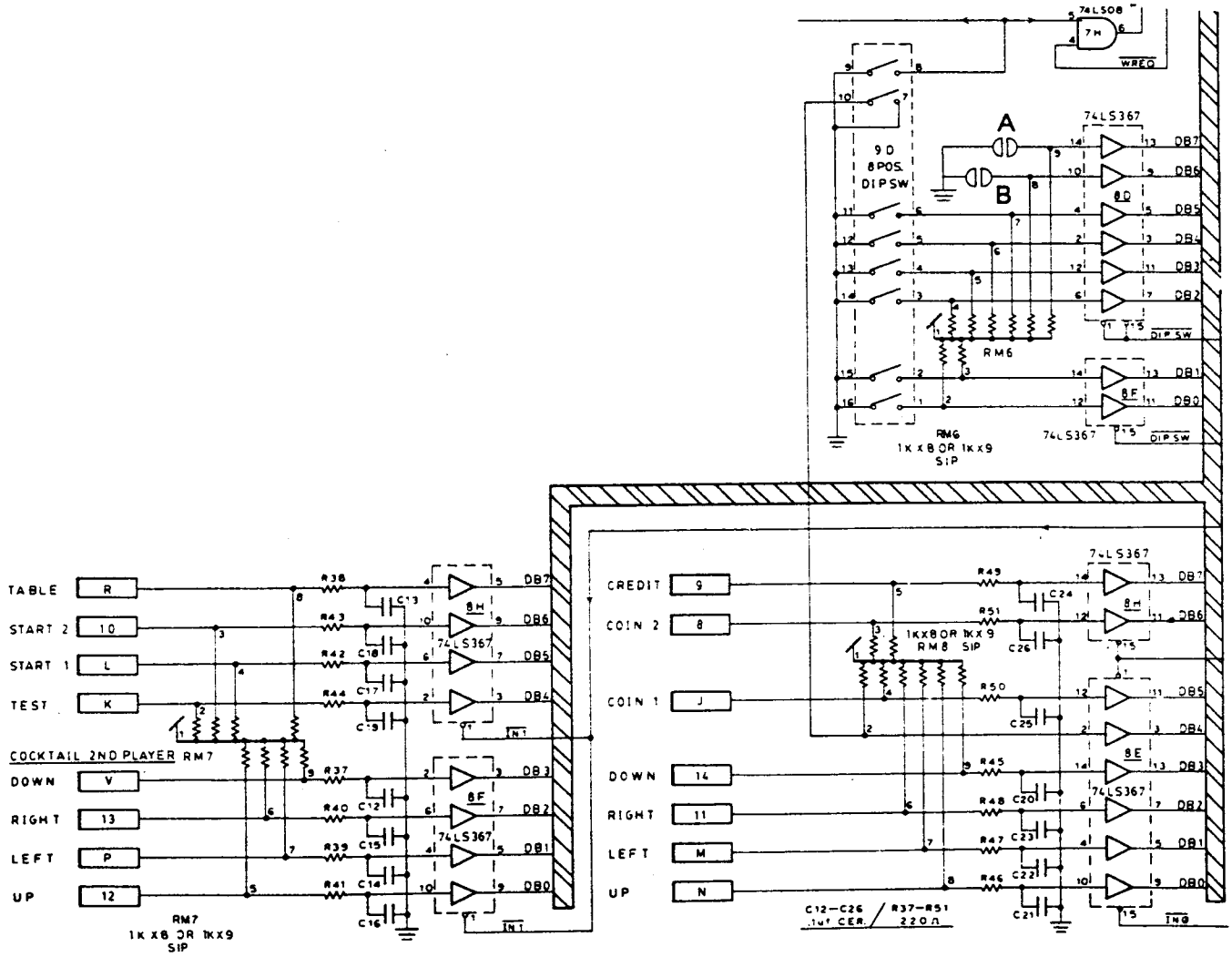
Switches 7 and 8 are used as diagnostic aids. When switch 8 is closed (or on) the game will freeze the action. The image on the screen will freeze and even a note in the middle of a tune will be held. This freeze option has proved valuable in troubleshooting the video circuits.

When switch 7 is on, the game will exhibit a rack test. First, the starting maze and cherries will appear. The cherries will shift to the bottom right corner of the screen. Then the second maze and the strawberry will appear. Within seconds the strawberry will shift to the bottom of the screen. Third, the intermission cartoon will break the tension. Then on to the 4th, 5th, 6th, etc. mazes and cartoons until 7 keys appear on screen. Anytime during this rack test one can turn switch 7 off and begin game play at that moment and maze.

Often a symptom occurs only after a certain maze. For instance, maybe after the 5th maze dots appear around the apple. even if one were skilled enough to play to the apple, one would have only seconds left to diagnose the circuit before being eaten, "with a joystick in one hand and a logic probe in the other".

Instead, one can simply rack test to the 5th maze, then turn switch 7 off. Game play would start immediately. As the symptom (dots around apple) appears, turn switch 8 on and the image will freeze.

CONTROL INPUT CIRCUITS



NOTES

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SYSTEM TIMING

System timing and clocking for the Z80 CPU starts with the crystal oscillator circuit. An 18.432 MHz (megahertz or millions of cycles per second) crystal at location 7B is used to set the oscillator frequency. The crystal is a slice of quartz which has been cut to precise dimensions so that it tends to oscillate at a certain frequency. Guitar and piano strings are designed with specific dimensions which depend on what frequency or note they are to generate. So is a tuning fork and xylophone. Two 330 ohm resistors, a 100pf. capacitor and three inverting buffers at 8B complete the oscillator circuit.

The signal from the oscillator circuit is used to clock the flip-flops at location 8A. Output pine 3 and 6 of 8A are inverted by two more buffers in 8B to yield the 6 MHz and 6M* signals. The inverse of the 6M* signal ($\overline{6M*}$) is available at pin number 11 of the XOR gate in location 4F.

6 MHz is connected to pin 3 of a flip-flop at 8C and also to the clock inputs of binary counters 3R and 3S. 8C divides the 6 MHz in half and outputs a 3 MHz signal from pin number 5. This 3 MHz is referred to as the 1H signal. The 1H signal is inverted by the last buffer in chip 8B and then used to clock pin 6 of the Z80 CPU.

The binary counter at 3R counts the 6 MHz signal and divides it in half four times. This way the 2H signal is half the frequency of 1H, 4H is half the frequency of 2H, 8H is half the frequency of 4H...etc. The 1H through $\overline{256H}$ (horizontal timing) signals are used to generate the HSYNC, HBLANK and $\overline{HBLANK}$ signals. Flip-flop 5M halves the frequency of HSYNC to provide the 1V signal and counters 2R and 2S provide 2V through 128V. $\overline{VSYNC}$ (vertical sync) from pin 11 of counter 2S is used to produce the $\overline{CMPSYNC}$ (composite sync) signal for the monitor.

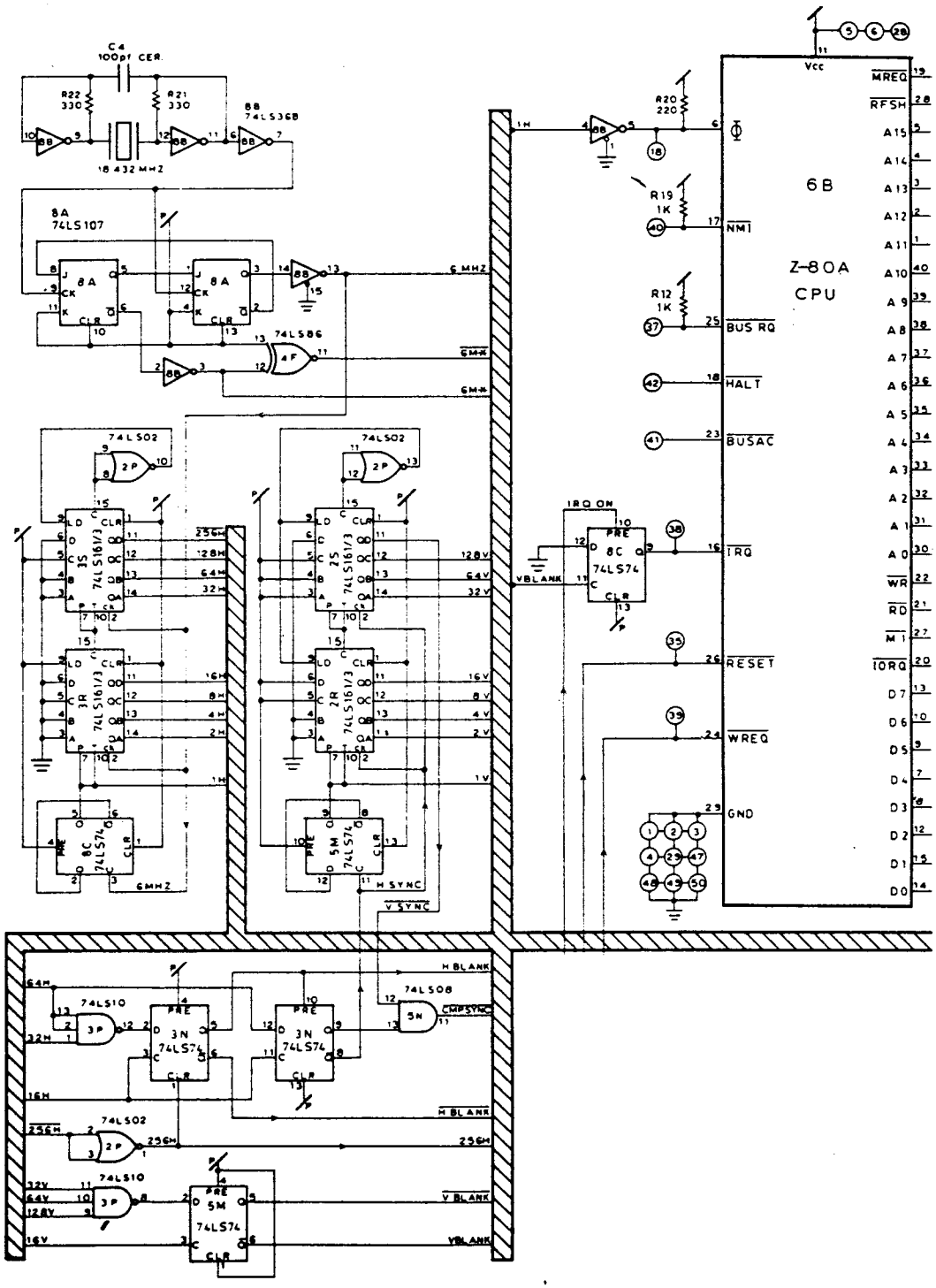
Usually the game will not be operative if any of the H or V signals are missing. Without the signal from pin 7 of 8B in the crystal oscillator circuit the game will be completely dead (no video, no sound and no pulsing or activity anywhere on the logic board).

An easy way to check the H and V signals is to use a video probe on the outputs (pins 11, 12, 13 and 14) of counters 2R, 2S, 3R and 3S. A video probe is simply a wire with a 470 ohm resistor connected to one end. By connecting the wire to either the red, green or blue color outputs to the monitor any signal probed by the resistor end will cause a change in color or pattern on the monitor screen. Assemble a video probe to check the H and V signals.

When using a video probe on the $\overline{256H}$ signal the monitor screen will turn light blue. The maze and characters will still be visible but it will appear as if a blue filter were placed over the screen. The 128H signal will split the screen in half horizontally so that one half is light blue while the other half is normal. 64H will cause two blue bars on the screen. 32H will cause four bars. Each H signal after 32H will double the number of bars on the screen. Using the video probe on the V signals will cause vertical bars.

The video probe can also be used as a logic probe. When the resistor end is connected to a high signal the monitor screen will turn light blue (red or green can be used also). When it is probing a low signal the screen will be normal. This can be useful in troubleshooting the control input circuits.

SYSTEM TIMING CIRCUITS



NOTES

This space is provided for personal notes

THE WATCHDOG CIRCUIT

The "watchdog" circuit was designed to reset the microprocessor if it detects an error in system timing or on the address and data buses. In older games without watchdog circuits static discharge, noise or vibration would introduce false information into the system which sometimes caused the game to lock-up until it was manually reset. In later games the watchdog will detect the false information or lock-up condition and will deliver an automatic reset pulse to the microprocessor. This automatic reset pulse will normally occur within seconds after the error has been detected, thereby minimizing the games down time.

The 74LS161 binary counter at location 9C will be cleared before it counts to 15. This way the signal on pin 15 remains low and the signal on pin 13 of NOR gate 7L remains high. Pin 26 of the Z80A microprocessor must be high for the system to operate.

If an error is detected in the system, 9C will not be cleared before reaching the critical count of 15. This will cause a high going pulse on pin 15. NOR gate 7L will invert the high going pulse and deliver a low going pulse to pin 26 of the microprocessor to reset the system.

Occasionally there will be a problem in the system timing or 9C will be faulty and the game will continually reset. Every second or two the game will run through the power up or self-test sequence and the signal on pin 26 of the microprocessor will be pulsing. To determine if the problem is caused by a faulty watchdog circuit, try the self-test. If the resetting stops and the test reads "Memory OK" the problem is probably the watchdog.

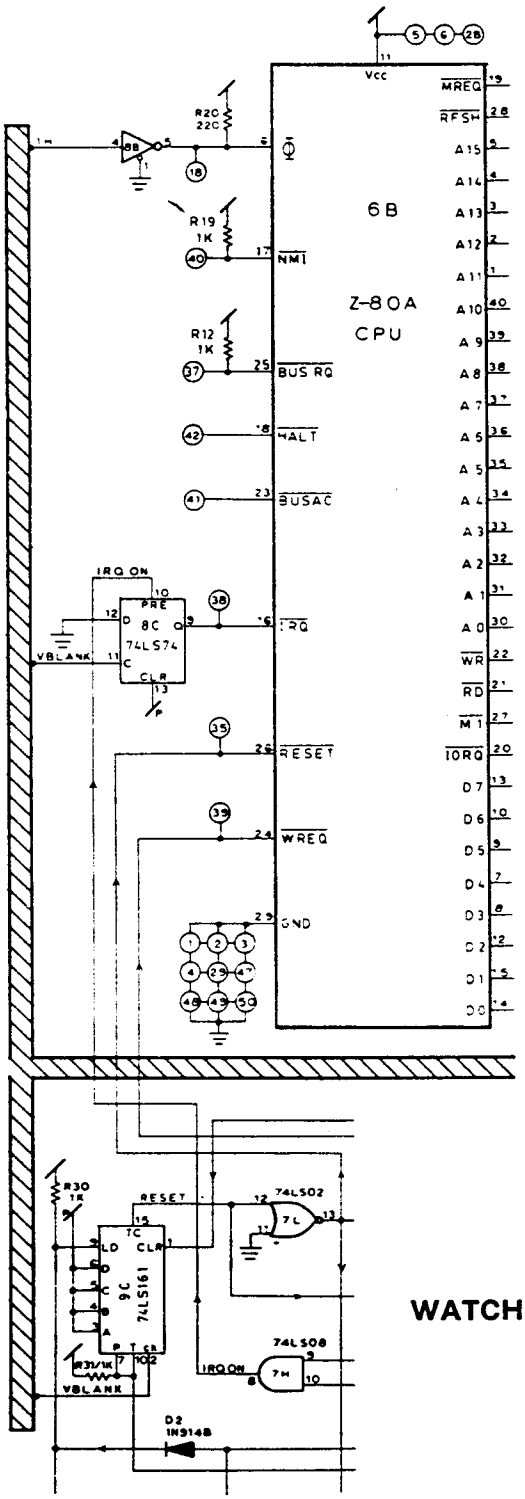
If the VBLANK signal is incorrect the watchdog will "bark" (pulse on pin 15 of 9C). Since the VBLANK signal is derived from the 16V through 128V signals, if it is incorrect, one may have to trace back to counters 2R, 2S, 3R and 3S to find the fault.

If the decoder at location 7J is faulty, the WDR (watchdog reset) signal on pin 12 will not clear counter 9C in time and the watchdog will bark. Also if the signals into 7J are incorrect the WDR signal will fail to clear 9C. It is through 7J that the watchdog detects an error on the address bus.

To determine if counter 9C is causing the problem, cut pin 2. The game should

then operate normally. If the game does not operate normally after cutting pin 2 of 9C the problem is elsewhere in the system.

Remember the tilt switch on the coin door and the red switch next to location 11A are also in the reset circuit and may cause problems similiar to a faulty watchdog.



WATCHDOG CIRCUIT

THE PROGRAM ROMS

The personality (software or program) of the game is stored in the program ROMS. Each ROM holds 4,096 words (8 bits per word) of the program. The schematic shows eight ROMS but only locations 6E, 6F, 6H and 6J are used. Either a ROM or an EPROM (erasable and programable ROM) can be used at these four locations.

Each ROM may be called upon hundreds or thousands of times a second to read out its programming to the data bus. When the CE (chip enable) input on pin 20 is low the ROM is enabled. When the ROM is enabled the 8 bit word at the location called for by the address bus will appear on the ROM outputs. The schematic shows pin 18 as a CE input but on the types of ROMS and EPROMS being used pin 18 is address A11.

The address and data buses are paralleled to the ROMS. Because these ROMS are tri-state components they can share the eight data lines. If they were not tri-state components four ROMS (with eight data outputs each) would require 32 data lines.

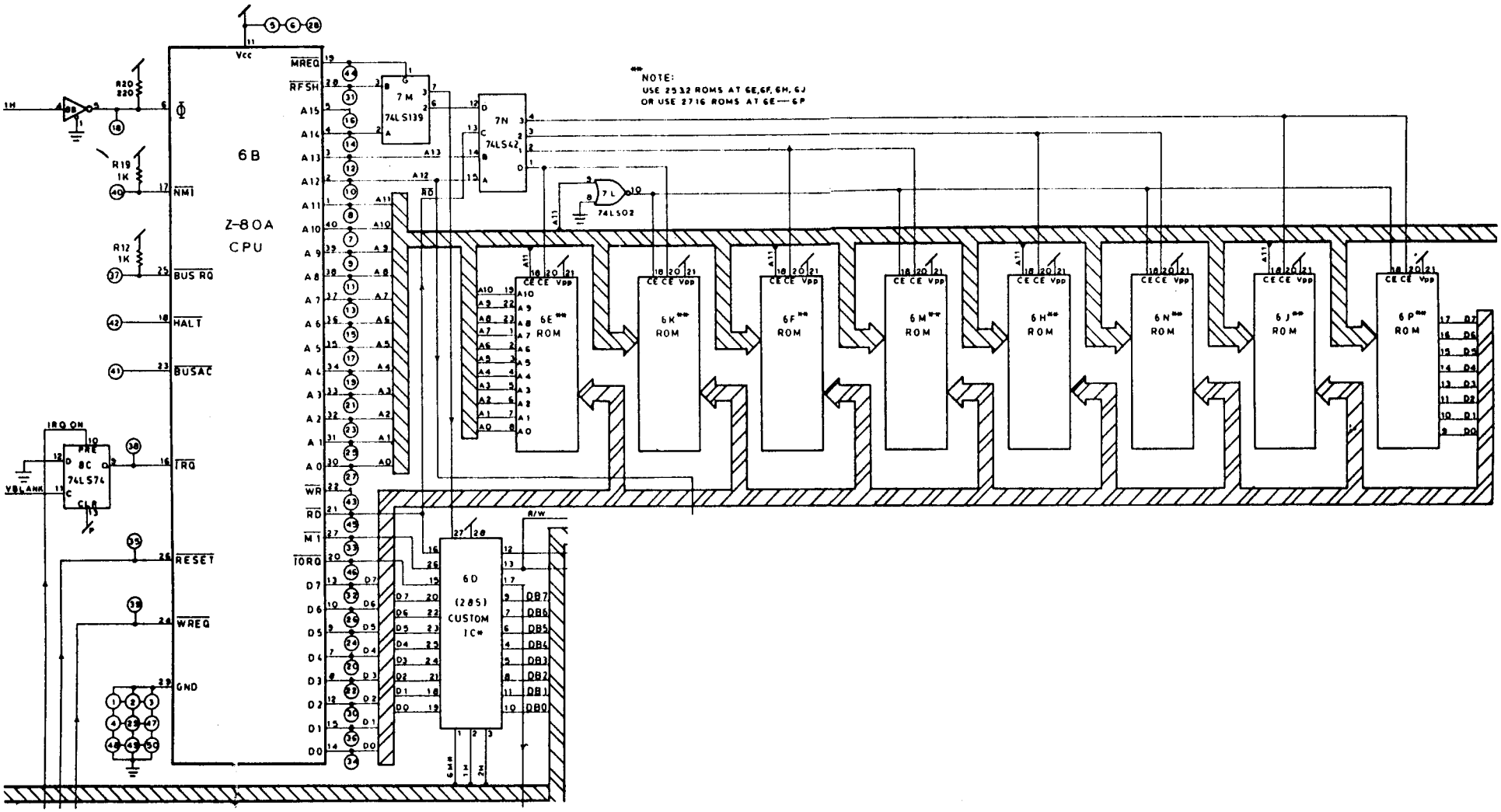
When a tri-state component is in the tri-state mode its outputs are disabled and will not drive a line high or low. When a component is in the tri-state mode its outputs respond as if it were completely removed from the circuit. With this tri-state feature many components can share the same output lines and as long as only one component is enabled at any time that component will control the lines. If two or more components are enabled at the same time the lines they share will not be driven properly and the components may be damaged. For example, if two program ROMS are enabled at the same time one might try to drive the D0 line low while the other tries to drive the D0 line high. The outcome would be a faulty D0 line. This tri-state feature is used elsewhere on the logic board. See the logic board schematic. The control input buffers at 8D, 8E, 8F and 8H are tri-state components. When pins number 1 and 15 are low data on the buffer inputs will appear on the outputs. When pins 1 and 15 are high the buffer outputs are disabled. This allows the four buffers to share the eight DB (buffered data) lines. The component at 5S and the buffers at 6R and 6S are also tri-state devices.

The component at location 7N is used to control the tri-state mode of the program ROMS. 7N is a 74LS42 BCD to decimal decoder. BCD means binary coded decimal. With the decimal system we count 0, 1, 2, 3, 4, 5...etc. Because the binary system in digital electronics only uses the symbols 1 and 0 we must use a code to indicate all other numbers. In binary the number 5 is written 0101. The first bit on the right represents a 1. The next bit represents a 2. The third bit represents a 4 and each bit to the left represents twice the number of the preceeding bit. The fourth bit from the right represents an 8. In the word 0101 the first bit is a 1 (or high) so we have a 1. The second bit is 0 (or low) so we do not have a 2. The third bit from the right is high so we do have a 4 and the last bit is low so we do not have an 8. Now add the numbers we do have. The first bit represents a 1 and the third bit represents a 4. 4 plus 1 equals 5. With the binary system we count 0000, 0001, 0010, 0011, 0100, 0101...etc.

The BCD to decimal decoder at 7N has ten outputs representing 0 through 9 in decimal. Pins number 12, 13, 14 and 15 are inputs for a 4 bit binary number. Pin 15 is the A input (or least significant bit) and represents a 1. Pin 12 is the D input (or most significant bit) and represents an 8. All ten decimal outputs are normally high. When a binary number is written into the inputs 7N decodes the 4 bits into decimal and the corresponding pin for that decimal number goes low. For example, if the binary number 0011 is on the inputs of 7N the output pin number 4 will go low because it represents the decimal number 3. When pin 4 goes low the program ROM at 6J will be enabled. Because only one output on 7N can be low at any time pins 1, 2 and 3 will be high and ROMS 6E, 6F and 6H will be in the tri-state mode. If the binary number 0001 was on the inputs pin 2 would go low because it represents the decimal number 1 and ROM 6F would be enabled while 6E, 6H and 6J would be in tri-state.

We can see that this circuit allows four tristate ROMS to share the data bus and that chip 7N controls the tri-state mode of the program ROMS.

PROGRAM ROMS

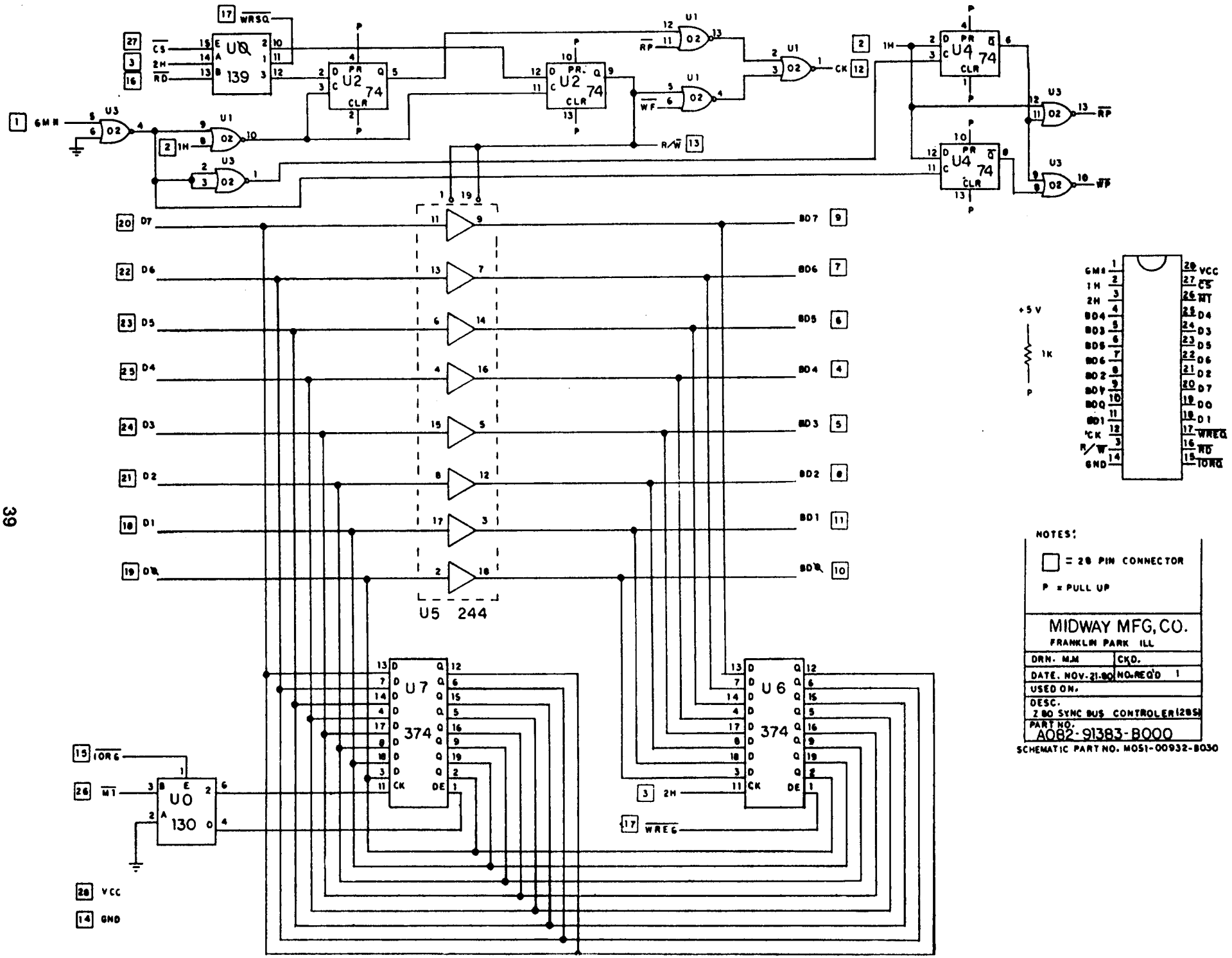


THE Z80 SYNC BUS CONTROLLER

The component at location 6D will be either an NVC285 custom integrated circuit or a small printed circuit board with TTL chips. This is the Z80 SYNC bus controller. Its purpose is to control the passage of data between the CPU data bus and the DB (buffered data) bus. Information can pass through component 6D from the CPU data bus to the DB bus or from the DB bus to the CPU. When a component can pass data in either direction it is called bidirectional. To see how this is accomplished look at the Z80 SYNC BUS CONTROLLER schematic. The numbers in square boxes represent the pins on the small printed circuit board or on the NVC285.

The eight CPU data lines on pins 18 through 25 are fed to the inputs of the tri-state buffers at location U5. The R/W (read/write) signal at pins 1 and 19 of U5 controls the buffer outputs. When the R/W signal is low data will pass from the CPU data bus to the DB bus. When the R/W signal is high the buffer outputs are disabled and pins 4 through 11 can be used as inputs from the DB bus. When the CPU requires data from the DB bus the WREQ (write request) signal goes low to enable the latches at location U6. When U6 is enabled and signals on the D inputs will pass to its Q outputs and the CPU data bus at pins 18 through 25. The direction that data passes through the Z80 SYNC BUS CONTROLLER depends on which component, U5 or U6, is enabled. The latches at U7 are used to store an 8 bit word from the CPU date bus or the DB bus until that word is needed on either bus.

Note that the R/W signal is derived from the component at 6D and the CK signal leaving pin 12 of 6D is gated through chip 7L to control the tri-state component at 4H in the "scratchpad circuit".


U0 139
U2 74
U4 74
U3 02
U1 02
U5 244
U7 374
U6 374
U0 130
WRSQ
CS
2H
RD
1H
6MH
RP
WF
R/W
CK
WREQ
IORQ
MT
VCC
GND
D7
D6
D5
D4
D3
D2
D1
D0
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
+5V
1K
NOTES:
= 28 PIN CONNECTOR
P = PULL UP
MIDWAY MFG, CO.
FRANKLIN PARK ILL
DRN. M.M
CK'D.
DATE. NOV-21-80
NO. REQ'D 1
USED ON.
DESC.
Z 80 SYNC BUS CONTROLER (28S)
PART NO.
A082-91383-B000
SCHEMATIC PART NO. MO51-00932-B030

THE SCRATCHPAD AND V RAM ADDRESSER

The 2114 RAMS in the number 4 row are used as "scratchpad" memory. Temporary data such as the number of credits or the high score is stored in scratchpad. These RAMS also store the first player's frame while the second player has control and vice versa. CPU commands and character positions can be held in the scratchpad.

Beacuse the scratchpad RAMS store information that can affect the video image as well as the program routine their addressing and outputs must be synchronized with system timing and the monitor scanning rates. The CPU address bus is buffered through chips 6R and 6S to the AB (buffered address) bus. The vertical and horizontal timing signals are processed through chip 5S to the AB bus. When the 2H signal is low the outputs of 5S will be tri-state and the buffers will control the AB bus. When the 2H signal is high the buffers will be in tri-state and 5S will pass the vertical and horizontal timing signals to the AB bus.

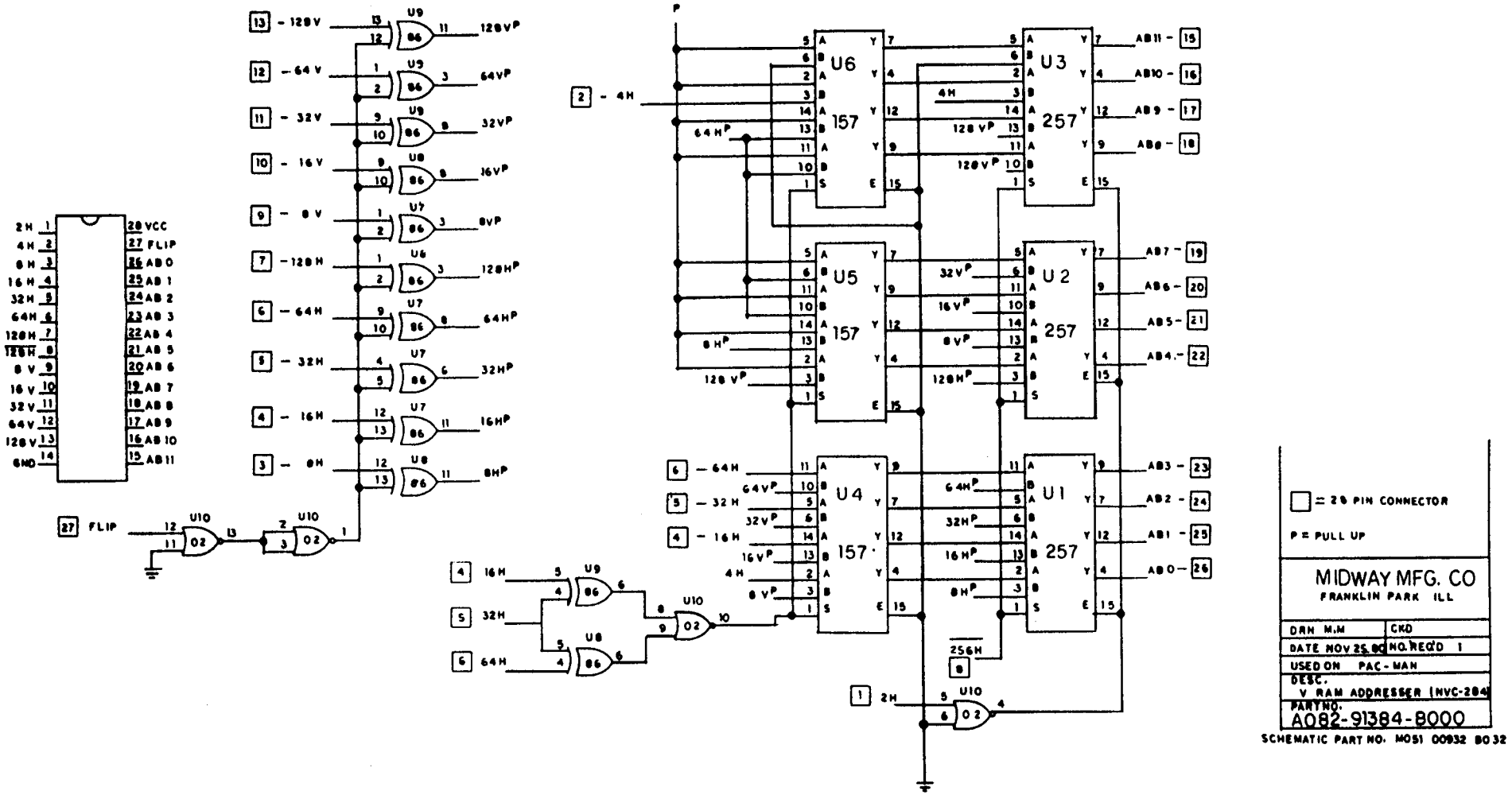
The component at location 5S will be either an NVC284 custom integrated circuit or a small printed circuit board with TTL chips. This is the V RAM ADDRESSER.

The horizontal timing signals on pins 3 through 7 and the vertical timing signals on pins 9 through 13 are Xored by the chips at U7, U8 and U9. The output of an XOR gate will be low whenever its inputs are both high or both low. Note that one of the inputs on each of these XOR gates is connected to pin number 1 of U10. When the FLIP signal is low the XOR gates will pass the vertical and horizontal timing signals. When the FLIP signal is high the outputs of the XOR gates will be the inverse (opposite) of the vertical and horizontal timing signals. Another way to look at this circuit is to consider the XOR outputs as a ten bit address bus. When the FLIP signal is low the highest address would be 1111111111, the second highest address 1111111110 and the third highest 1111111101, etc. When the FLIP signal is high these addresses will become 0000000000, 0000000001 and 0000000010 respectively. This is how the image on the monitor screen is flipped upside down for the table model games. The FLIP signal goes high for the second player in a table model game and the video circuits and scratchpad RAMS are addressed backwards.

From the outputs of the XOR gates the H^P and V^P signals are fed to the multiplexers at U1 through U6. The SELECT signal on pin number 1 of U4 through U6 determines whether word-A or word-B will appear on the Y outputs. The 256H signal is used as the SELECT line for multiplexers U1, U2 and U3. The 74LS257 chips at U1 through U3 are tri-state devices. When pin 15 on these three chips is high the Y outputs will be in the tri-state mode. When pin 15 is low either word-A or word-B will appear on the outputs. The 2H signal is inverted by an OR gate in U10 to provide the tri-state enable to pin 15 on U1, U2 and U3.

From this one can see that the V RAM ADDRESSER is used to flip the image on the monitor screen in the table model games and to synchronize the scratchpad with system timing. The vertical and horizontal timing signals used by the V RAM ADDRESSER also provide the CMP SYNC (composite sync) signal for the monitor.

The outputs of the 2114 RAMS are pushed through the component at 4H to the buffered data bus. 4H is bi-directional and so are pins 11, 12, 13 and 14 on the scratchpad RAMS. When the R/W (read/write) signal is low data passes through 4H into the RAMS. When the R/W signal is high data leaves the RAMS and passes through 4H to the buffered data bus. 4H is also a tri-state device. The V RAM signal controls the tri-state mode on 4H.



□ = 28 PIN CONNECTOR

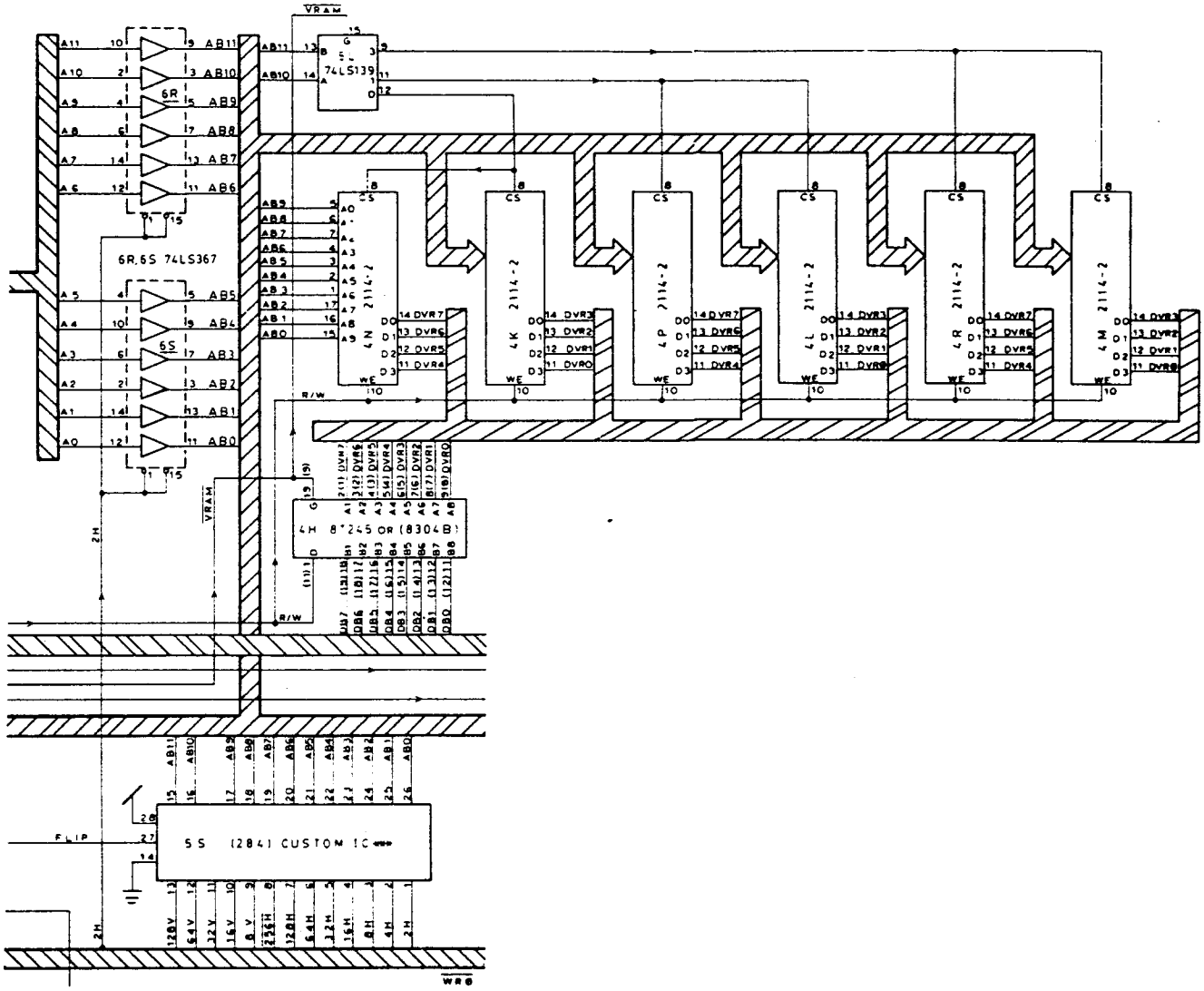
P = PULL UP

MIDWAY MFG. CO
FRANKLIN PARK ILL

DRN M.M	CKD
DATE NOV 25, 80	NO. REQ'D 1
USED ON PAC-MAN	
DESC. V RAM ADDRESSER (NVC-284)	
PART NO. A082-91384-B000	

SCHEMATIC PART NO. MOS1 00932 B032

SCRATCHPAD AND V RAM ADDRESSER



CHARACTER ROM CIRCUITS

Character ROMS 5E and 5F generate the images on the screen. ROM 5E generates the maze and dots. ROM 5F and the "attack" RAMS generate the Pac-Man and ghosts.

One can simulate a problem in the character ROM circuit by bending a pin on either ROM so that the pin is out of the socket. This might cause missing portions of video, broken images or objects in the wrong places on screen. When ROM 5F is completely out of the socket the Pac-Man and ghosts will be square blocks. The game will play without ROM 5F but instead of characters with eyes and features, colored square blocks will run through the maze.

A problem in the attack RAM circuit might cause the characters to change color or eyes and other features may distort. A bad attack RAM can also cause dots and lines to appear where they should not.

To start at the beginning note the buffered address and buffered data signals at RAMS 3F and 3H. A problem in this area can cause the characters to appear in the wrong place on the screen or they might pass through the blue lines of the maze. In one case the WE signal to RAM 3F was missing. This caused the characters to be stuck in the upper left hand corner of the screen.

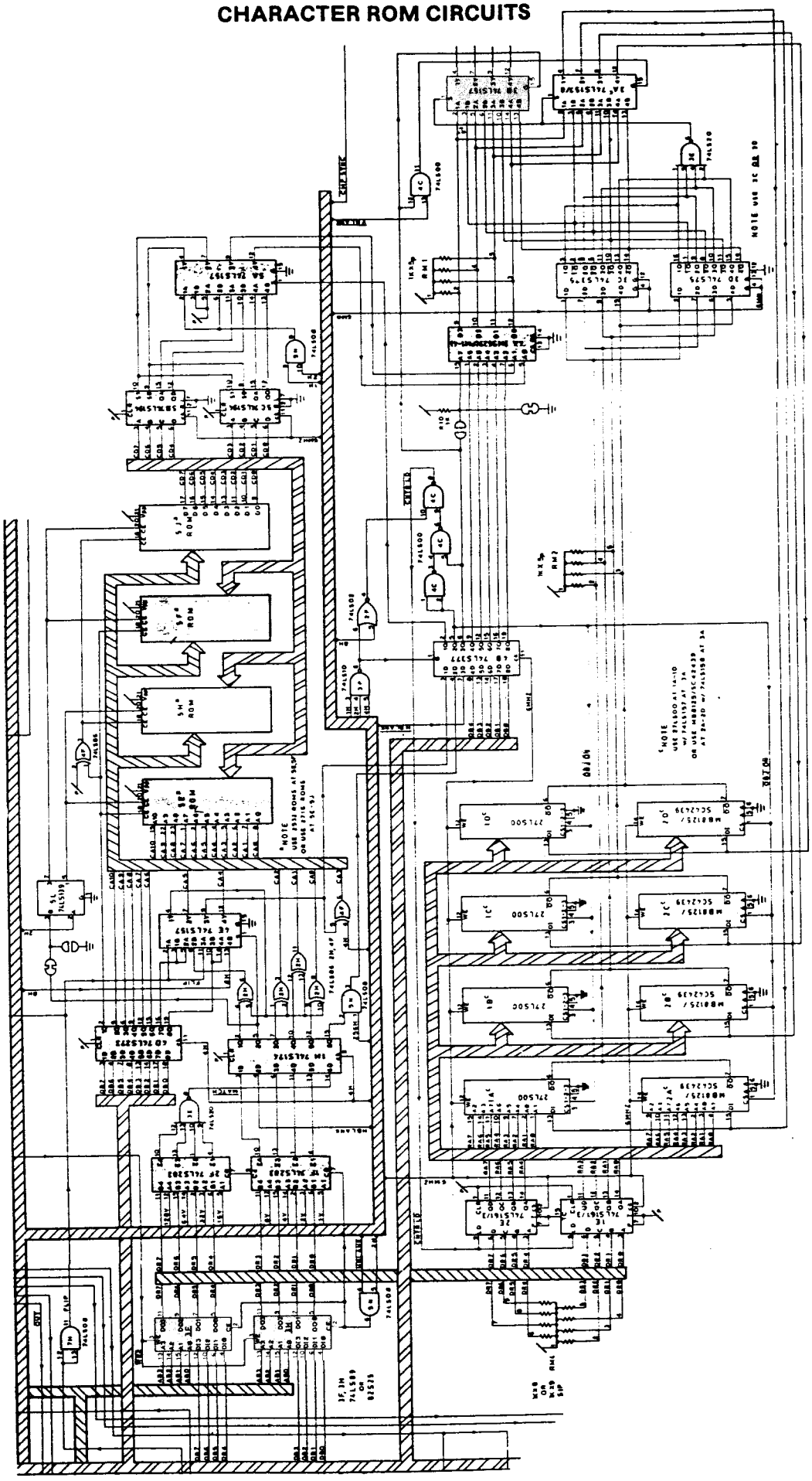
The DR0 through DR7 signals from RAMS 3F and 3H are used in addressing both the character ROMS and the attack RAMS. Signals DR0 through DR7 supply word-B to the full adders at 1F and 2F. Vertical blanking signals 1V through 128V supply word-A. The sum or outputs of 2F are NANDED by 3E to pin number 14 of the flip-flop at 1H. The sum of adder 1F and the HBLANK (horizontal blanking) signal supply the remaining inputs of flip-flop 1H.

The outputs of chip 1H are Xored by chip 2H to provide character addresses CA0, CA1 and CA2. CA3, CA4 and CA5 require the 4H, 8H, flip and DB0 signals at 4F and 4E chips. The buffered data bus is pushed through the flip-flops at 4D to supply addresses CA6 through CA10 to the character ROMS. The CE signal for the character ROMS is derived from the 2H and HBLANK signals decoded by chip 5L.

Character data CD0 through CD7 from the character ROMS feeds the parallel load inputs of the shift registers at 5B and 5C. From the outputs of the shift registers (pins 12 and 15) the character data passes through the multiplexer at 5A to become addresses A0 and A1 for PROM PM1-4 at location 4A. Buffered data passes through the flip-flops at 4B to provide addresses A2 through A6. Note that address input A7 of PROM PM1-4 is held low permanently.

Data from PROM PM1-4 is multiplexed through chips 3A and 3B. At 3B this data becomes signals COL0 through COL3 which address the "color" PROM at location 7F. Through 3A it becomes input data for the attack RAMS.

CHARACTER ROM CIRCUITS



ATTACK RAM CIRCUITS

Addressing for the attack RAMS starts with the DR0 through DR7 signals from RAMS 3F and 3H. First, the DR signals are parallel loaded into counters 1E and 2E. When the CNTR LD (counter load) signal goes low the DR signals will appear on the counter outputs as RA0 through RA7.

If there is a problem with the RA (ram address) signals the Pac-Man and ghosts might be split into sections either vertically or horizontally. The characters might also appear in the wrong places on the screen. All of the RA lines should be pulsing. If one finds an RA line stuck low or high the counter or DR signal associated with that line is probably faulty. To determine which RA line carries the problem, use a jumper wire connected to common or logic ground to force each RA line low one at a time. IMPORTANT: If a pulsing output is forced low for too long the component might be damaged. It is recommended that one force the RA lines low for no more than 5 or 10 seconds at a time. When an RA line is forced low the characters will split or move to another position on the screen. An RA line that does not cause a change in the characters when it is forced low is bad. Remember that a bad attack RAM might hold an RA signal low.

The CNTR LD signal on pin 9 of counters 1E and 2E comes from pin 8 of the NAND gate at 4C. Note the three sections of NAND gates at 4C. The first section (pins 1, 2 and 3) inverts the signal from pin number 5 of flip-flop 4B. The second section nands the result of the first section with the signal from pin 6 of 4B. The third section (pins 8, 9, and 10) nands the output of the second section with the result of the 1H, 2H, 4H and 8H signals from gates 2P and 3P. Note also that pin 6 of the NAND gate at 3P is strobing flip-flop 4B and the H BLANK signal is connected to pin number 7 of 4B. The signal on pin 4 of flip-flop 4B is the result of the 256H and MATCH signals at NAND gate 5N. As one can see a faulty signal anywhere in these circuits will cause an incorrect CNTR LD signal and distortion of the moving characters.

The 6 MHz signal is used to clock the counters at 1E and 2E and it also provided WE (write enable) for the attack RAMS. Although the schematic shows eight attack RAMS only locations 2A, 2B, 2C and 2D are used. Acceptable substitutes for the attack

RAMS are numbers 93415, MB8125 and SC42439. Note that the OBJ ON (object on) signal at pin number 1 of the attack RAMS is coming from flip-flop 4B where it was also used in the CNTR LD circuit.

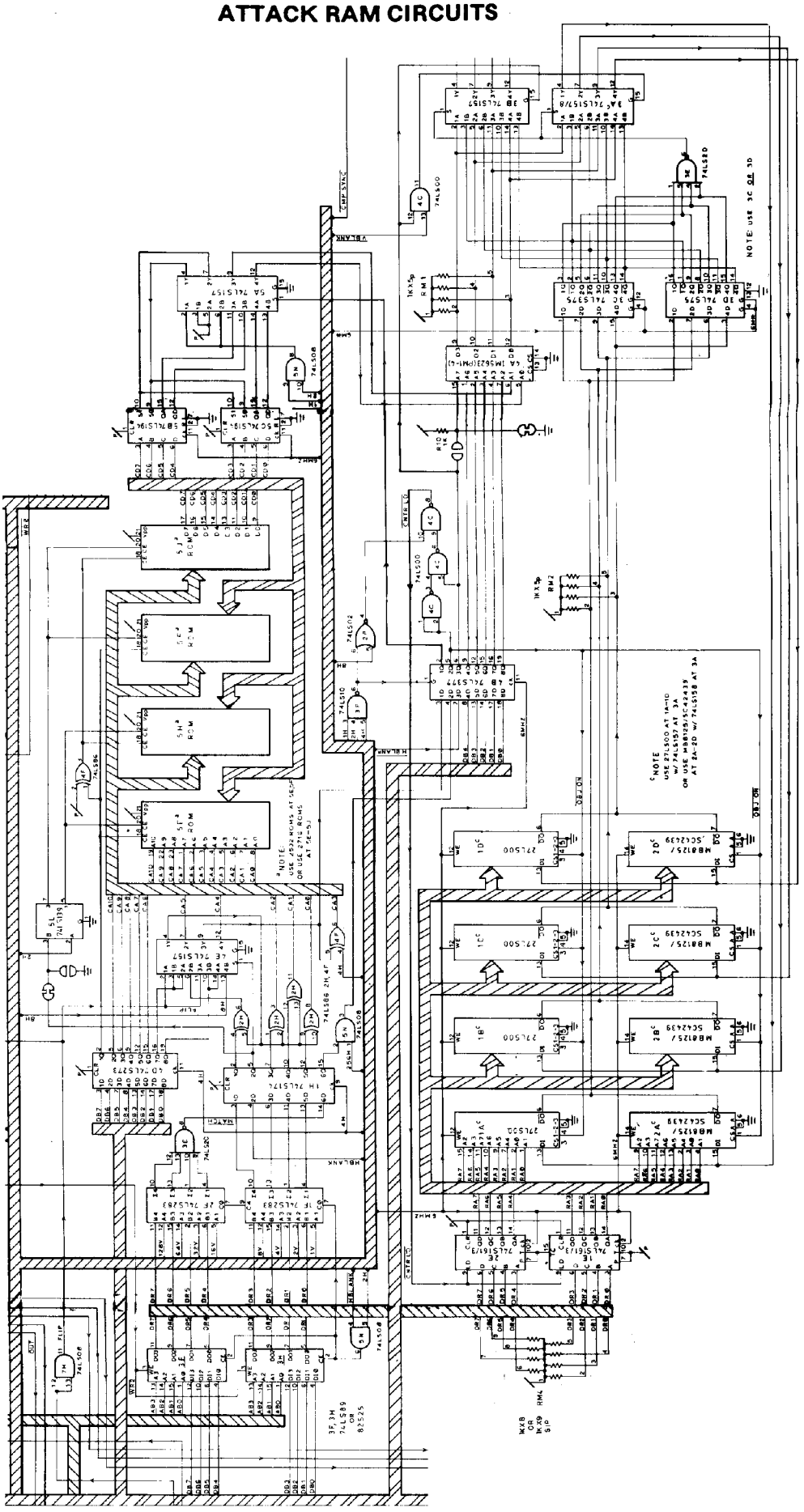
Data enters each attack RAM on pin 15. The attack RAM data leaving pin 7 is sent to either latch 3C or latch 3D (only one of these components are used on each board). From the latch this attack RAM data takes two paths. Like data from PROM PM1-4 it can either pass through multiplexer 3A and return to the attack RAM inputs or it can pass through multiplexer 3B to address the color PROM at location 7F.

A faulty attack RAM can cause the characters or their eyes to change color. The Pac-Man might disappear or the ghosts might be invisible except for a pair of eyes. If the attack RAM is only partially faulty, lines and dots might appear on the screen.

The easiest way to determine which attack RAM is faulty, is to momentarily force the output of each RAM high and to observe the screen. Connect one end of a jumper wire to +5VDC and use the other end to probe pin number 7 on each RAM. IMPORTANT: If a pulsing output is forced high for too long the component might be damaged. It is recommended that one force the RAM outputs high for no more than 5 or 10 seconds at a time. One may choose to use the switch 8 freeze option (See Section on Control Input Circuits) to make any change on the screen easier to see.

Each attack RAM will cause a change in the Pac-Man or ghosts when its output is forced high. (These RAMS do not affect the characters with nicknames during the attract mode.) For example, RAM 2B will cause Inky to turn red and the characters eyes to turn blue when its output is forced high. The purpose of forcing the attack RAM outputs high is to determine which RAM is associated with the symptoms. If the symptoms are blue eyes and Inky is red and if RAM 2A causes the Pac-Man to turn red, 2B does nothing, 2C causes Clyde to turn blue and 2D causes the Pac-Man to disappear, then RAM 2B is faulty. RAM 2B was already faulty so forcing its output high caused no change in the characters. Of course the symptoms might also be caused by a broken trace from the output of the RAM to the input of the latch. If the symptom is lines on the screen, one of the RAMS will probably cause the lines to disappear when its output if forced high. Change the RAM that causes the lines to disappear.

ATTACK RAM CIRCUITS



THE COLOR PROM

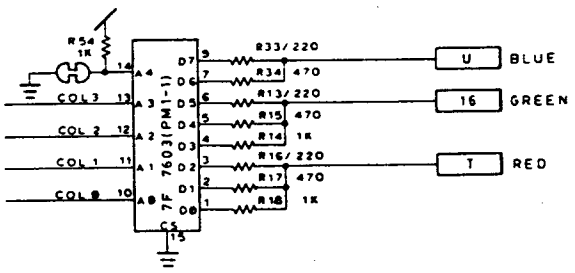
The "color" PROM PM-1 at location 7F receives the COL signals on its address inputs. Note that address input A4 is held low through a set of jumper pads. If these pads are disconnected and A4 is allowed to go high there will be no color output to the monitor.

The four COL signals can address sixteen different eight bit words in the color PROM. Each word will offer a different combination of red, green and blue signals to the monitor. The eight bit word will also determine the intensity of each color.

Examine the D0, D1 and D2 outputs on pin numbers 1, 2 and 3 of the color PROM. If pin number 1 goes high current will pass through a one thousand ohm resistor and the red color will be low intensity. If pin 2 goes high the red color will be more intense and if pin 3 goes high current passses through only 220 ohms for very intense red. A "resistor ladder" circuit is also used for the green and blue signals.

The color at a given point on the monitor screen is determined by the combination of the red, green and blue signals from PROM PM1-1. For example, the eight bit word 01010100 will produce a color mixture of low intensity blue, medium intensity green and high intensity red. The word 10000100 will turn on the red and blue signals to produce purple. The word 10100100 mixes equal parts of red, green and blue to produce white.

COLOR PROM



AUDIO CIRCUITRY

AB0 through AB3 from the buffered address bus and 4H through 32H from the system timing bus are multiplexed by the chip at location 3L and then used to address RAMS 2K and 2L. These RAMS are 16 X 4 (16 words by 4 bits per word) bipolar chips and either number 74S89 or 82S25 can be used. The 74LS157 at location 3L will pass the buffered address signals to the RAMS when its select input on pin number 1 is low. Note that the signal on pin 1 of 3L is actually the 2H signal which has been buffered by the XOR gate at 4F. When the select input is high the H signals will pass through 3L to addres the RAMS.

Buffered data lines DB0 through DB3 and the 2Q, 3Q, 4Q and 5Q outputs from chip 1L are multiplexed at 3K to supply data to RAMS 2K and 2L. The 74LS158 multiplexer at location 3K is identical to a 74LS157 except that its outputs are inverting.

PROM PM1-2 at location 3M is addressed by the 1H through 32H signals. Note that WRO supplies the A6 input and the A7 input is held low through a set of jumper pads. The 4 bit word on the PROM outputs is used to clock chips 1L and 2M and to clear chip 2M. The D1 output is used as WE (write enable) to RAM 2K. WR1 supplies the WE input on RAM 2L. It is interesting to note that the chip select input on PROM PM1-2 is driven by the 6M* signal which is faster than the clocking for the Z80 CPU.

With the circuitry described so far we can address and load data into the RAMS and PROM PM1-2 will control the flow of data from the RAMS through chips 1K and 1L to the "sound" PROM PM1-3. The signals sent to the final audio stage will have come from the sound PROM.

The 4 bit words from RAMS 2K and 2L are added by the 74LS283 at location 1K. The sum is passed through 1L to address the sound PROM. Address inputs A5, A6 and A7 of the sound PROM are driven directly from the outputs of RAM 2K.

The four lines of data leaving the sound PROM enter the 5D, 6D, 7D and 8D inputs of chip 2M.

FINAL AUDIO STAGES

In this last section of the audio circuitry, digital sound information from PROM 1M must pass through flip-flops 2M and then be reduced or mixed to a single line of analog data for the final amplifier at 11A.

The digital sound information enters 2M at the 5D, 6D, 7D and 8D inputs. 2M is clocked by pin number 10 of PROM 3M and cleared by the "sound on" signal from pin 1 of either 7K or 8K (only one of these chips are used in each game). The "sound on" signal goes high to enable 2M.

The sound information leaves 2M on its 5Q, 6Q, 7Q and 8Q outputs and is still in digital form. Note that each of these four outputs are connected to a resistor and that after resistors R6, R7, R8 and R9, the four lines are shorted together. In this way each input on the chip at 1N sees all four sound lines. The chip at 1N contains four electronic switches. Look at the bottom switch in schematic on page 54. Information will enter pin 8 and pass to pin 9 only when the control pin number 6 is high. The sound lines pass through these switches unchanged except that each switch offers some slight resistance. As one can see the control pins on 1N are driven by the 1Q, 2Q, 3Q and 4Q outputs of 2M. The signals on the electronic switch outputs are no longer of a TTL level (high near +5VDC and low near 0 volts) and may be considered analog. Each switch output is passed through a resistor and then once again the four sound lines are shorted together. Note capacitor C1 at the junction of the four lines, if it is shorted, ground would pass through it and hold the junction low causing no audio signal to the amplifier. From capacitor C1 this signal line of sound information passes through the volume control (10K potentiometer) to input pins 6 and 9 of the amplifier at 11A.

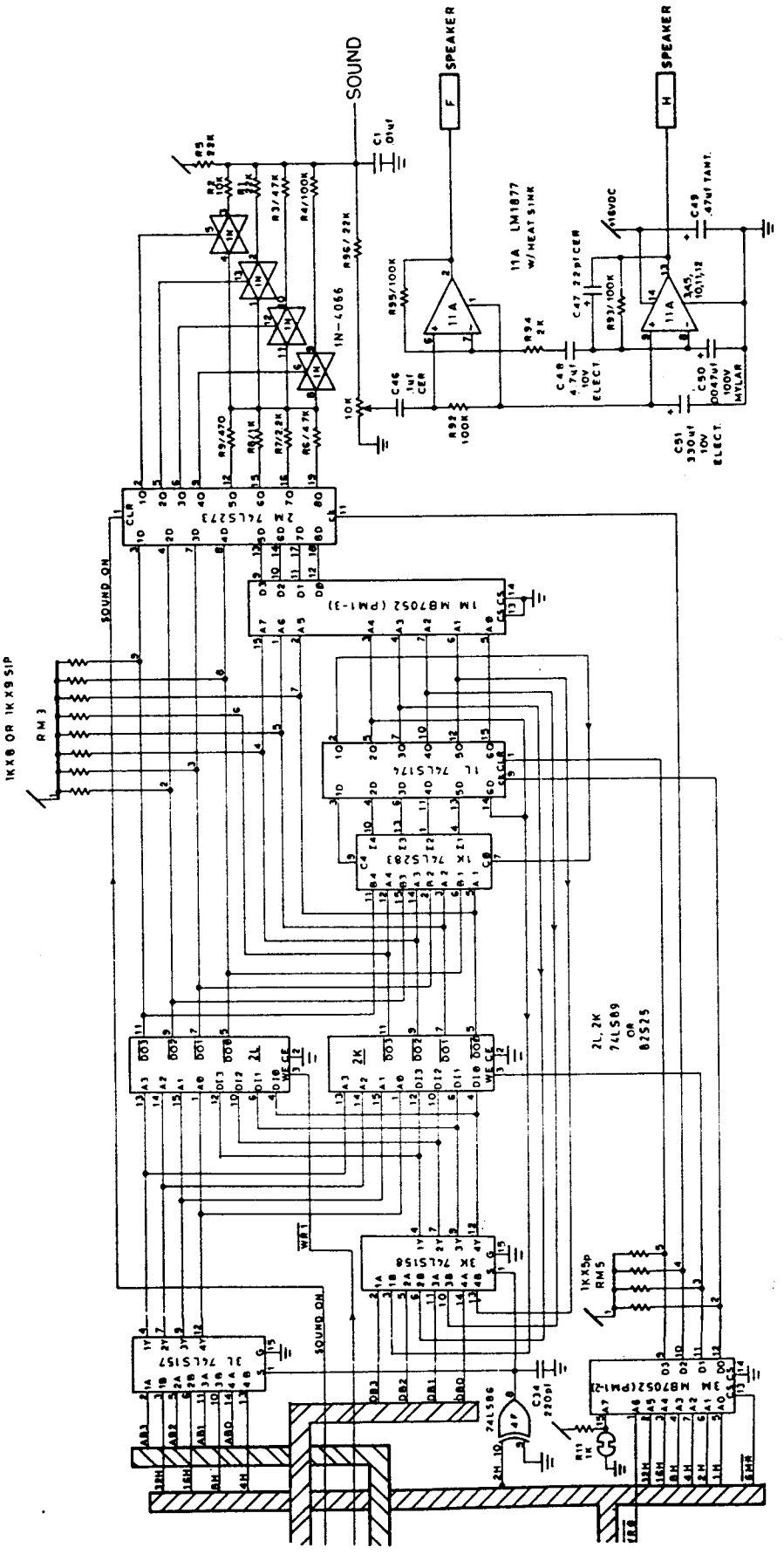
An easy way to check the audio amplifier is to tap your fingers underneath the board on the input pins of the amplifier. If you hear a loud thumping or scratching through the speaker, the amplifier is probably good.

The game will lose all sound if +16VDC does not reach pin 14 of the amplifier, if the amplifier itself is bad or if the volume control is open. Naturally, if there is a loose connection to the speaker or if the speaker is bad all sound will be lost. If a loud

humming occurs continuously, the amplifier or one of the capacitors near it may be bad. Humming can also be caused by a bad filter capacitor on the +16VDC line or if 12VAC is not reaching pin X or pin W on the main connector.

If only part of the sound is missing or distorted it is recommended that one start at the outputs of 1N and work backwards through 2M and on. As one can see, if a switch in chip 1N were bad any sound coming through that switch would be effected. If instead of sound only clicking is heard, check RAMS 2K and 2L and PROM 3M. Remember, most sounds can be checked by closing the movement, start or coin switches during the test mode and don't forget to use the switch number 8 freeze option for troubleshooting sounds that occur briefly and only once during a game, like the bonus sound.

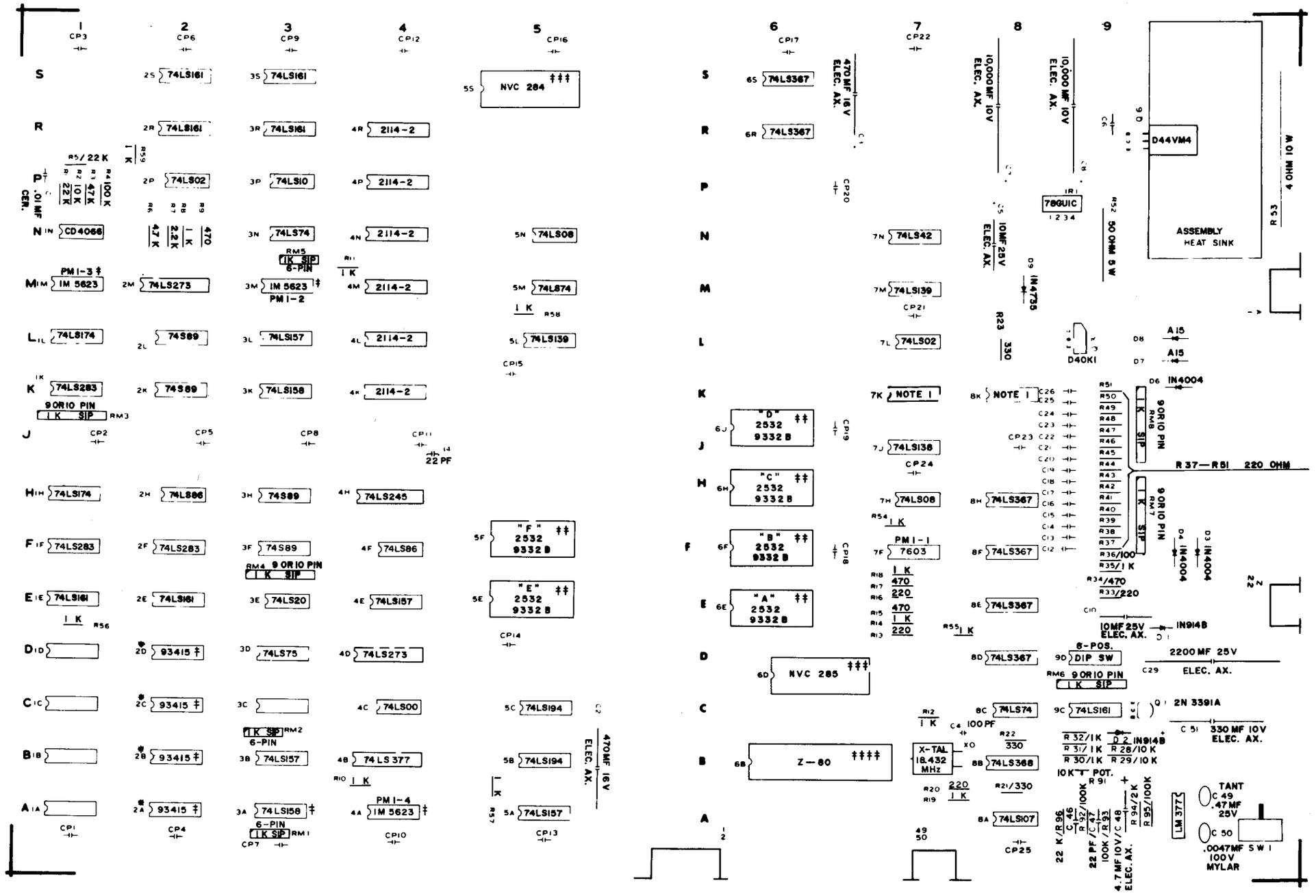
AUDIO CIRCUITRY



MS. PAC-MAN AUXILIARY BOARD
(PC A804-91415-B617)

To determine which board (the main logic board or the Ms. Pac-Man auxiliary board) is faulty, first remove the ribbon cable from the 40 pin socket at location 6B on the main logic board. Then remove the Z80 from the auxiliary board and insert it into socket 6B on the main logic board. If the main logic board is good the game will function as a Pac-Man except that Ms. Pac-Man will eat the dots and her mouth will open 180°. To completely convert the main logic board to Pac-Man simply change the character ROMS at locations 5E and 5F.

The main logic board and the program ROMS are identical in both Pac-Man and Ms. Pac-Man. The Ms. Pac-Man auxiliary board periodically interrupts the main program to create the new mazes and game patterns. The character ROMS at 5E and 5F add her bow, lipstick and glamour.



* RAM HEAT SINK ASSEMLY

NOTE 1: PLACE EITHER 74LS259 IN LOC. 8K
OR CD4099 IN LOC. 7K

UNMARKED CAPS ARE .1MF CER. AX.

RESISTOR UNIT = Ohm

‡ — 16 PIN SOCKET (9 PER)

‡‡ — 24 PIN SOCKET (6 PER)

‡‡‡ — 28 PIN SOCKET (2 PER)

‡‡‡‡ — 40 PIN SOCKET (1 PER)

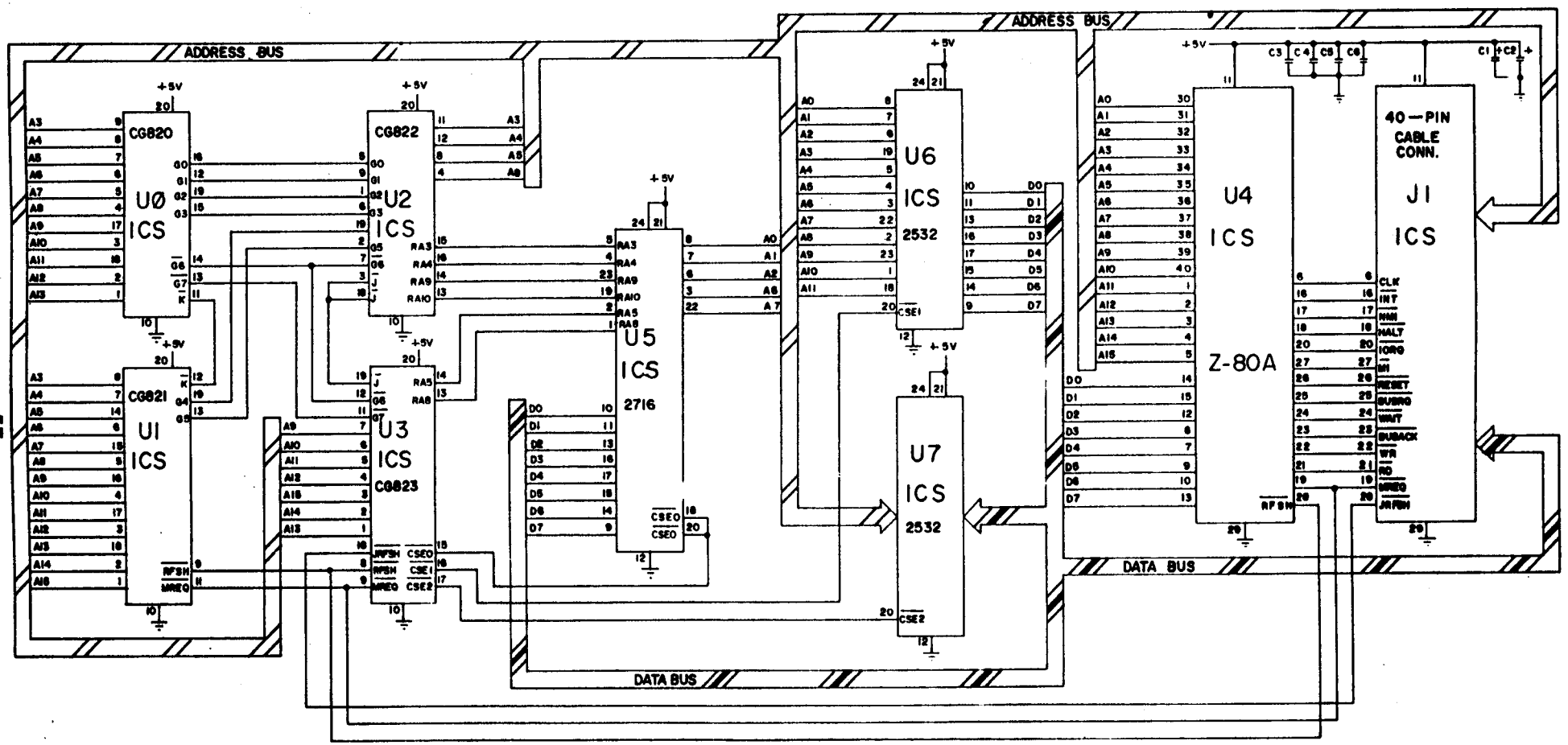
SHEET 11

M051-00932-A026

DO NOT SCALE DWG	HEAT TREAT	SCALE	USED ON PAC-MAN "A"
DIM TOLERANCES UNLESS SPECIFIED	DWN C.L.	MATL	NO REQ'D 1 PER
CONCENTRICITY T.I.R. .001 FRACTIONAL 1/64 DECIMAL .005 HOLE DIA +.002 .000	CKD	FINISH	ASSEMBLY DRAWING PAC—MAN
	DATE 10/9/80		PART NO. A082-91375-A000

REVISIONS

MIDWAY MFG. CO.
FRANKLIN PK. ILL.



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PROJECT ENG: J. SZERSZEN

MS. PAC-MAN

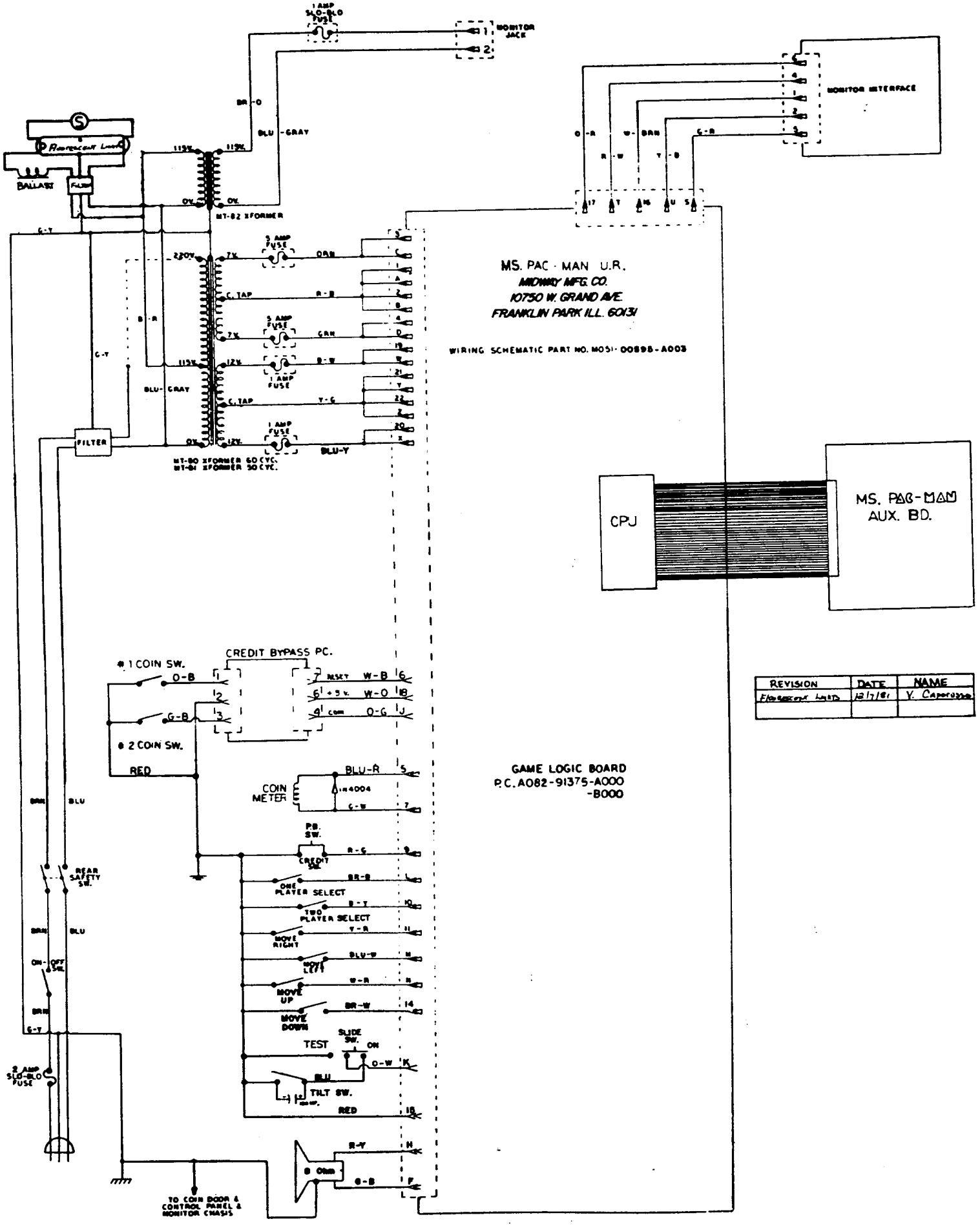
1/4/81 FULL

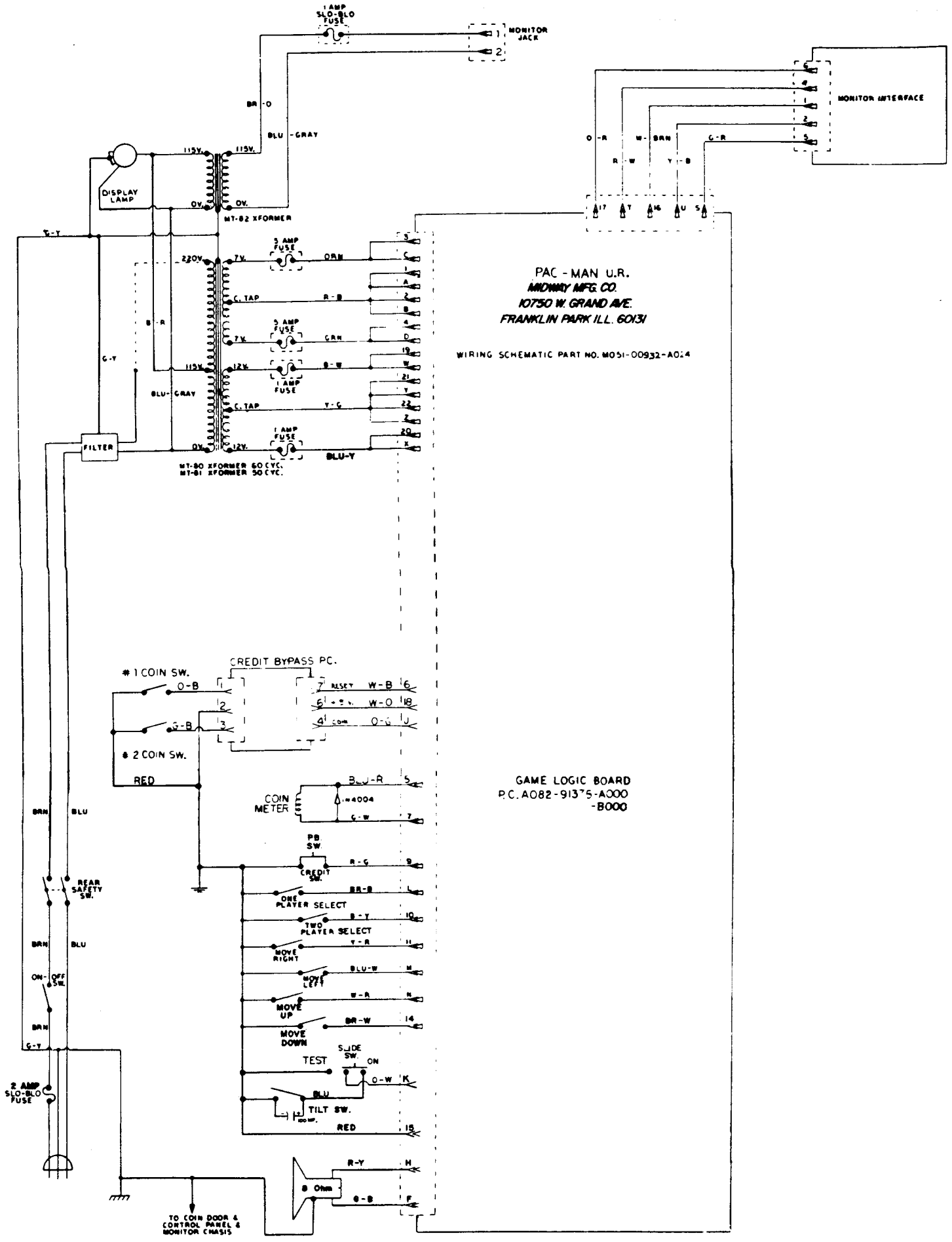
MIDWAY MFG. CO.

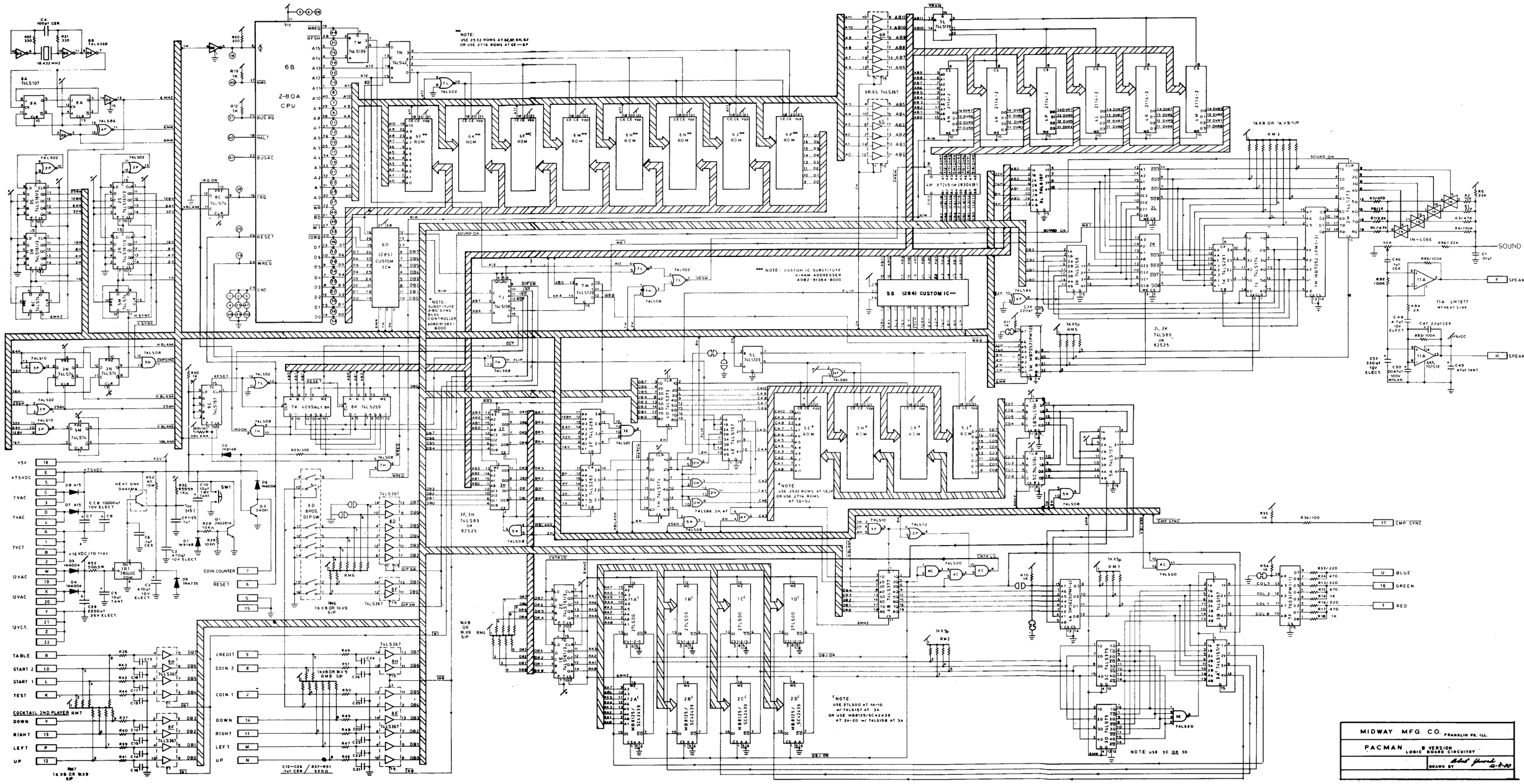
MS. PAC-MAN P.C.
A084-91415-0617
SCHEMATIC

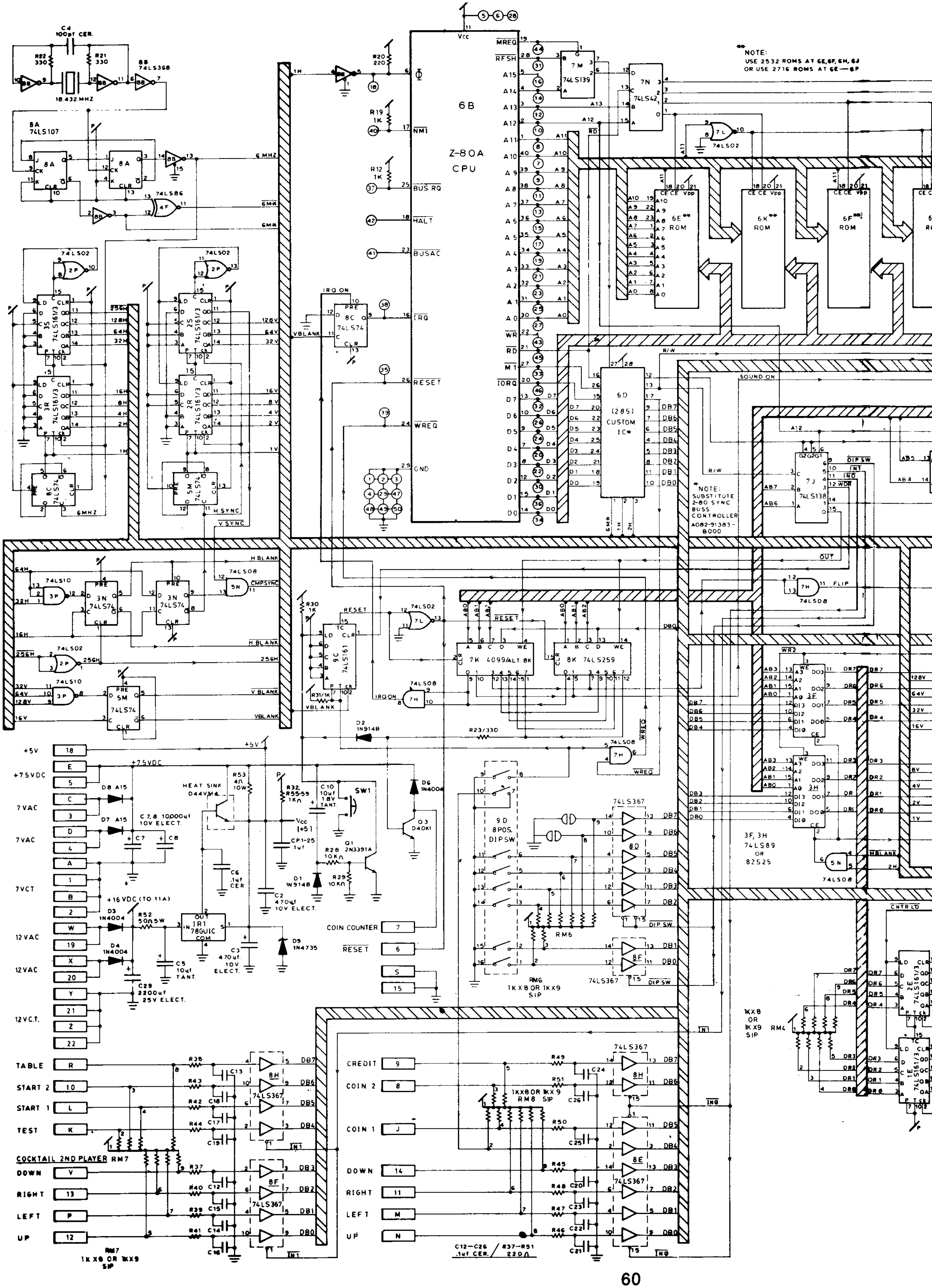
REVISIONS

M051-00617-0002

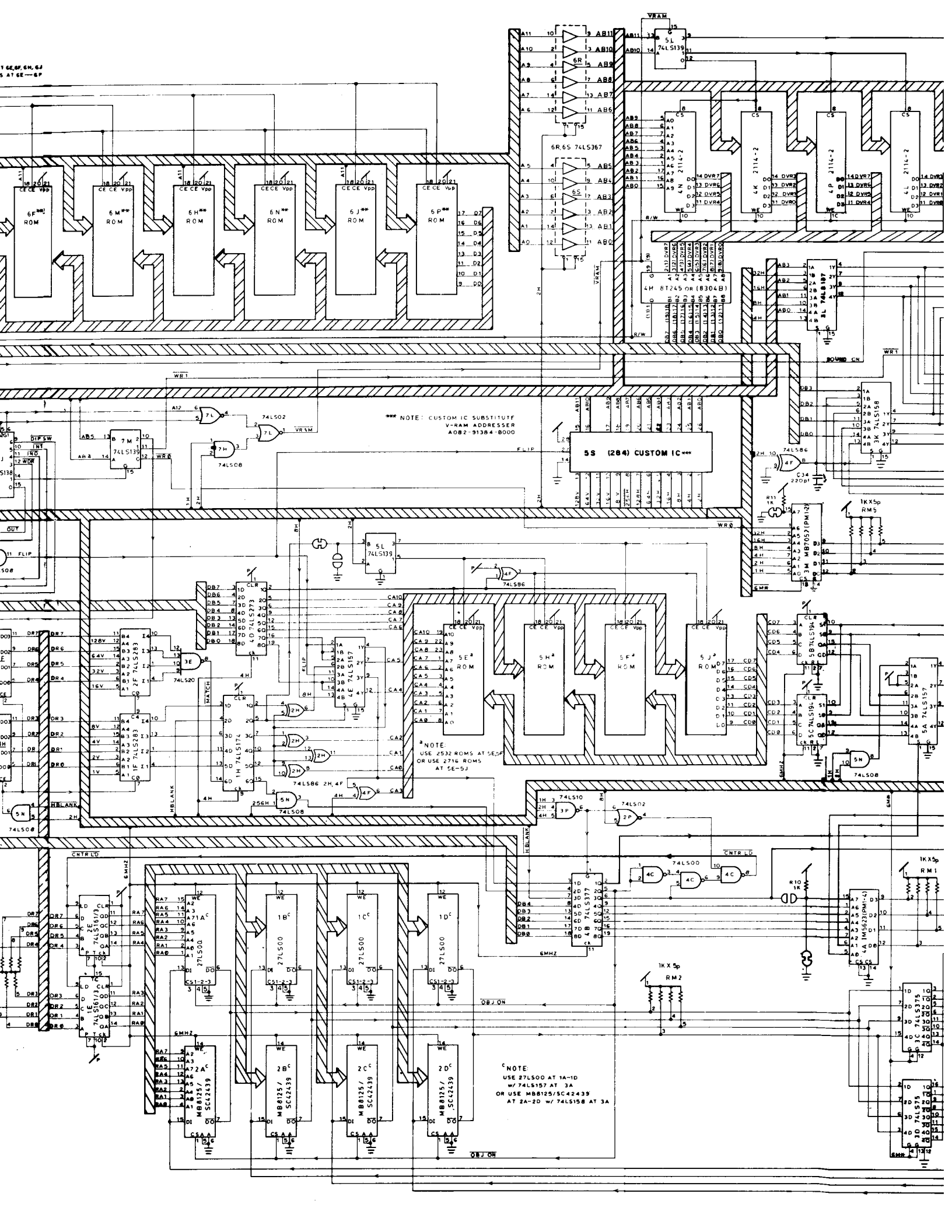

MS. PAC · MAN U.R.
MIDWAY MFG. CO.
10750 W. GRAND AVE.
FRANKLIN PARK ILL. 60131
WIRING SCHEMATIC PART NO. MOSI-00898-A003
MONITOR INTERFACE
MONITOR JACK
1 AMP SLO-BLO FUSE
MT-82 XFORMER
MT-80 XFORMER 60 CYC.
MT-81 XFORMER 50 CYC.
5 AMP FUSE
1 AMP FUSE
FILTER
BALLAST
CPU
MS. PAC-MAN AUX. BD.
CREDIT BYPASS PC.
#1 COIN SW.
#2 COIN SW.
COIN METER
PB. SW.
CREDIT SW.
ONE PLAYER SELECT
TWO PLAYER SELECT
MOVE RIGHT
MOVE LEFT
MOVE UP
MOVE DOWN
TEST
SLIDE SW.
TILT SW.
REAR SAFETY SW.
ON-OFF SW.
2 AMP SLO-BLO FUSE
8 Ohm
TO COIN DOOR & CONTROL PANEL & MONITOR CHASIS
GAME LOGIC BOARD
P.C.A082-91375-A000
-B000
REVISION
DATE
NAME
Fluorescent Lamp
12/7/81
Y. Camerena

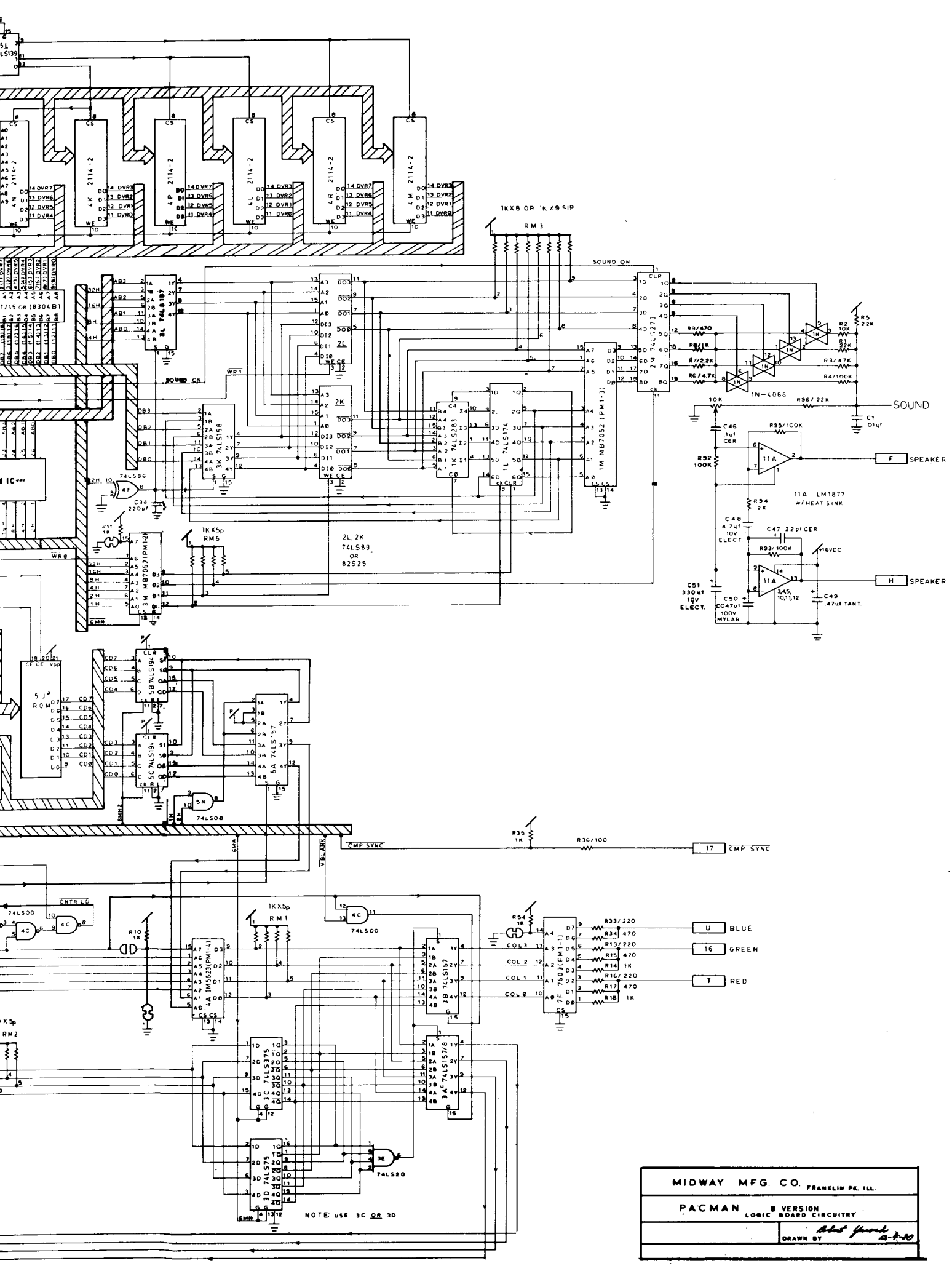

PAC - MAN U.R.
MIDWAY MFG. CO.
10750 W. GRAND AVE.
FRANKLIN PARK ILL. 60131
WIRING SCHEMATIC PART NO. MOSI-00932-A014
GAME LOGIC BOARD
P.C. A082-91375-A000
-B000
MONITOR INTERFACE
MONITOR JACK
1 AMP SLO-BLO FUSE
DISPLAY LAMP
MT-82 XFORMER
MT-80 XFORMER 60 CYC.
MT-81 XFORMER 50 CYC.
FILTER
5 AMP FUSE
1 AMP FUSE
2 AMP SLO-BLO FUSE
CREDIT BYPASS PC.
#1 COIN SW.
#2 COIN SW.
COIN METER
PB SW
CREDIT SW.
ONE PLAYER SELECT
TWO PLAYER SELECT
MOVE RIGHT
MOVE LEFT
MOVE UP
MOVE DOWN
TEST
SLIDE SW.
TILT SW.
REAR SAFETY SW.
ON-OFF SW.
8 Ohm
TO COIN DOOR & CONTROL PANEL & MONITOR CHASIS


6B
Z-80A CPU
6A 2114-2
6B 2114-2
6C 2114-2
6D 2114-2
6E 2114-2
6F 2114-2
6H ROM
6J ROM
6K ROM
6L ROM
6M ROM
6N ROM
6P ROM
5S (284) CUSTOM IC
5H ROM
5J ROM
5K ROM
5L ROM
6D (285) CUSTOM IC
SOUND ON
SPEAKER
SOUND
CMP SYNC
BLUE
GREEN
RED
CREDIT
COIN 2
COIN 1
DOWN
RIGHT
LEFT
UP
TABLE
START 2
START 1
TEST
COCKTAIL 2ND PLAYER RM7
COIN COUNTER
RESET
8 POS. DIPSW
1K X 8 OR 1K X 9 SIP
NOTE: USE 3C OR 3D
MIDWAY MFG. CO. FRANKLIN PK. ILL.
PACMAN 8 VERSION
LOGIC BOARD CIRCUITRY
DRAWN BY



NOTE:
USE 2532 ROMS AT 6E,6F,6H,6J
OR USE 2716 ROMS AT 6E—6P
6B
Z-80A
CPU
18.432 MHZ
6D
(285)
CUSTOM
IC*
NOTE:
SUBSTITUTE
Z-80 SYNC
BUSS
CONTROLLER
A082-91383-
B000
6E ROM
6K ROM
6F ROM
9D
8POS.
DIPSW
RM6
1K X8 OR 1K X9
SIP
3F, 3H
74LS89
OR
82S25
TABLE
START 2
START 1
TEST
COCKTAIL 2ND PLAYER RM7
DOWN
RIGHT
LEFT
UP
RM7
1K X8 OR 1K X9
SIP
CREDIT
COIN 2
COIN 1
COIN COUNTER
RESET
C12—C26
.1uf CER.
R37—R51
220Ω


*** NOTE: CUSTOM IC SUBSTITUTE V-RAM ADDRESSER A082-91384-8000
5S (284) CUSTOM IC***
[a] NOTE: USE 2532 ROMS AT 5E,5F OR USE 2716 ROMS AT 5E-5J
[c] NOTE: USE 27LS00 AT 1A-1D W/ 74LS157 AT 3A OR USE MB8125/SC42439 AT 2A-2D W/ 74LS158 AT 3A
6R,6S 74LS367
4H 8T245 OR (8304B)
VRAM
WRT
WRQ
FLIP
CNTR LD
OBJ ON
H BLANK
6MHZ


1KX8 OR 1KX9 SIP
RM 3
SOUND ON
WR1
2L
2K
1L
74LS89
OR
82S25
1KX5p
RM5
1N-4066
SOUND
SPEAKER
11A LM1877
W/HEAT SINK
CMP SYNC
BLUE
GREEN
RED
1KX5p
RM1
74LS00
74LS08
74LS20
NOTE: USE 3C OR 3D
MIDWAY MFG. CO. FRANKLIN PK. ILL.
PACMAN 8 VERSION
LOGIC BOARD CIRCUITRY
DRAWN BY

PAC - MAN

PC A082-91375-A000

CHIP NUMBER	FUNCTION
74LS00	Quad 2 Input Nand
74LS02	Quad 2 Input Nor
74LS08	Quad 2 Input And
74LS10	Triple 3 Input Nand
74LS20	Dual 4 Input Nand
74LS42	BCD to Decimal Decoder
74LS74	Dual "D" Flip-Flop
74LS75	Quad Latch
74LS86	Quad 2 Input Exclusive or
74S89	64 Bit Ram 16 x 4
74LS107	Dual "JK" Flip-Flop
74LS138	3 to 8 Line Decoder
74LS139	Dual 2 to 4 Line Decoder
74LS157	Quad 2 to 1 Line Multiplexer
74LS158	Quad 2 to 1 Line Multiplexer Inverting
74LS161	4 Bit Binary Counter
74LS174	Hex "D" Flip-Flop
74LS194	8 Bit Shift Register
74LS245	Octal Bus Transceiver
74LS259	8 Bit Addressable Latch
74LS273	Octal "D" Flip-Flop
74LS283	4 Bit Full Adder
74LS367	Hex Bus Driver
74LS368	Hex Bus Driver Inverting
74LS377	Octal "D" Flip-Flop
Z80	CPU
LM377 - LM1877	Dual Audio Amplifier
NVC284	Custom V Ram Addresser
NVC285	Custom Z80 Sync Buss Controller
CD4066	Quad Bilateral Switch

CHIP NUMBER	FUNCTION
2114	Ram 1K x 4
1M5623	Prom 256 x 4
7603	Prom 32 x 8
MCM 2532	Prom 4K x 8
SL 4239	Ram 1K x 1
93415	Ram 1K x 1
27LS00	Ram 1K x 1
MB 8125	Ram 1K x 1
CD 4099	8 Bit Addressable Latch
N8T245	Octal Bus Transceiver
54LS174	Hex "D" Flip-Flop
MB7052	Prom 256 x 4
MB7051	Prom 32 x 8
8304	Octal Bus Transceiver

ADDITIONAL DEVICES

18.4320	Crystal
78GVIC	Voltage Regulator
D44VM4	Transistor NPN
D40K1	Transistor NPN
2N3391	Transistor NPN
1N4004	Diode
A15	Diode
1N914B	Diode
1N4737	6.2V Zener Diode

SERVICE BULLETIN

GAME: PAC-MAN

SUBJECT: Custom Chips 6-D and 5-S

When the custom chips are not available due to a supply problem the following alternate plug in units will be used.

1. At location 6-D PC 082-91383-B000 Z80 sync buss controller.

2. At location 5-S PC 082-91384-B000 V-Ram Addresser.

PAC - MAN

V - RAM ADDRESSER (284)

 # A082-91384-B000

CHIP NUMBER	FUNCTION
74LS02	Quad 2 Input Nor
74LS86	Quad 2 Input Exclusive or
74LS157	Quad 2 to 1 Line Multiplexer
74LS257	Quad 2 to 1 Line Multiplexer-Tri State

Z - 80 SYNC BUSS CONTROLLER (285)

 # A082-91383-B000

74LS02	Quad 2 Input Nor
74LS74	Dual "D" Flip-Flop
74LS139	Dual 2 to 4 Line Decoder
74LS244	Octal Buffers - Tri State
74LS374	Octal "D" Flip-Flop-Tri State

MS. PAC-MAN

AUXILIARY P. C. A084-91415-B617

CHIP NUMBER	FUNCTION
Z80	CPU
2532	4K X 8 EPROM
2716	2K X 8 EPROM
CG820	Custom Component
CG821	Custom Component
CG822	Custom Component
CG823	Custom Component

CABLE – MIDCO
TELEX NO. 72-1596

MIDWAY MFG. CO.
A BALLY COMPANY
10750 W. GRAND AVENUE • FRANKLIN PARK, ILL. 60131

PHONE: AREA CODE 312 451-1360
CHICAGO PHONE: 992-2250

February 12, 1982

SERVICE BULLETIN

GAME: MS. PAC-MAN

SUBJECT: MS. PAC-MAN MAIN LOGIC BOARD
(PC A082-91375-B000)

1. The main "Ms. Pac-Man" logic board is the same logic board as in Pac-Man.

2. There are two minor changes:

   A. Character Proms at 5E and 5F are Ms. Pac-Man type.

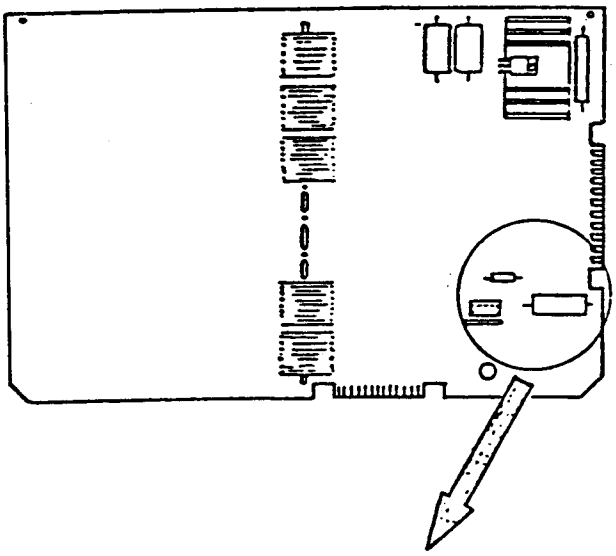
   B. The Z80 is removed and inserted into Ms. Pac-Man auxiliary board (PC A084-91415-B617).

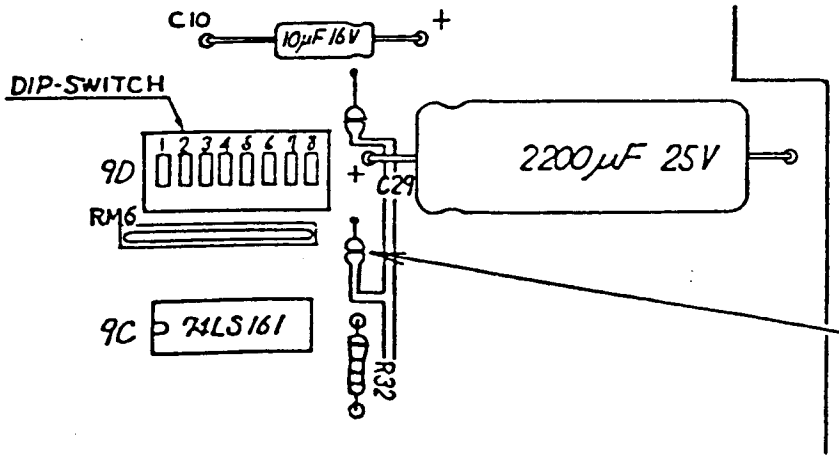
Andy Ducay
Service Manager

AD/dd

INSTRUCTIONS FOR MODIFICATION OF PAC-MAN GAME PCB

THE FOLLOWING ARE INSTRUCTIONS FOR MODIFYING PAC-MAN PCB SUCH THAT ① THE DEGREE OF DIFFICULTY OF THE GAME IS INCREASED.





CABLE – MIDCO
TELEX NO. 72-1596

MIDWAY MFG. CO.
A BALLY COMPANY
10750 W. GRAND AVENUE • FRANKLIN PARK, ILL. 60131

PHONE: AREA CODE 312 451-1360
CHICAGO PHONE: 992-2250

December 3, 1980

SERVICE BULLETIN

GAME: PAC - MAN

SUBJECT: STATIC CONDITION CAUSING A FALSE RAM AND ROM TEST.

MODIFICATION:

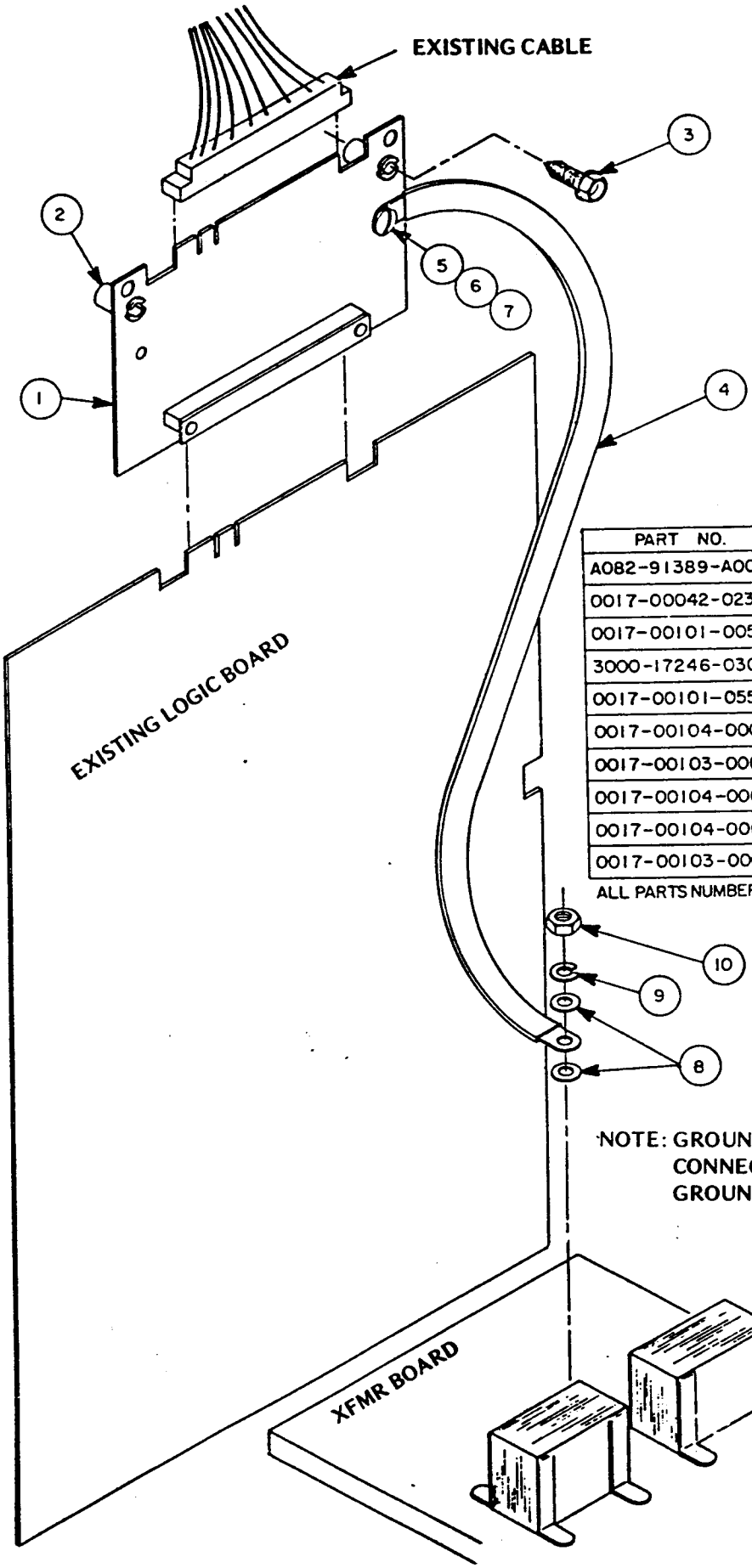
1. ORDER FROM MIDWAY'S SERVICE DEPARTMENT A ANTI-STATIC KIT PC A082-91389-A000 AND INSTALL AS SHOWN IN INSTRUCTION DIAGRAM. (FIGURE #1).

2. CHECK GAME OUT ELECTRICALLY.

ANDY DUCAY
SERVICE MANAGER

ANTI-STATIC INSTALLATION INSTRUCTIONS

FIGURE #1



PART NO.	QTY	DESCRIPTION	ITEM
A082-91389-A000	1	FILTER P.C. BOARD ASSY.	1
0017-00042-0237	2	SPACER	2
0017-00101-0052	2	6x1 1/4 SLT HEX HD SCREW	3
3000-17246-0300	1	GROUND STRAP	4
0017-00101-0551	1	6-32x 1/4 BIND. HD. M.S.	5
0017-00104-0002	1	6 SPLIT LOCK WSHR	6
0017-00103-0005	1	6-32 HEX NUT	7
0017-00104-0062	2	8 FLAT WSHR	8
0017-00104-0003	1	8 SPLIT LOCK WSHR	9
0017-00103-0008	1	8-32 HEX NUT	10

ALL PARTS NUMBERED INCLUDED IN KIT A866-00078-0000

NOTE: GROUND STRAP TO BE CONNECTED TO EXISTING GROUND STUD

MIDWAY MFG. CO.
A BALLY COMPANY

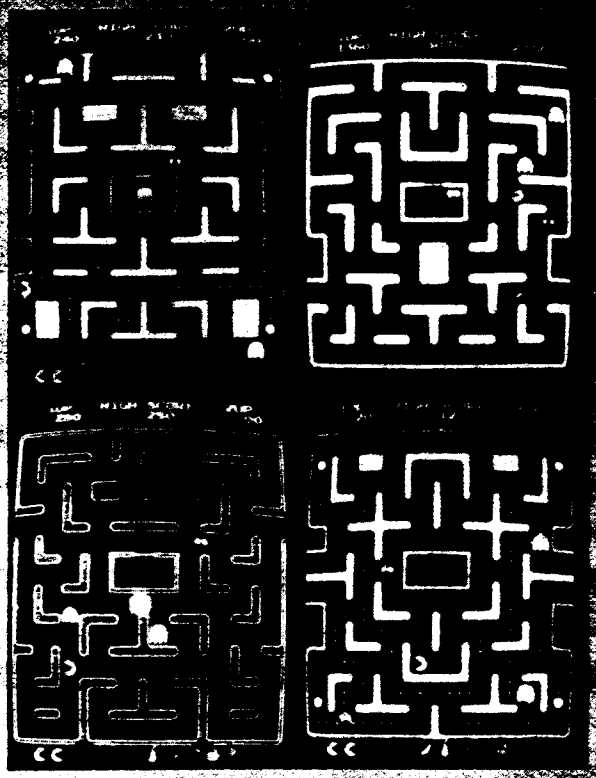
M051-00866-A019

Ms. PAC-MAN

A more challenging version of the well-known Pac-Man maze game, Ms. Pac-Man is sure to be the most popular girl in the game world.

Pursued by the familiar Inky, Blinky, Pinky and the newest ghost, Sue, Ms. Pac-Man goes through 4 new and changing mazes that increase in difficulty and offer varying side-exit locations. Each of the 4 mazes has an additional 2 side exits that give Ms. Pac-Man a total of 4 ways out of the maze.

Dots score 10 points each with Power Dots serving 50 points each. Points double for each ghost Ms. Pac-Man munches. 200 points for the first 400 [illegible] third and fourth ghosts while Ms. Pac-Man is caught [illegible] she dramatically swoons [illegible]



As in Pac-Man, bonus fruit symbols indicate how many times a player has cleared the screen of dots. Ms. Pac-Man boasts additional bonus fruit symbols that also float freely through the maze and have higher point values when gobbled.

100 points

200 points

500 points

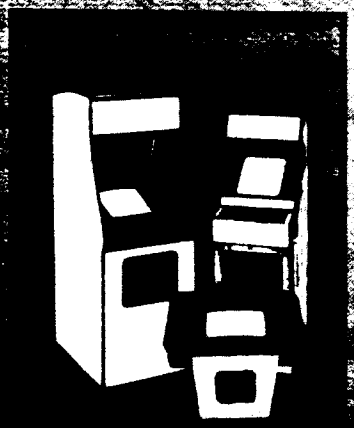
700 points

1,000 points

2,000 points

5,000 points

[illegible] with a new sound package players may witness the touching love story of Ms. Pac-Man's [illegible] Pac-Man himself, [illegible] courtship and marriage and even the delivery of Pac-Baby™ in the three act, between-maze cartoon series.



[illegible] with 22"

[illegible] Co. intends to assert its copyright and trademark rights in this game [illegible]