ATARI

Drawing Package Supplement

to

Cocktail WARLORDS™

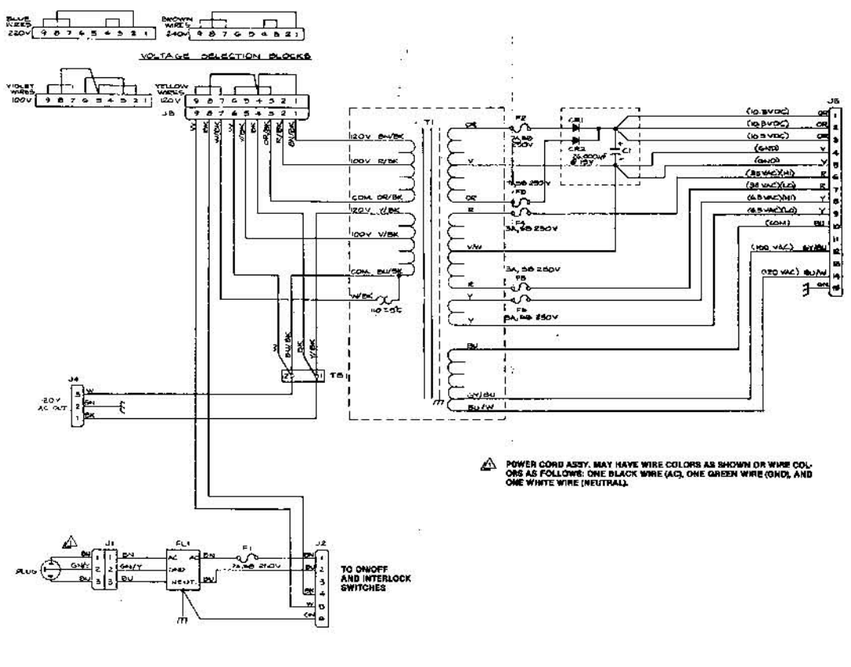
Operation, Maintenance, and Service Manual

Contents of this Drawing Package

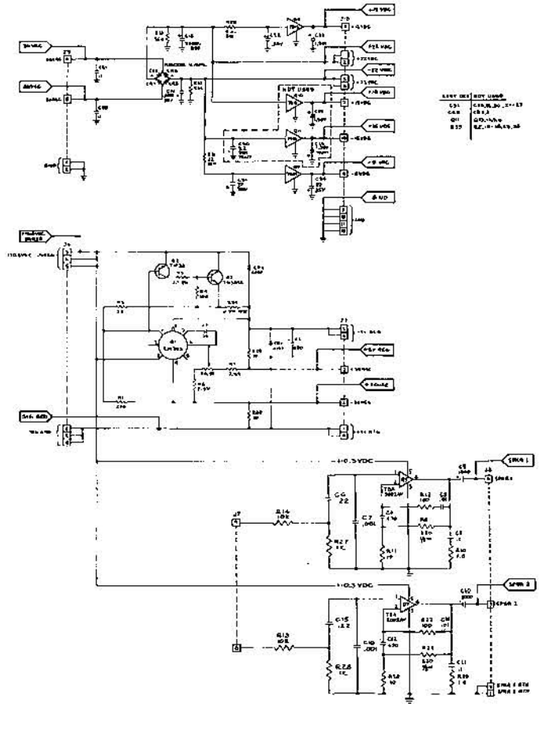
A Warner Communications Company

Sheet 1, Side A
DP-177-01 1st printing

Video Power Supply Wiring Diagram (036097-01 A)



Regulator/Audio II PCB Schematic (035435-02 D)



Regulator/Audio II PCB

The Regulator/Audio II PCB has the dual functions of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage regulator Q1, current source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through high-impedance inputs + SENSE and – SENSE. The inputs are directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage on the game PCB. This eliminates a reduced voltage due to IR buildup on the wire harness between the regulator and the game PCB. Variable resistor R6 is adjusted for the +5 VDC on the game PCB. Once adjusted, the voltage at the input of the game PCB will remain constant at this voltage.

Regulator Adjustment

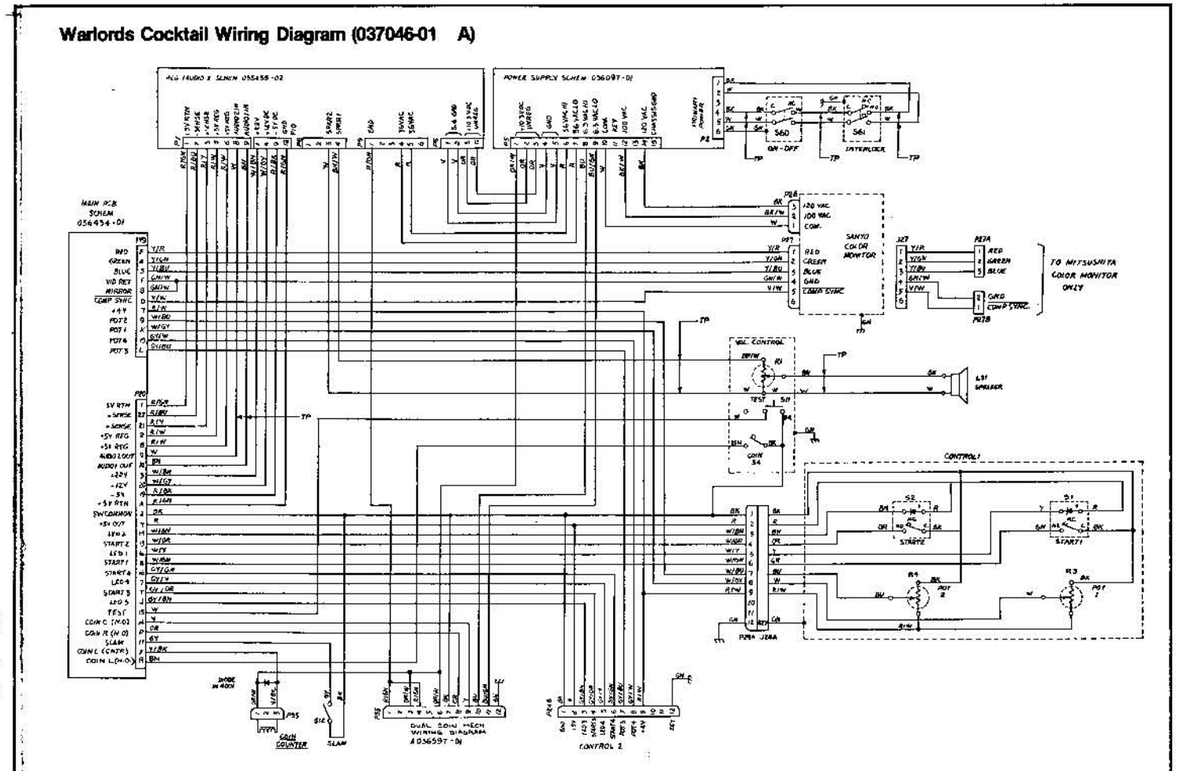
1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable resistor R6 on the Regulator/Audio II PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND on the Regulator/Audio II PCB. Voltage reading must not be greater than +5.5 VDC. If greater, try cleaning edge connectors on both the game PCB and the Regulator/Audio II PCB.
4. If cleaning PCB edge connectors doesn't decrease voltage difference, connect minus lead of voltmeter to GND test point of Regulator/Audio II PCB and plus lead to GND test point of game PCB. Note the voltage.
   Now connect minus lead of voltmeter to +5 REG test point on Regulator/Audio II PCB and plus lead to +5 V test point on game PCB. From this you can see which harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

Audio Circuit

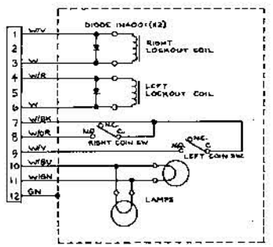
The audio circuit contains two independent audio amplifiers. Each amplifier consists of a TDA2002AV amplifier with a gain of ten.

Denotes a test point

Warlords Cocktail Wiring Diagram (037046-01 A)



Double Coin Acceptor/Mount Assembly (036597-01 A)



ATARI®

Sheet 1, Side B

WARLORDS™

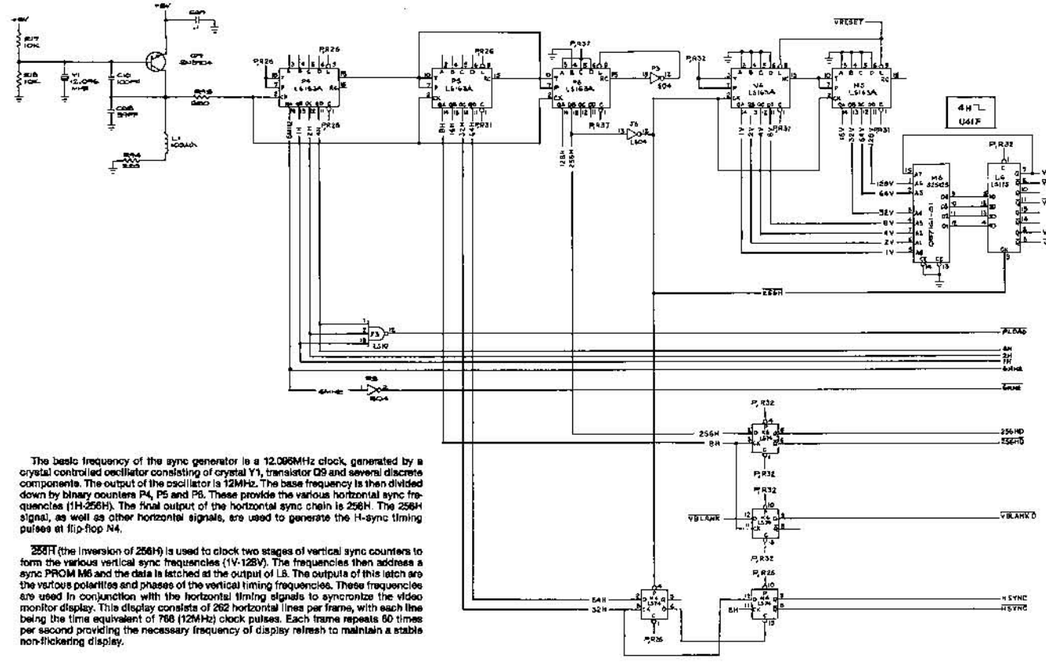
Sync Generator
MPU
Address Decoder
RAM
ROM
Power Input

Section of 036434-01 B

A Warner Communications Company

Sheet 1, Side B
DP-177-01 1st printing

Sync Generator Circuitry

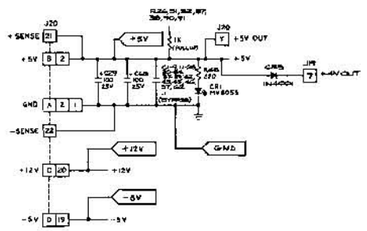


The basic frequency of the sync generator is a 12.096MHz clock, generated by a crystal controlled oscillator consisting of crystal Y1, transistor Q9 and several discrete components. The output of the oscillator is 12MHz. The base frequency is then divided down by binary counters P4, P5 and P6. These provide the various horizontal sync frequencies (1H-256H). The final output of the horizontal sync chain is 256H. The 256H signal, as well as other horizontal signals, are used to generate the H-sync timing pulses at flip-flop N4.

256H (the inversion of 256H) is used to clock two stages of vertical sync counters to form the various vertical sync frequencies (1V-128V). The frequencies then address a sync PROM M6 and the data is latched at the output of L8. The outputs of this latch are the various polarities and phases of the vertical timing frequencies. These frequencies are used in conjunction with the horizontal timing signals to synchronize the video monitor display. This display consists of 262 horizontal lines per frame, with each line being the time equivalent of 768 (12MHz) clock pulses. Each frame repeats 60 times per second providing the necessary frequency of display refresh to maintain a stable non-flickering display.

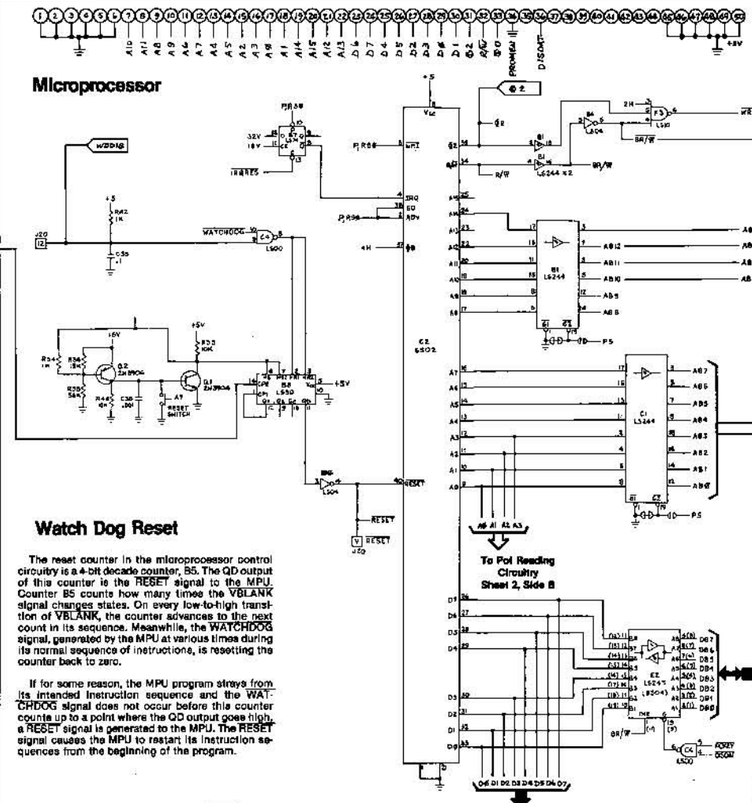
Denotes a signature

Power Input Circuitry



Denotes a test point

Microprocessor



Watch Dog Reset

The reset counter in the microprocessor control circuitry is a 4-bit decade counter, B5. The QD output of this counter is the RESET signal to the MPU. Counter B5 counts how many times the VBLANK signal changes states. On every low-to-high transition of VBLANK, the counter advances to the next count in its sequence. Meanwhile, the WATCHDOG signal, generated by the MPU at various times during its normal sequence of instructions, is resetting the counter back to zero.

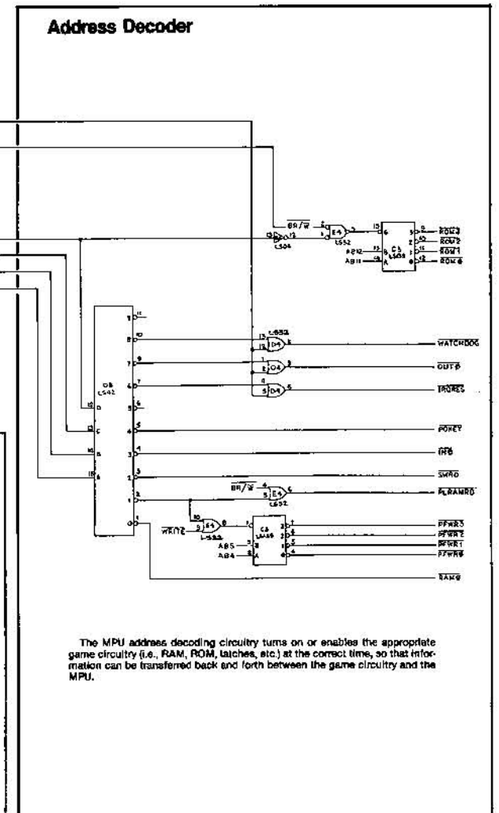
If for some reason, the MPU program strays from its intended instruction sequence and the WATCHDOG signal does not occur before this counter counts up to a point where the QD output goes high, a RESET signal is generated to the MPU. The RESET signal causes the MPU to restart its instruction sequences from the beginning of the program.

Denotes a test point

To Pot Reading Circuitry Sheet 2, Side B

To Sheet 2, Side B

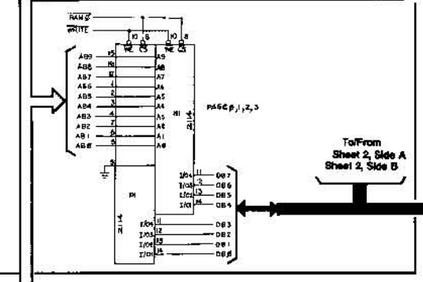
Address Decoder



The MPU address decoding circuitry turns on or enables the appropriate game circuitry (i.e., RAM, ROM, latches, etc.) at the correct time, so that information can be transferred back and forth between the game circuitry and the MPU.

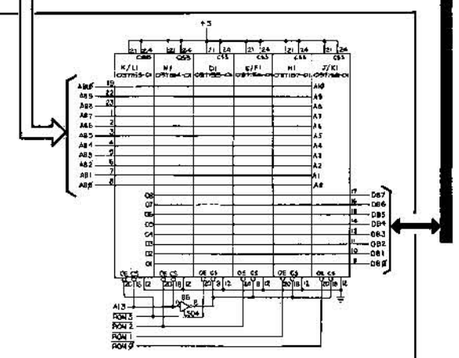
RAM Circuitry

The MPU uses RAM memory to temporarily store information which it will later recall. The MPU is capable of writing (putting data into) the RAM and then later reading (pulling data out of) the RAM, via address bus A00-A09 and bidirectional data bus D00-D07.



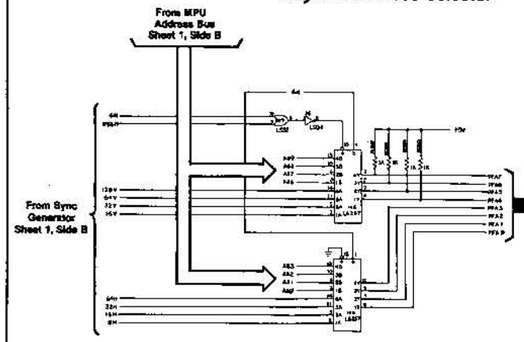
To/From Sheet 2, Side A Sheet 2, Side B

ROM Circuitry



MEMORY MAP									
HEXADECIMAL ADDRESS	R/W	DATA D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000-00FF		D	D	D	D	D	D	D	D	Program RAM
0400-07BF		D	D	D	D	D	D	D	D	Playfield RAM
07C0-07CF		D	D	D	D	D	D	D	D	Object Code
07D0-07DF		D	D	D	D	D	D	D	D	Vert. Position
07E0-07EF		D	D	D	D	D	D	D	D	Horiz. Position
0800	R			D						1 Player Cost
	R				D					2-4 Player Cost
	R						D			High-Score Music
	R								D	German/Spanish Language
	R								D	English/Spanish Language
0801	R	D	D							No. of Coins Per Credit
	R			D	D					Right Coin Mech
	R					D				Left Coin Mech
	R						D	D	D	Bonus Coin Adder
0000	R	D								Upright/Cocktail
	R		D							VBLANK
	R			D						Self-Test Switch
	R				D					Diag. Step Switch
0C01	R	D								Left Coin Switch
	R		D							Center Coin Switch
	R			D						Right Coin Switch
	R				D					Slam Switch
	R					D				Player Start (PS4)
	R						D			Player Start (PS3)
	R							D		Player Start (PS2)
	R								D	Player Start (PS1)
1000-100F		D	D	D	D	D	D	D	D	Custom Audio Chip
1800										IRQ Reset
1C00	W	D								Right Coin Counter
1C01	W	D								Center Coin Counter
1C02	W	D								Left Coin Counter
1C03	W	D								LED 1
1C04	W	D								LED 2
1C05	W	D								LED 3
1C06	W	D								LED 4
4000	W									Watchdog
5000-7FFF	R	D	D	D	D	D	D	D	D	Program ROM

Playfield Address Selector

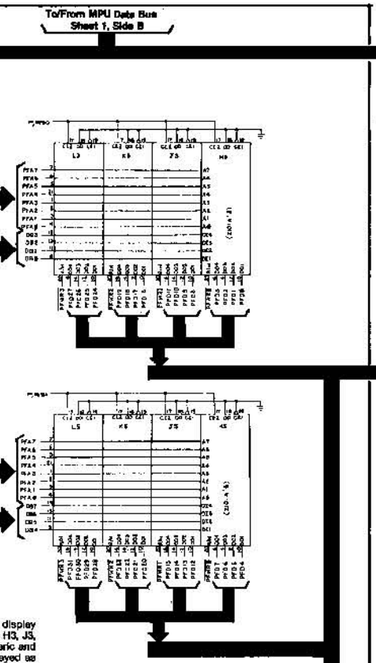


The Playfield Address Selector controls the access to the playfield memory. It allows either the game MPU or the sync generator to scan the playfield memory. The Playfield Address Selector consists of multiplexers M3, and M5 and gates J6 and N8.

When 4H on pin 1 of M3 and M5 is low and pin 15 on M5 is low, the Playfield Address Selector receives 8H, 16H, 32H, and 64H on M3 and 16V, 32V, 64V, and 128V on M5 from the sync generator. These signals enable the sync generator circuits to access the playfield memory.

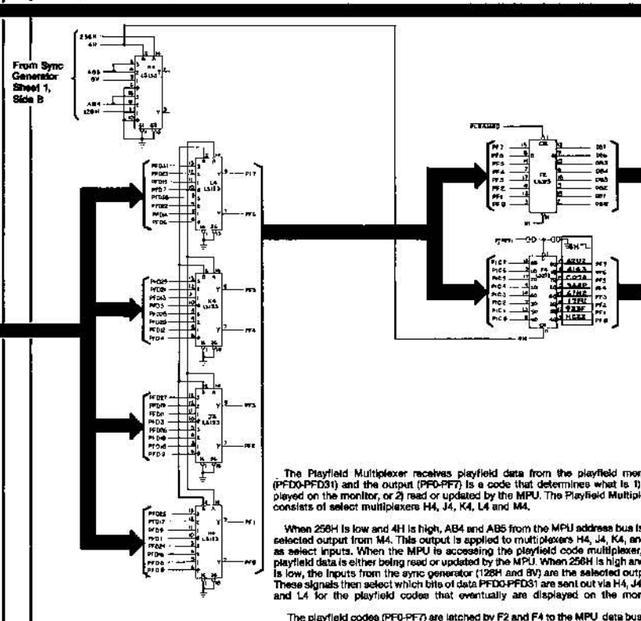
When 4H goes high the game MPU addresses the playfield memory (via AB0-AB9) for the positioning of the graphics. During horizontal blanking (pin 15 of M5 is high) the outputs of M5 (PFA4-PFA7) are held high enabling the motion object circuitry to access the playfield memory for the motion objects to be displayed.

Playfield Memory



The playfield RAM contains the playfield display information. The playfield RAM consists of H3, J3, K3, L3, H5, J5, K5, and L5. The alpha, numeric and the playfield picture components are displayed as 8-line by 8-bit blocks of video on the monitor screen. The microprocessor loads the playfield location bits into the playfield RAM via DB0-DB7 and the RAM outputs are PFD0-PFD31.

Playfield Multiplexer



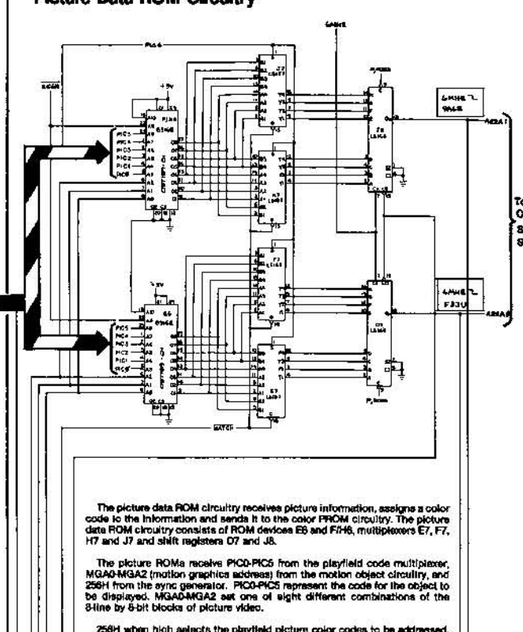
The Playfield Multiplexer receives playfield data from the playfield memory (PFD0-PFD31) and the output (PF0-PF7) is a code that determines what is 1) displayed on the monitor, or 2) read or updated by the MPU. The Playfield Multiplexer consists of select multiplexers H4, J4, K4, L4 and M4.

When 256H is low and 4H is high, AB4 and AB5 from the MPU address bus is the selected output from M4. This output is applied to multiplexers H4, J4, K4, and L4 as select inputs. When the MPU is accessing the playfield code multiplexer, the playfield data is either being read or updated by the MPU. When 256H is high and 4H is low, the inputs from the sync generator (128H and 8V) are the selected outputs. These signals then select which bits of data PFD0-PFD31 are sent out via H4, J4, K4, and L4 for the playfield codes that eventually are displayed on the monitor.

The playfield codes (PF0-PF7) are latched by F2 and F4 to the MPU data bus (F2) and to the picture data PROM circuitry (F4). When PLRAMD is low and 1H from the sync generator goes high, the inputs on F2 (PF0-PF7) are latched out to the MPU via DB0-DB7. When 4H on pin 11 of F4 goes high, the inputs (PF0-PF7) are latched to the picture data PROM circuitry.

Denotes a signature

Picture Data ROM Circuitry



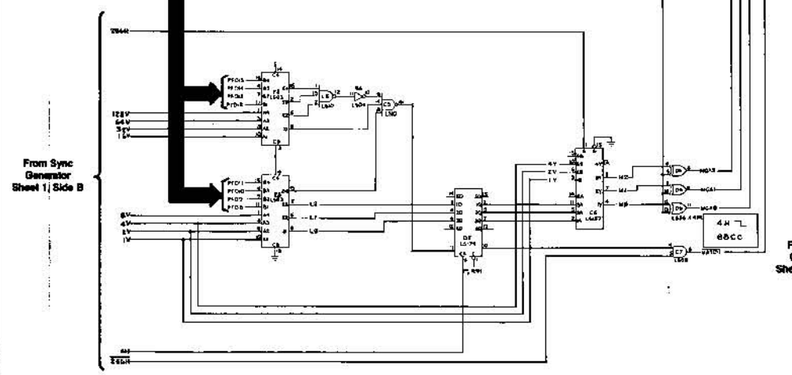
The picture data ROM circuitry receives picture information, assigns a color code to the information and sends it to the color PROM circuitry. The picture data ROM circuitry consists of ROM devices E6 and F/H6, multiplexers E7, F7, H7 and J7 and shift registers D7 and J8.

The picture ROMs receive PIC0-PIC5 from the playfield code multiplexer, MGA0-MGA2 (motion graphics address) from the motion object circuitry, and 256H from the sync generator. PIC0-PIC5 represent the code for the object to be displayed. MGA0-MGA2 set one of eight different combinations of the 8-line by 8-bit blocks of picture video.

256H when high selects the playfield picture color codes to be addressed. 256H when low selects the motion object color codes to be addressed. The picture data ROM outputs D1-D8 on E6 and F/H6, are multiplexed by E7, F7, H7 and J7, and shifted out serially at D7 and J8 as AREA0 and AREA1 to the motion object horizontal circuitry and the video output circuitry.

Denotes a signature

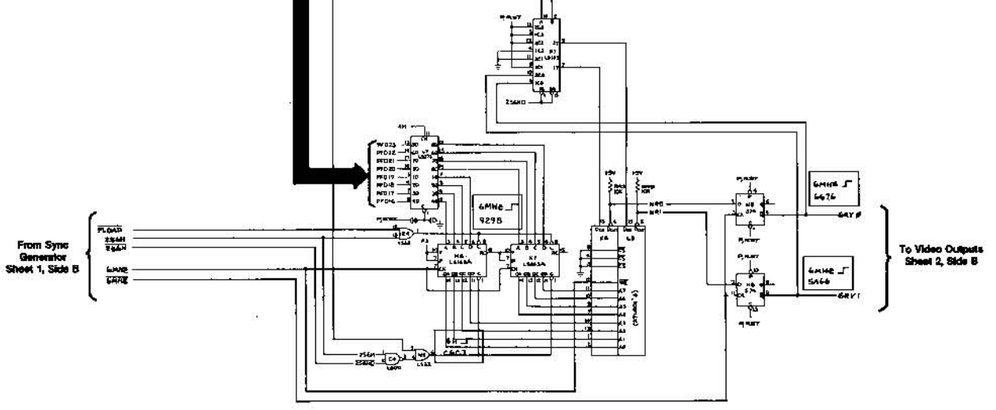
Motion Object Circuitry (Vertical)



The Motion Object Circuitry (vertical) receives playfield data and vertical inputs from the sync generator circuitry to generate the vertical component of the motion object video. PFD8-15 from the playfield memory and 1V-128V from the sync generator are compared at E5 and F5. The output is gated by C5 when a motion object is on one of the eight vertical lines and is latched by D5 to AND gate C7. A low on C7 pin 6 indicates the presence of a motion object on one of the vertical lines during non-active video time. This signal (MATCH) enables the multiplexers in the picture data circuitry.

When 256H on pin 1 of C6 goes high, the sync generator inputs (1V, 2V and 4V) are selected. When 256H goes low, the latched output of D6 is selected. The output of C6 is EXCLUSIVE OR gated at D6 and is sent to the picture data selector circuitry as motion graphic address (MGA0-MGA2). The other input to EXCLUSIVE OR gate D7 is PIC7 from the playfield code multiplexer circuitry. PIC7 when high causes the output of D7 to be complimented. If MGA0 is high, MGA1 is low and MGA2 is high, a high at PIC7 causes MGA1 to be high and MGA2 to be low. This causes the motion object video to be inverted top to bottom.

Motion Object Circuitry (Horizontal)



The motion object circuitry (horizontal) receives playfield data and horizontal inputs from the sync generator circuitry. PFD16-PFD23 from the playfield memory determines the horizontal position of the motion object. This data is latched by L7 and loaded into the horizontal position counters K7 and M8 by a low on pin 9 of K7 and M8. The horizontal position counters then address video RAMs K8 and L8. These RAMs are loaded with the video data for the particular motion object from shift registers D7 and J8 (which were loaded from the graphics ROM). The output for RAMs K8 and L8 is then sent to the color PROM circuitry as MR0 and MR1.

Denotes a signature

ATARI

Sheet 2, Side A

WARLORDS™

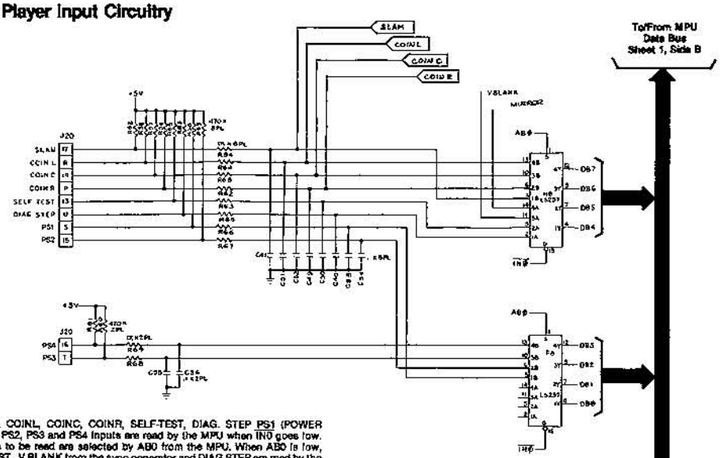
Playfield Address Selector
Playfield Memory
Playfield Multiplexer
Picture Data ROM Circuitry
Motion Object Circuitry

Section of 036434-01 B

A Warner Communications Company

Sheet 2, Side A
09-177-02 1st printing

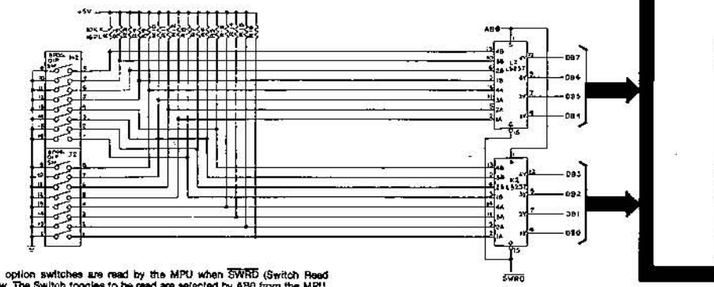
Coin and Player Input Circuitry



SLAM, COINL, COINC, COINR, SELF-TEST, DIAG. STEP PS1 (POWER STONE), PS2, PS3 and PS4 inputs are read by the MPU when IN0 goes low. Switches to be read are selected by AB0 from the MPU. When AB0 is low, SELF-TEST, V BLANK from the sync generator and DIAG STEP are read by the MPU on DB4 and DB5. When AB0 goes high, SLAM, COINL, COINC, COINR, PS1, PS2, PS3 and PS4 are read by the MPU on DB0-DB7.

Denotes a test point

Option Input Circuitry

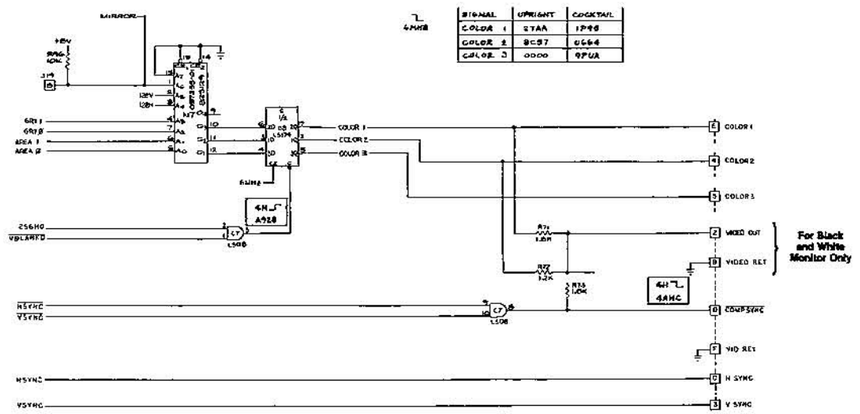


The game option switches are read by the MPU when SWRD (Switch Read Enable) is low. The Switch toggles to be read are selected by AB0 from the MPU. When AB0 is high, switch toggles 9, 10, 11, and 12 on J2 and M2 are read on DB0-DB7. When AB0 is low switch toggles 13, 14, 15 and 16 on J2 and M2 are read on DB0-DB7. Toggle inputs are "on" when pulled to ground.

Video Output

The color PROM circuitry receives playfield (AREA0-AREA1) and motion object (GRY0-GRY2) information and assigns a color or shade of gray (if using a black and white monitor) before it is sent on to the video monitor for display.

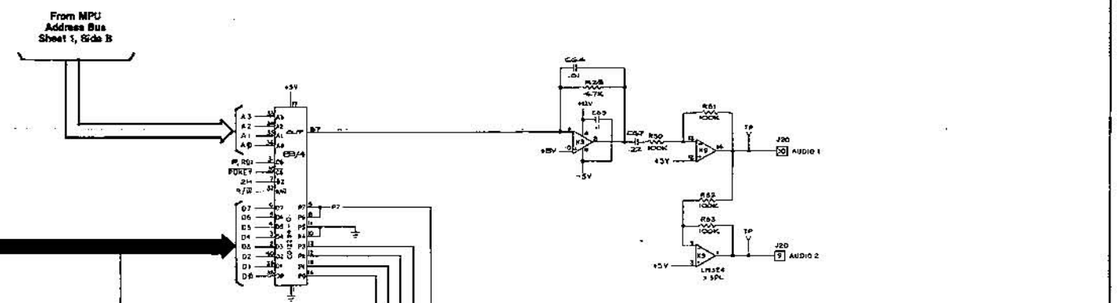
128V and 128H from the sync generator circuit determines in which corner of the monitor the active video is displayed. If 128V is high and 128H is low, the video is in the lower left corner of the monitor.



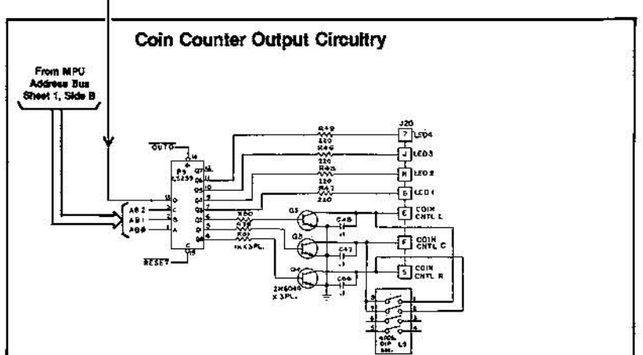
Denotes a signature

Pot Reading and Audio Circuit

The pot reading and audio output circuit receives a voltage from the control panel pots and sends it to the MPU via the custom chip for placement of the "shields" on the monitor. It also generates all the sounds in the Warlords™ game. When P7 of the pot select circuit goes low, an internal counter in the custom audio chip B3/4 begins counting. Also the base of Q7 goes high and Q7 conducts, discharging the voltage across C44. When P7 goes high, Q7 is then cut off and C44 starts to build up a charge via constant current source Q8. When the voltage on C44 is equal to the pot voltage, the comparator associated with the individual pot input changes state disabling the counter inside the custom audio chip B3/4. The MPU then reads the count for each pot input via D0-D3, and moves the "shield" to the spot on the playfield corresponding to that count.



Coin Counter Output Circuitry



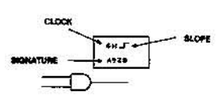
This circuit consists of coin counter drivers Q3, Q4, and Q5 and data latch P9. The circuit is addressed by the MPU on AB0-AB2 and written by the MPU on data line DB7. When the input to a driver is clocked high, its collector goes low grounding the return of the coin counter in the coin door.

Signature Analysis Procedure

1) Remove the following:
   - The electrical power from the Warlords™ game.
   - The game PCB from the cabinet. Attach extender cables between the PCB and the game wiring diagram.
   - The MPU chip at location C2 from the game PCB. Using a thin piece of wire (28 AWG), jumper pin 37 to pin 39 on the MPU socket.

2) Connect the following:
   - The CAT™ Box flex cable to the Warlords™ PCB test edge connector.
   - The three BNC to E-Z clip cables (supplied with the CAT™ Box) to the SIGNATURE ANALYSIS CONTROL START, STOP and CLOCK BNC jacks on the CAT™ Box.
   - The black E-Z clips on the three cables to a ground lug on the PCB.
   - The red E-Z clips on the START and STOP cables to the PCB at L6 pin 2.

3) The red E-Z clip on the clock cable will be moved from 4H to 6MHz and back throughout the actual signature analysis. The clock signal and slope for each signature is located on the schematic sheet above the signature. Note the example below:



4) Position the CAT™ Box switches as follows:
   SIGNATURE ANALYSIS CONTROL
   START: ⌐
   STOP: ⌐
   CLOCK: ⌐
   READ/WRITE CONTROL
   BYTES: 1024
   DBUS: AD0B
   ERROR DATA DISPLAY: GAME
   R/W: WRITE
   R/W MODE: OFF
   TESTER CONTROL
   TESTER MODE: R/W
   TESTER SELF TEST: OFF

In order to obtain reliable signatures from the Warlords™ PCB, the Playfield RAM must be addressed and a specific pattern "written" into the memory.

5) Apply power to the Warlords™ game. Turn the CAT™ Box ON/OFF switch to ON.
6) On the ADDRESS/SIGNATURE keypad enter 0400.
7) Toggle the R/W MODE switch to momentary SINGLE.
8) Set the TESTER CONTROL, TESTER MODE switch to SIG.

   If the signature to be taken is connected to the 6MHz clock (P4 pin 14), the ADDRESS/SIGNATURE will indicate 1F31.

   If the signature to be taken is connected to the 4H clock (P4 pin 11), the ADDRESS/SIGNATURE will indicate C6C3.

   If the ADDRESS/SIGNATURE display is incorrect, press TESTER RESET. If the display is still incorrect, return to step 2 and check the Cat™ Box connections to the game PCB.

9) Connect the data probe supplied with the CAT™ Box to the DATA PROBE, DATA BNC. The data probe has a black alligator clip attached to it. Connect this alligator clip to a ground lug on the PCB.

The Warlords™ game PCB is now set up to provide proper signatures.

ATARI®

Sheet 2, Side B

WARLORDS™

Coin and Player Input Circuitry
Pot Reading and Audio Circuitry
Option Input Circuitry
Coin Counter Output Circuitry
Signature Analysis Procedure

Section of 036434-01 B

A Warner Communications Company

Sheet 2, Side B
DR-177-02 1st printing