

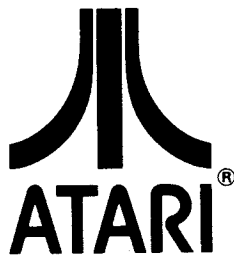
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**Sheet 2, Side A**

# **Centipede™**

**Playfield Address Selector**

**Playfield Memory**

**Playfield Multiplexer**

**Picture Data ROM Circuitry**

**Motion Object Circuitry (Vertical)**

**Motion Object Circuitry (Horizontal)**

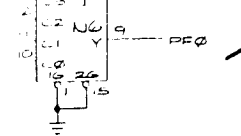
**Section of 037241-01 C +**

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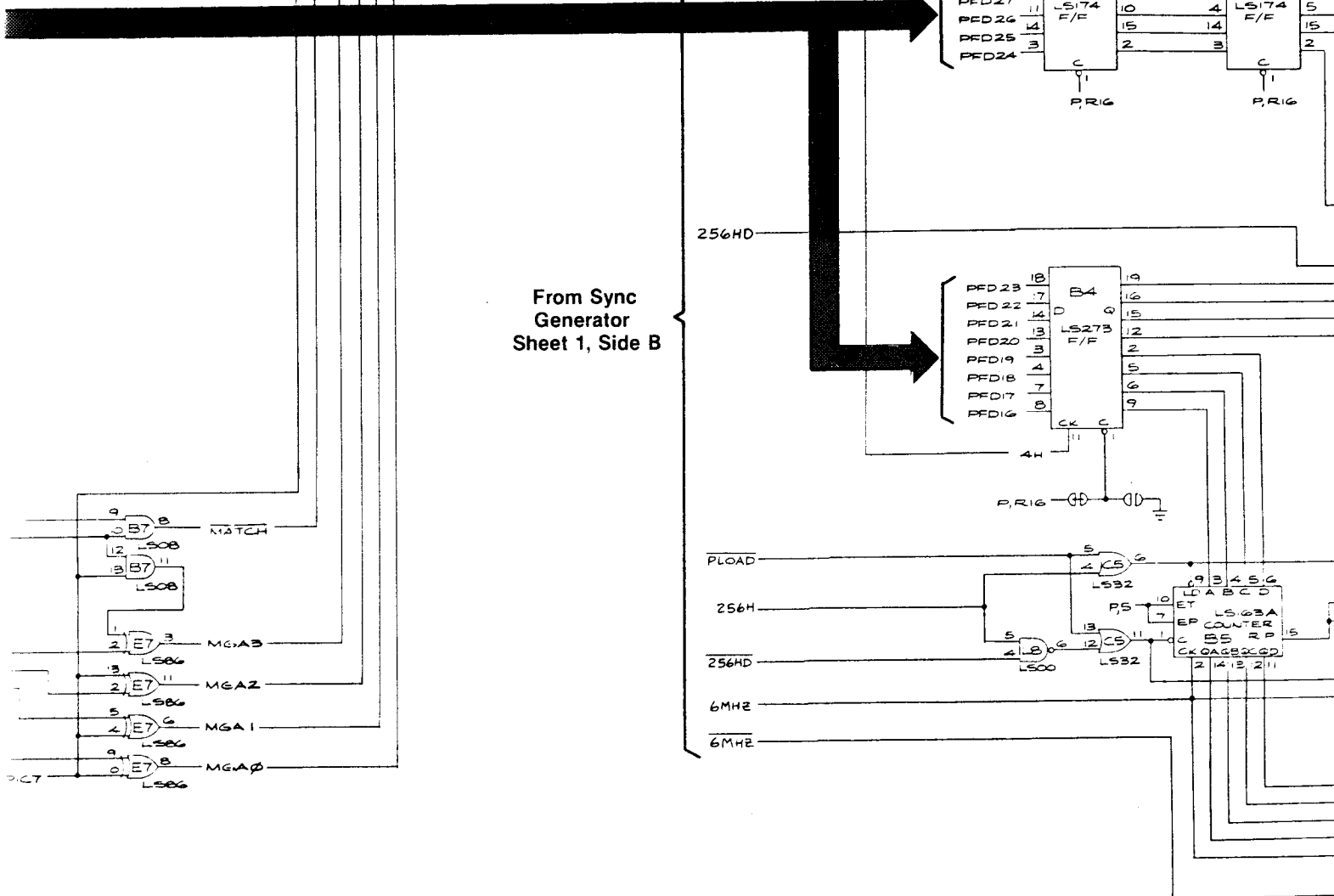


# Motion Object Circuitry (Horizontal)

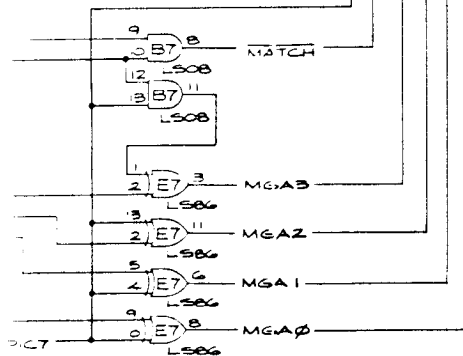
The motion object circuitry (horizontal) receives playfield data and horizontal sync signals from the sync generator circuitry. PFD16-PFD23 from the playfield memory determine the position of the motion object. PFD24-PFD29 from the playfield memory determine the color of the motion object. PFD16-PFD23 are latched by L7 and loaded into the horizontal position counters A5 and B5 by a low on pin 9. The horizontal position counters then output data to RAMs A6 and B6. These RAMs are loaded with the video data for the particular line from shift registers H9 and J9 (which were loaded from the graphics ROM). The data from RAMs A6 and B6 is then sent to the color PROM circuitry as MR0 and MR1.

cal inputs from the motion object video. PFD8-PFD15 are compared at F6 and H6. The outputs of these comparators are used to determine vertical lines and is used to determine a motion object on the screen. This circuitry enables the multi-line motion object.

When 256H goes low, the circuitry is gated at E7 and is inverted (GA0-MGA3). The other logic circuitry. PIC7 GA0-MGA3 are low, so to be inverted top



From Sync Generator Sheet 1, Side B

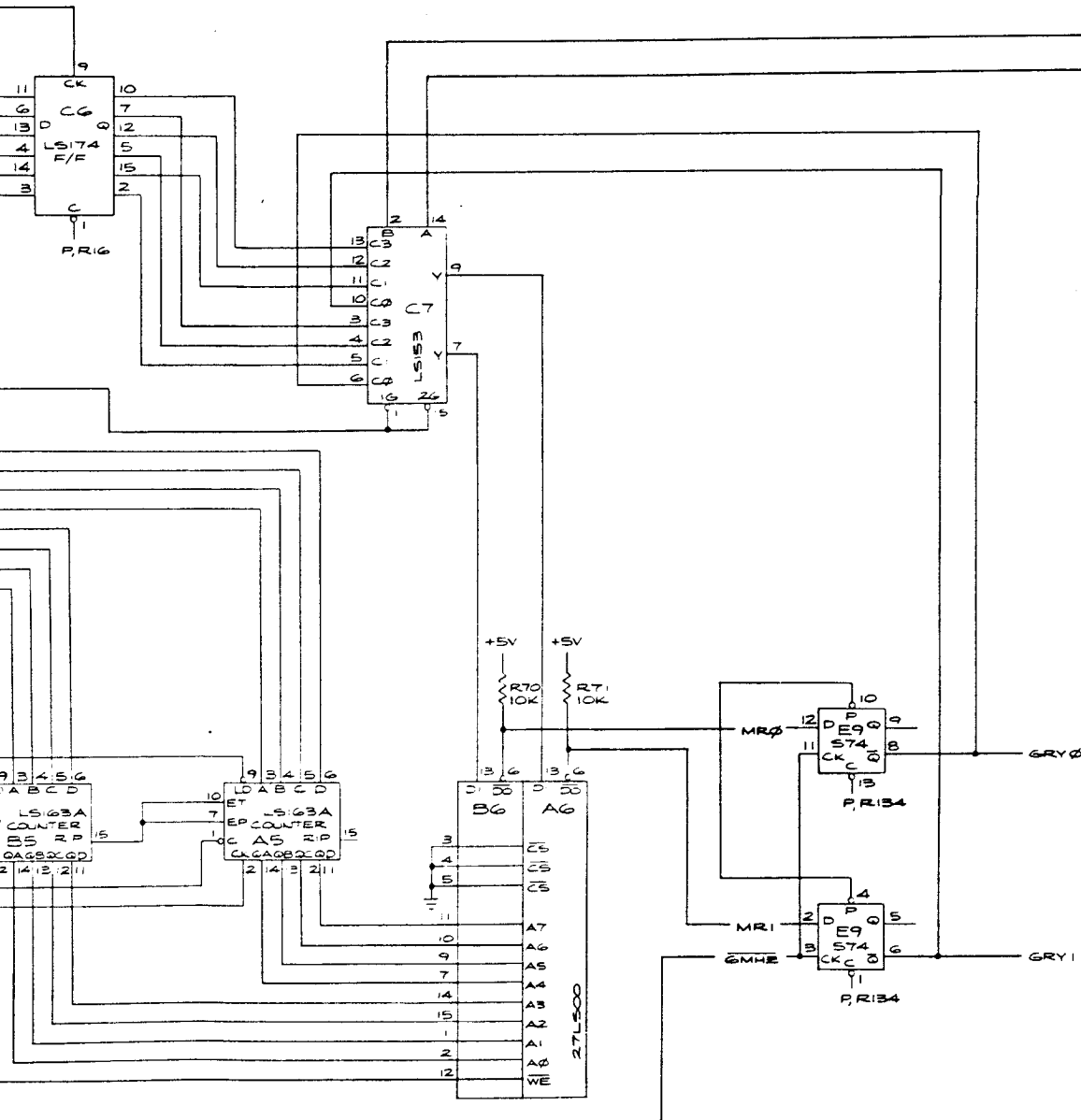


# Horizontal)

...a and horizontal inputs from memory determine the horizontal memory determine the indirect address into the horizontal position counters then address video for the particular motion object (graphics ROM). The output for MR0 and MR1.

playfield code multiplexer, MGA0-MGA3 (motion graphics address) from the motion object circuitry, 256H and 256H from the sync generator. PIC0-PIC5 represent the code for the object to be displayed. MGA0-MGA3 set one of eight different combinations of the 8-line by 8-bit blocks of picture video or the 16 line by 8 bit blocks of motion object video.

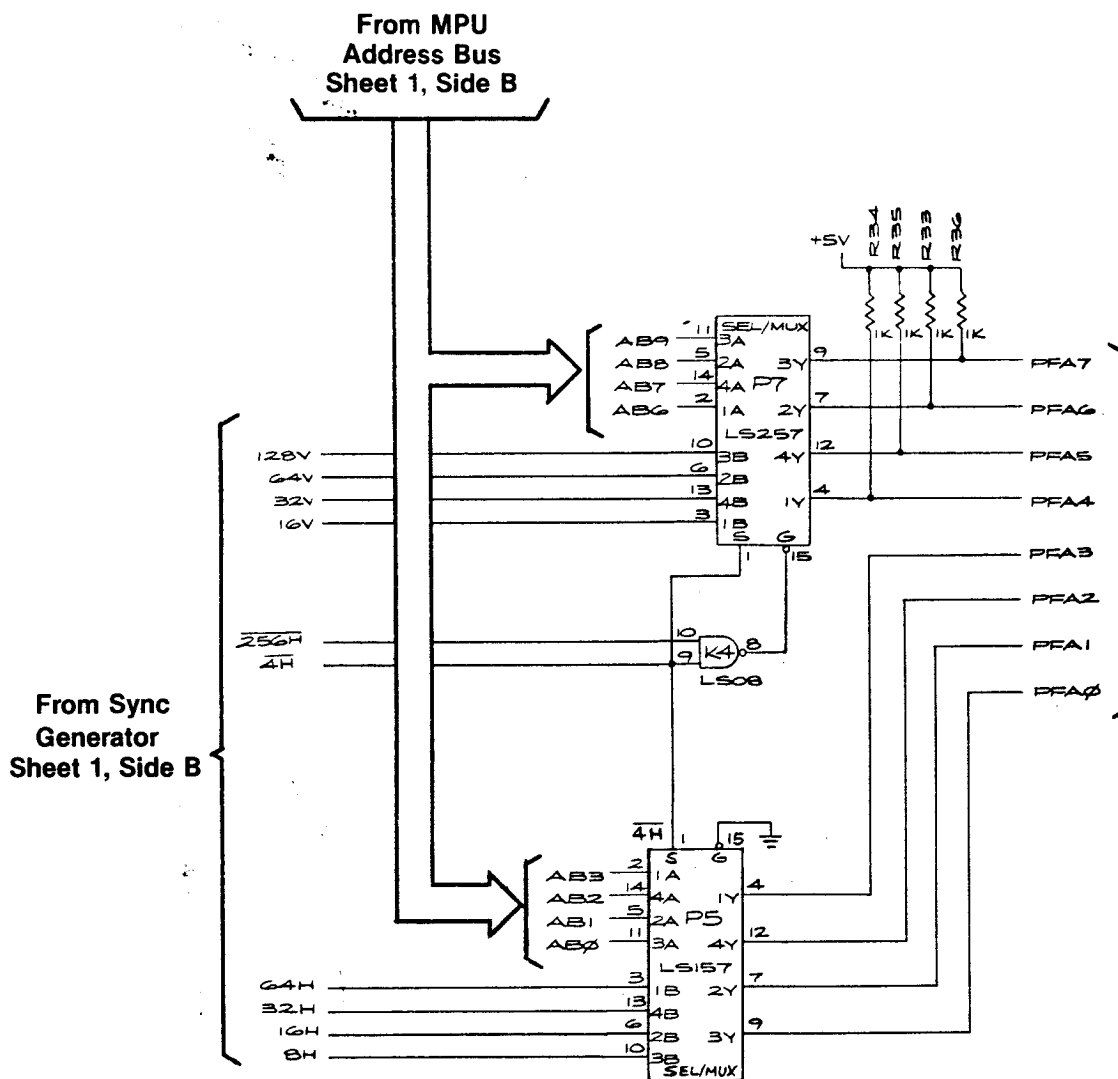
256H when high selects the playfield picture color codes to be addressed. 256H when low selects the motion object color codes to be addressed. The picture data ROM output D1-D8 on F7 and H/J7 are multiplexed by F8, H8, J8 and K8 and shifted out serially at H9 and J9. This serial output is latched by F9 as AREA0 and AREA1 to the motion object horizontal circuitry and the video output circuit.



# Centipede PL

## Testing the P

1. Perform the CAT E
2. Set the CAT Box s
  - a. Press TESTER I
  - b. DBUS SOURCE
  - c. BYTES to 1024
  - d. R/W MODE to (
  - e. R/W to WRITE
  - f. Key in 0400
  - g. Set R/W MODE
  - h. R/W to READ
  - i. Set R/W MODE



## Playfield Address Selector

The Playfield Address Selector controls the access to the playfield memory. It allows either the game MPU or the sync generator to scan the playfield memory. The Playfield Address Selector consists of multiplexers P5, and P7 and gate K4.

When  $\overline{4H}$  on pin 1 of P5 and P7 is low and pin 15 on P7 is low, the Playfield Address Selector receives 8H, 16H, 32H, and 64H on P5 and 16V, 32V, 64V, and 128V on P7 from the sync generator. These signals enable the sync generator circuits to access the playfield memory.

When  $\overline{4H}$  goes high the game MPU addresses the playfield memory (via AB0-AB9) for the positioning of the graphics. During horizontal blanking (pin 15 of P7 is high) the outputs of P7 (PFA4-PFA7) are held high enabling the motion object circuitry to access the playfield memory for the motion objects to be displayed.

# Code Playfield RAM

## the Playfield RAM

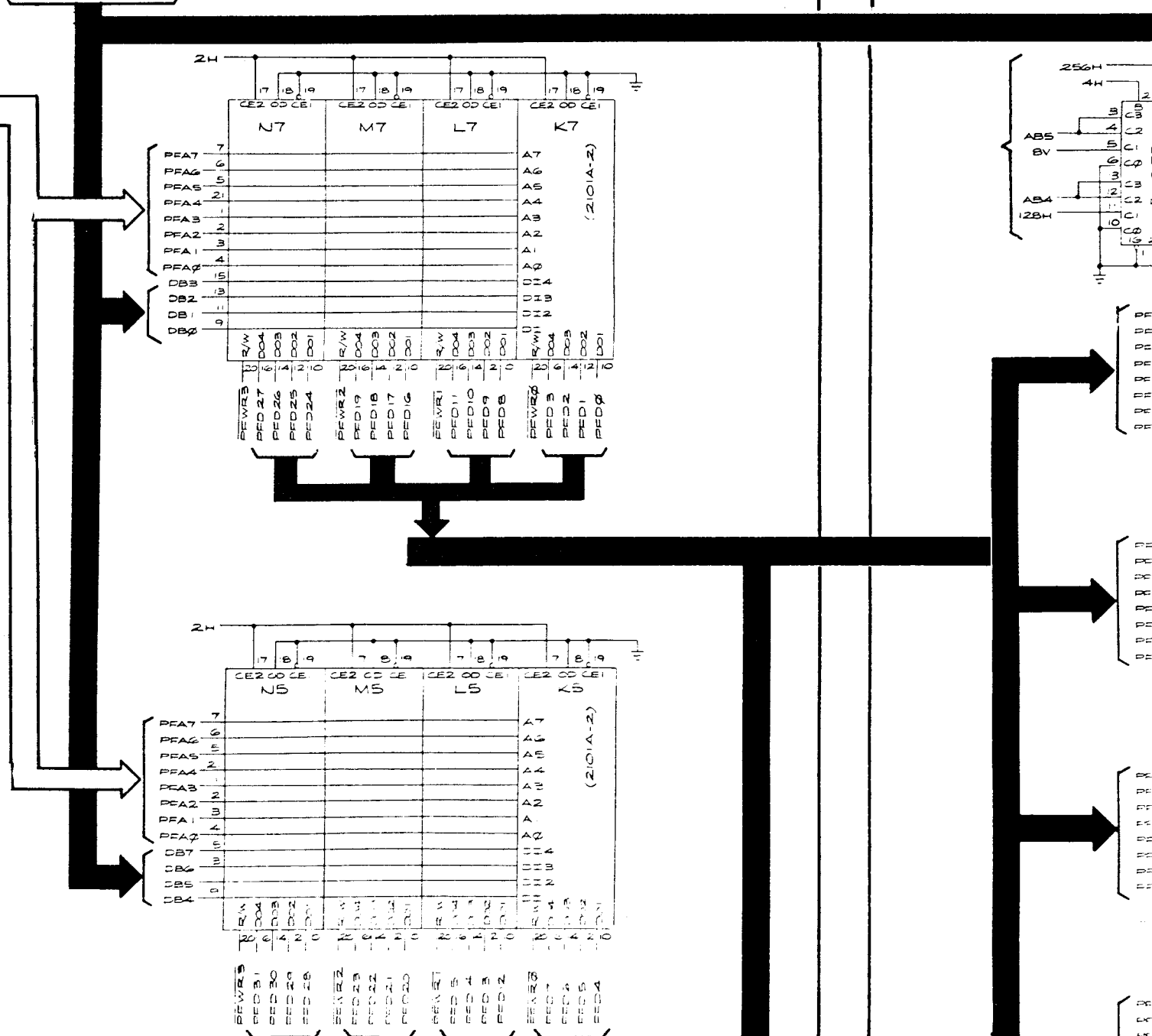
the CAT Box preliminary set-up.

CAT Box switches as follows:

- TESTER RESET
- SOURCE TO ADDR
- S to 1024
- MODE to (OFF)
- WRITE
- 0400
- W MODE to PULSE, then to OFF.
- READ
- W MODE to PULSE, then to OFF.

3. If the CAT Box reads an address that doesn't compare, the COMPARE ERROR LED lights, the ADDRESS/SIGNATURE display shows the failing address location, and the ERROR DATA DISPLAY switch is enabled.
4. If the COMPARE ERROR LED does not light, rekey 0400 and repeat the test with the DBUS SOURCE switch set to ADDR. This ensures that the data bits at address 0400 will go high. If the COMPARE ERROR LED does not light after this step, the Playfield RAM is good.

To/From MPU  
Data Bus  
Sheet 1, Side B



The PL  
(PF0-PF  
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consists

When 2  
selected  
as select  
playfield  
is low, th  
These sig  
M6, and

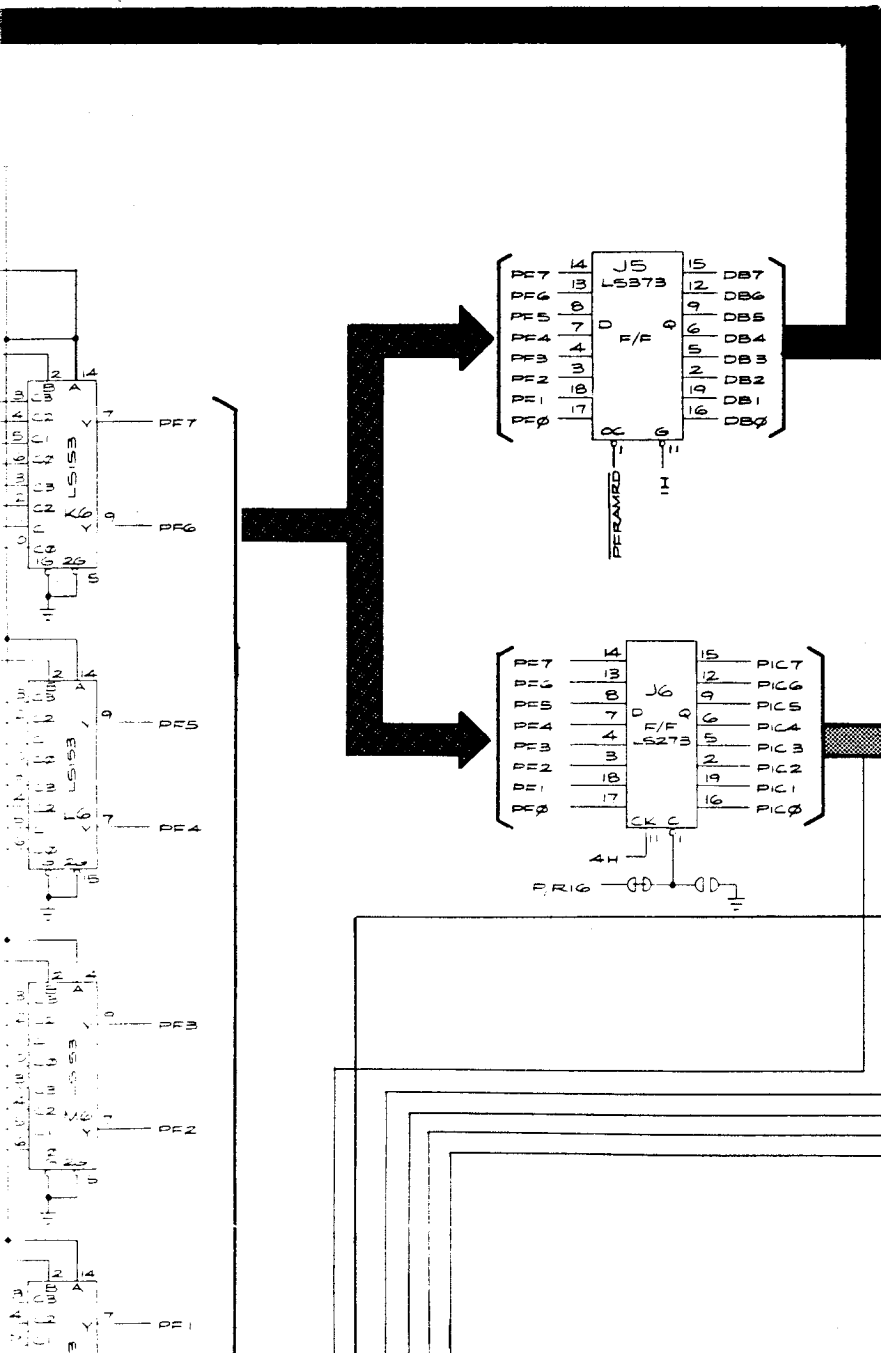
The pl  
and to th  
sync gen  
DB0-DB7  
picture d

# Playfield Multiplexer

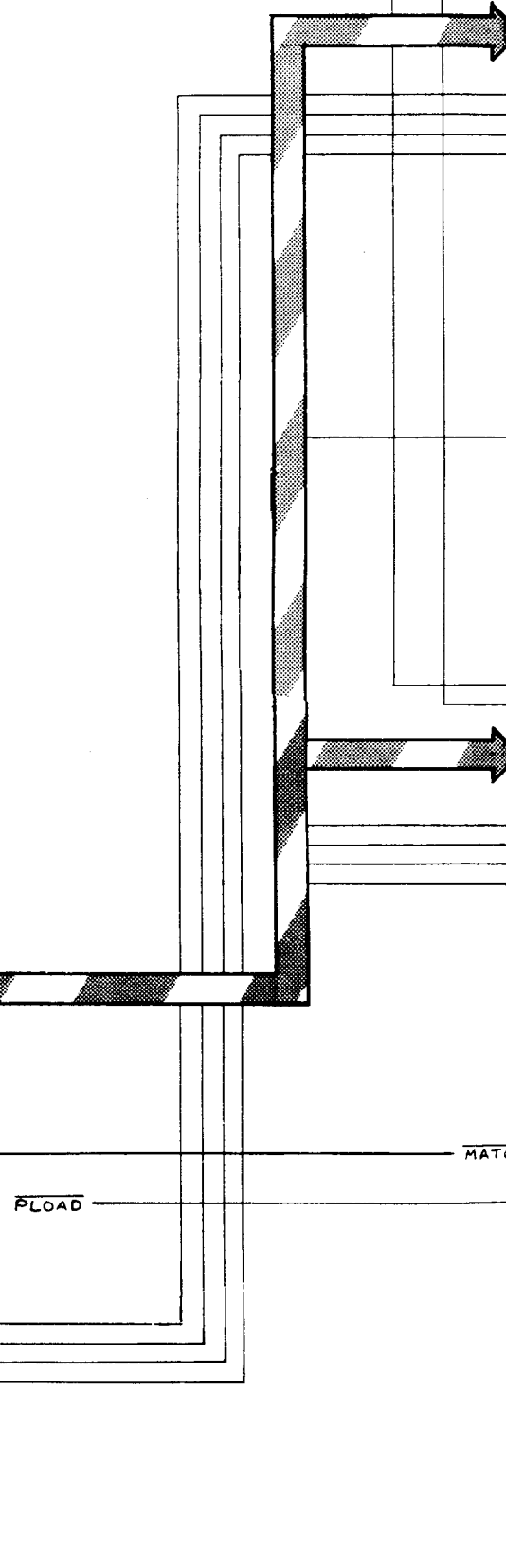
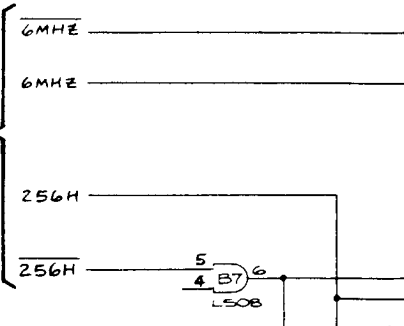
The Multiplexer receives playfield data from the playfield memory and the output (PF0-PF7) is a code that determines what is 1) displayed on the monitor, or 2) read or updated by the MPU. The Playfield Multiplexer consists of eight multiplexers K6, L6, M6, N6 and P6.

When 4H is low and 4H is high, AB4 and AB5 from the MPU address bus is the select signal from P6. This output is applied to multiplexers K6, L6, M6, and N6. When the MPU is accessing the playfield code multiplexer, the output is either being read or updated by the MPU. When 256H is high and 4H is low, the outputs from the sync generator (128H and 8V) are the selected outputs. When 256H is high and 4H is high, the outputs from the sync generator (128H and 8V) are the selected outputs. When 256H is high and 4H is low, the outputs from the sync generator (128H and 8V) are the selected outputs.

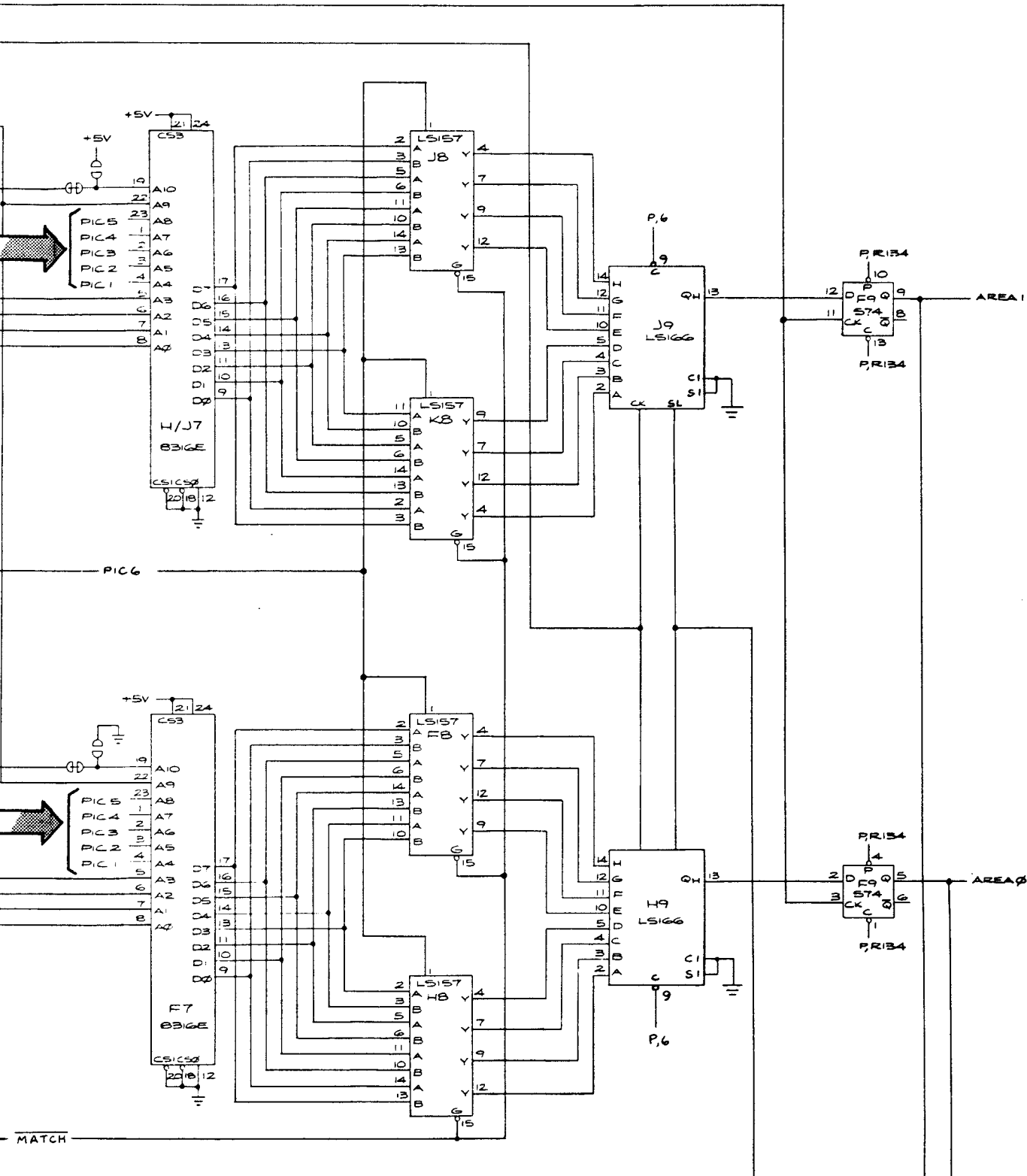
When 256H is high and 4H is high, the outputs from the sync generator (128H and 8V) are the selected outputs. When 256H is high and 4H is low, the outputs from the sync generator (128H and 8V) are the selected outputs. When 256H is high and 4H is high, the outputs from the sync generator (128H and 8V) are the selected outputs.



From Sync Generator Sheet 1, Side B







## Picture Data ROM Circuitry

The picture data ROM circuitry receives picture information, assigns a color code to the information and sends it to the color PROM circuitry. The picture data ROM circuitry consists of ROM devices F7 and H/J7, multiplexers F8, H8, J8, K8, shift registers H9 and J9, and latch F9.