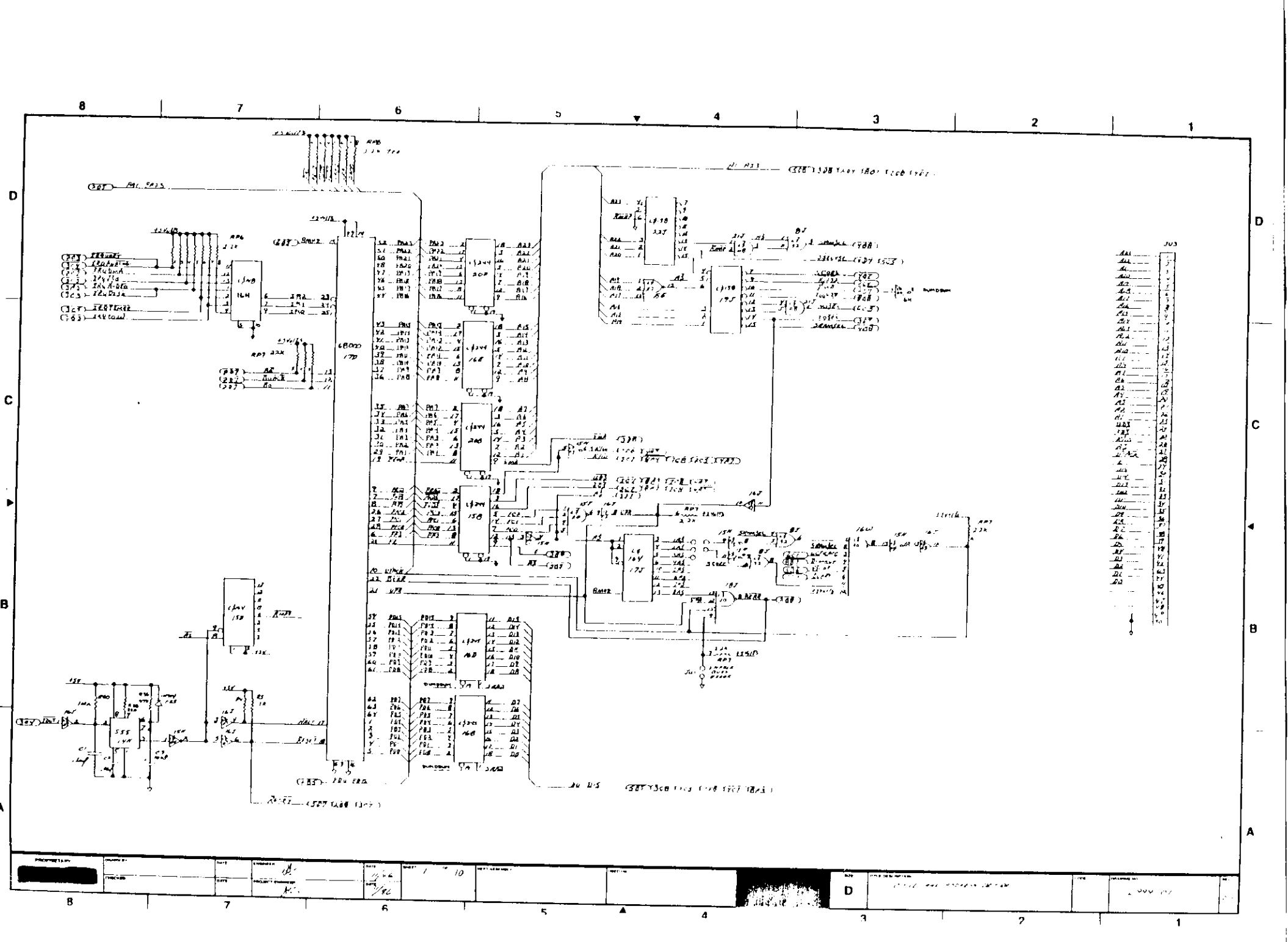
MILLENNIUM
GAMES PRODUCTS
A Subsidiary of Malibu Grand Prix Corp.

CPU AND ADDRESS DECODING LOGIC SCHEMATIC PAGE 1 of 10

Schematic Grid Location	Board Location	Function
D7	16H	Interrupt priority encoder
C6	17D	CPU
C5,D5	20P,16E,20B	Address line buffers
B5	15B	Control line buffer
B5	16D,16B	Data line buffers
A8	14H	Power on reset ckt
B7	15D	Power on reset remap of ROM
-	-	memory space to pick up stack
-	-	pointer and reset vector
B4	17J	DTACK delay circuit
B3	16W	DTACK combination circuit

This page contains the heart of the game system. The CPU implemented in this system is the MC68000 (17D). The CPU address lines are buffered by three (3) 74LS244s (20P,16E,20B), and then distributed throughout the main logic pcb. System address decoding is performed by two (2) 74LS138s (22J,19J), and these enable signals are used by each major system on the board to control the transfer of data. Data line buffering is the function of the two (2) 74LS245 (16B,16D). CPU control line buffering is performed by the 74LS244 (15B). Power on reset is accomplished by the NE555 (14H) and the 74LS164 (15D). CPU interrupts are applied to the processor through a priority encoder 74LS148 (16H). The circuitry of the 74LS164 (17J), 74LS30 (16W), and 74LS20 (18J) provide the necessary signals to accept DTACK responses from each major system on the board and to generate buss error conditions encountered by the CPU. JU3 is an expansion connector, which is not used in this implementation of the game system. This connector is for future expansion.

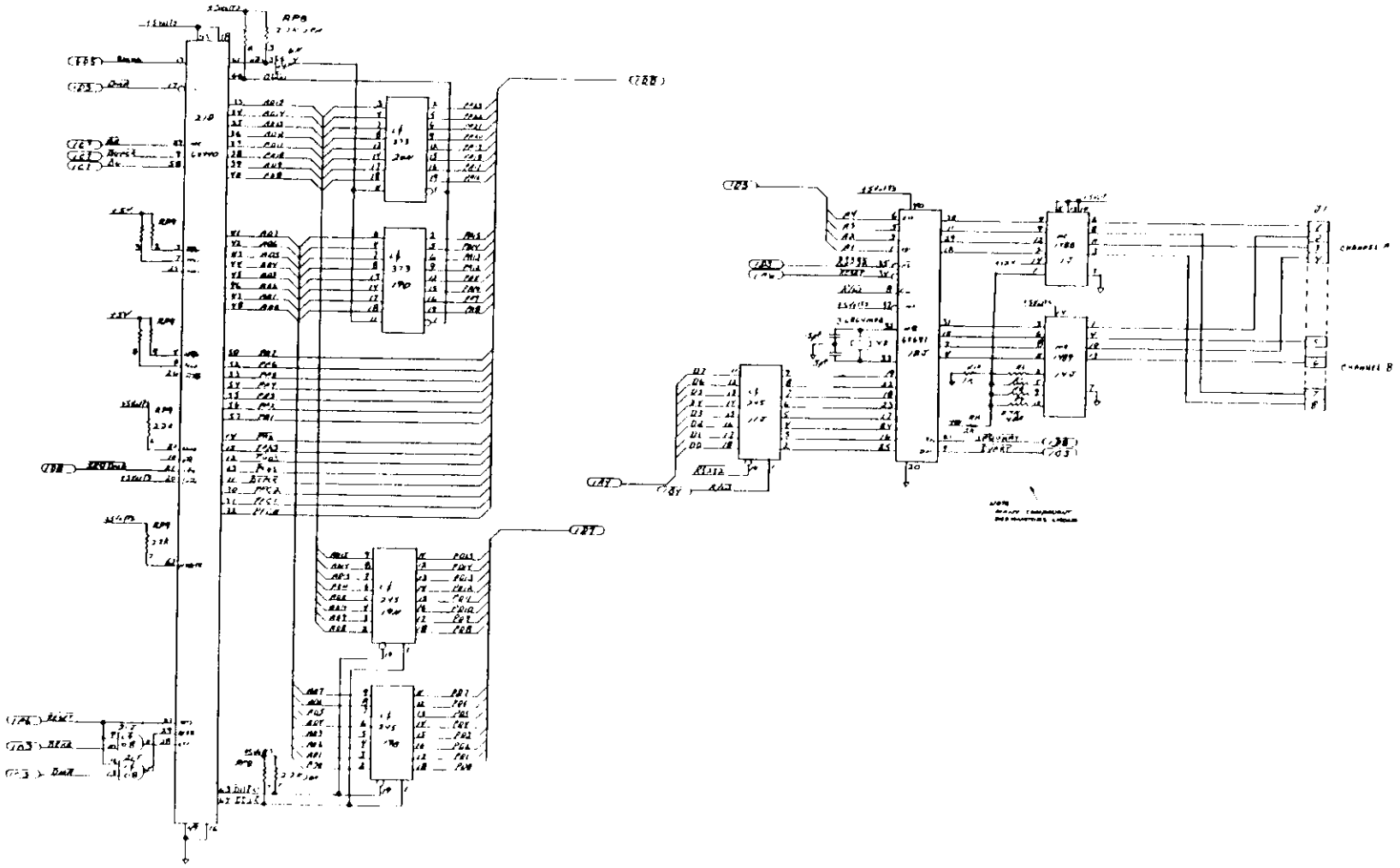


DMA AND SERIAL I/O SCHEMATIC PAGE 2 of 10

Schematic Grid Location	Board Location	Function
C7	21D	DMA device
D6	20H	Address line buffer for DMA
C6	19D	Address line buffer for DMA
B6	19H	Data line buffer for DMA
B6	19B	Data line buffer for DMA
C4	11J (opt.)	Data line buffer for serial
C4	12J (opt.)	2 channel serial driver
C3	1J (opt.)	TTL to RS232 driver
C3	14J (opt.)	RS232 to TTL driver

Memory to memory transfers are performed by the Direct Memory Access device MC68440 (21D). This DMA device is programmed by the CPU to move data from ROM to other parts of the system.

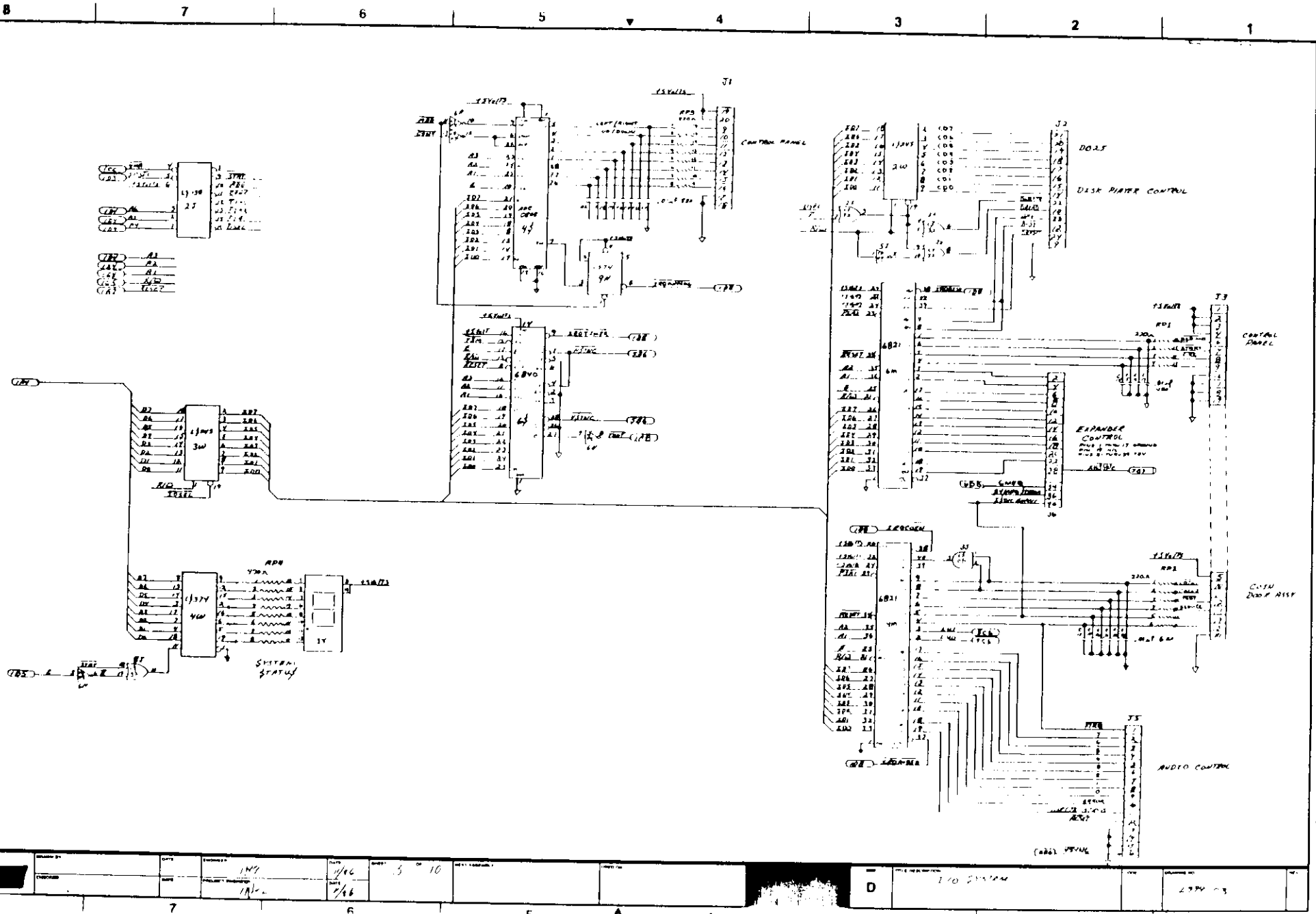
Designed for future applications, a two channel serial input and output device, the MC68681 (12J) is included in the system. The components required for this function were intentionally not installed into this pcb.



I/O SYSTEM SCHEMATIC PAGE 3 of 10

Schematic Grid Location	Board Location	Function
D7	2J	I/O address decoder
C7	3W	I/O data line buffer
B7	4W	System status output driver
B6		Error code display
D5	4S	Analog to digital converter
C5	9H	Interrupt driver for converter
C5	6S	3 channel timer
D3	2W	Video disk data line buffer
C3	6M	Disk,control panel, Expander I/O
B3	4M	Coin door and Audio I/O

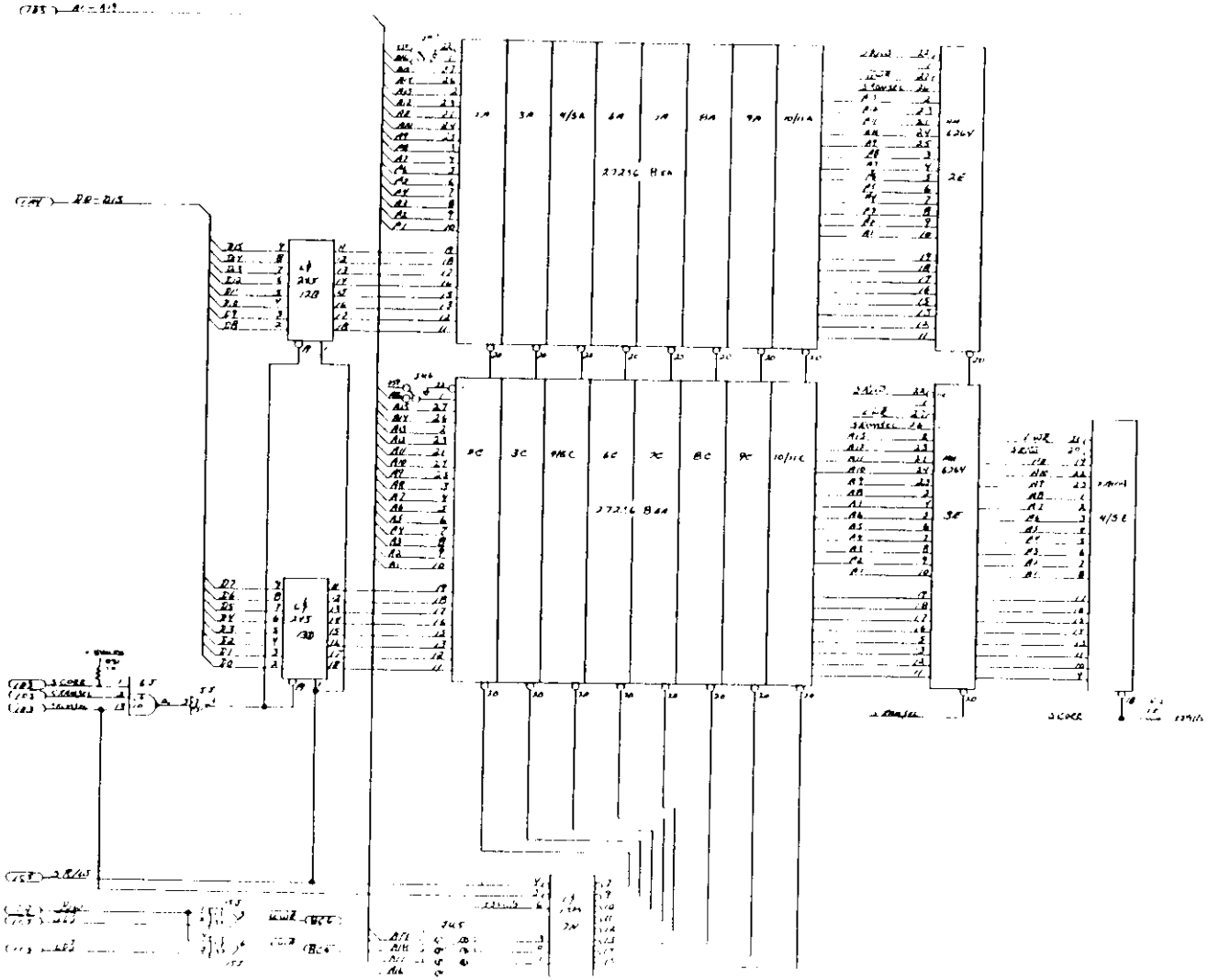
The Address lines are decoded by the 74LS138 (2J), and device enables are generated to select each device on this page of the system diagram. The analog to digital converter ADC0808 (4S) converts the movement of the joystick to digital signals. The two inputs presently being used are pins 9 and 10 of connector J1. This device generates interrupts to the CPU through the 74LS74 (9H) when a conversion is complete. The video disk interface circuitry through connector J2, performs all command and communication with the video disk. Connector J3 connects the control panel and coin door to the system. These signals are conditioned by passive components and are applied to the two MC6821s (6M)(4M). The interface between the video expander and the main logic pcb is accomplished through the MC6821 (6M). This interface controls the operation of the expander. Expander enable is generated from pin 19 of the MC6821 while the other pins control the display start position of the expanded line. Several other signals are required to interface the expander pcb. These are timing and enable signals. Communication and control of the audio pcb is accomplished through connector J5.


8
7
6
5
4
3
2
1
A
B
C
D
CONTROL PANEL
DOOR
DISK DRIVER CONTROL
EXPANDER CONTROL
CONTROL PANEL
SYSTEM STATUS
AUDIO CONTROL
I/O SYSTEM

ROM, RAM, AND CORE SCHEMATIC PAGE 4 of 10

Schematic Grid Location	Board Location	Function
C6	12B	Data line buffer to ROM
B6	13D	Data line buffer to ROM
D5,D4	2A,3A,4A,6A,7A,8A,9A,10A	Program and Data ROM
C5,C4	2C,3C,4C,6C,7C,8C,9C,10C	Program and Data ROM
D3	2E	System RAM
C3	3E	System RAM
C3	5E	Electrical Erasable ROM
A5	7H	ROM address decoder
A7	15J	Write control to system RAM
B7	6J	ROM data buss unable decoder

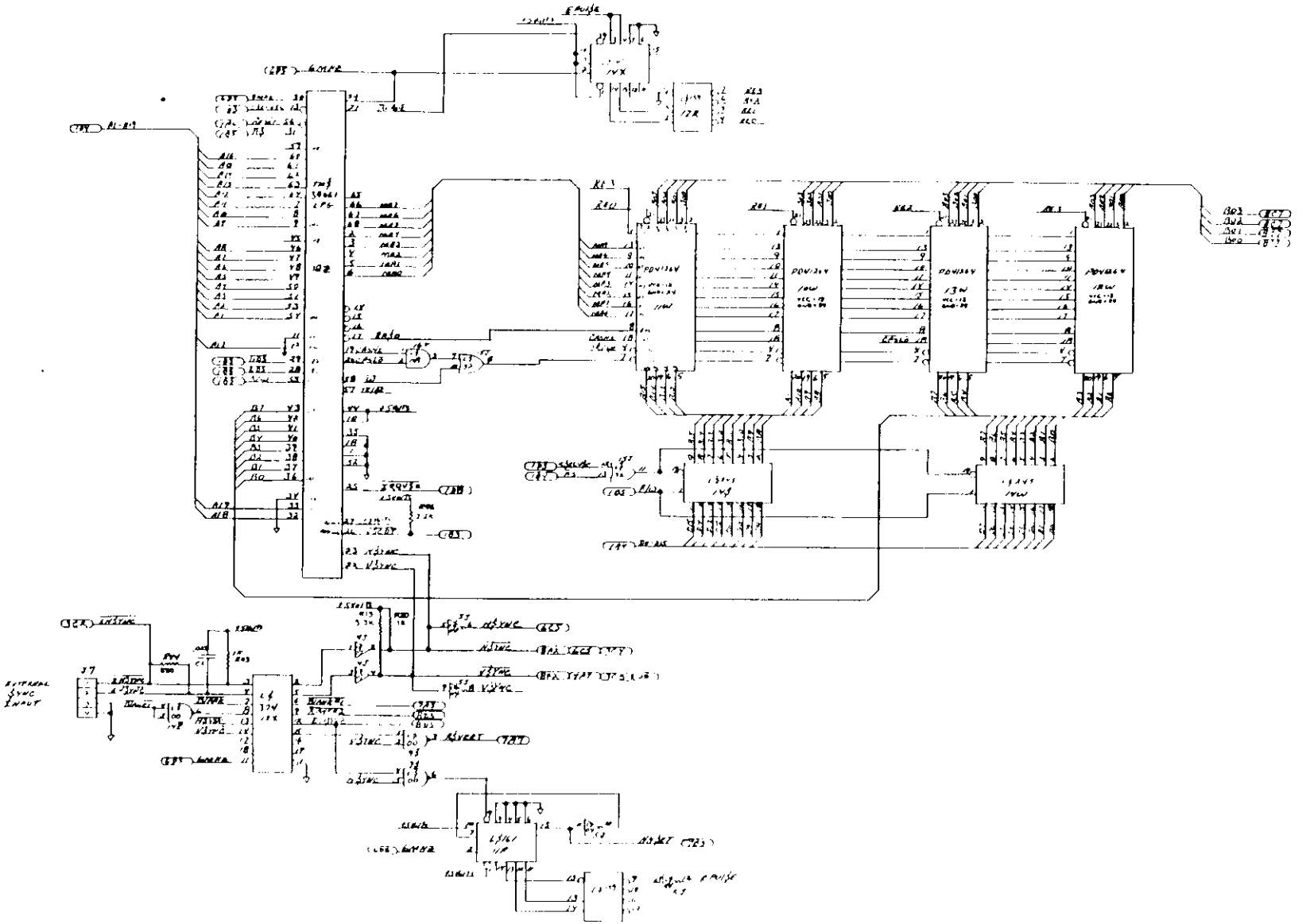
The system ROM and RAM are contained on this page of the system diagram. The address decoding for the selection of individual components are accomplished by the 74LS138 (7H). Selection jumpers JU7, JU6, and JU5 are used if 27512 Eproms are installed into the system.



BACKGROUND VIDEO GENERATOR SCHEMATIC PAGE 5 of 10

Schematic Grid Location	Board Location	Function
C6	12Z	Video Controller Device
D5	14X	Video RAM Counter
D4	12R	Video RAM decoder
C5,C4,C3,C2	11W,10W,13W,12W	Video RAM
C4	14S	Video data line buffer
C3	14W	Video data line buffer
B6	15X	External sync buffer
A5	11R	Horz line resync counter
A5	12R	Resync decoder

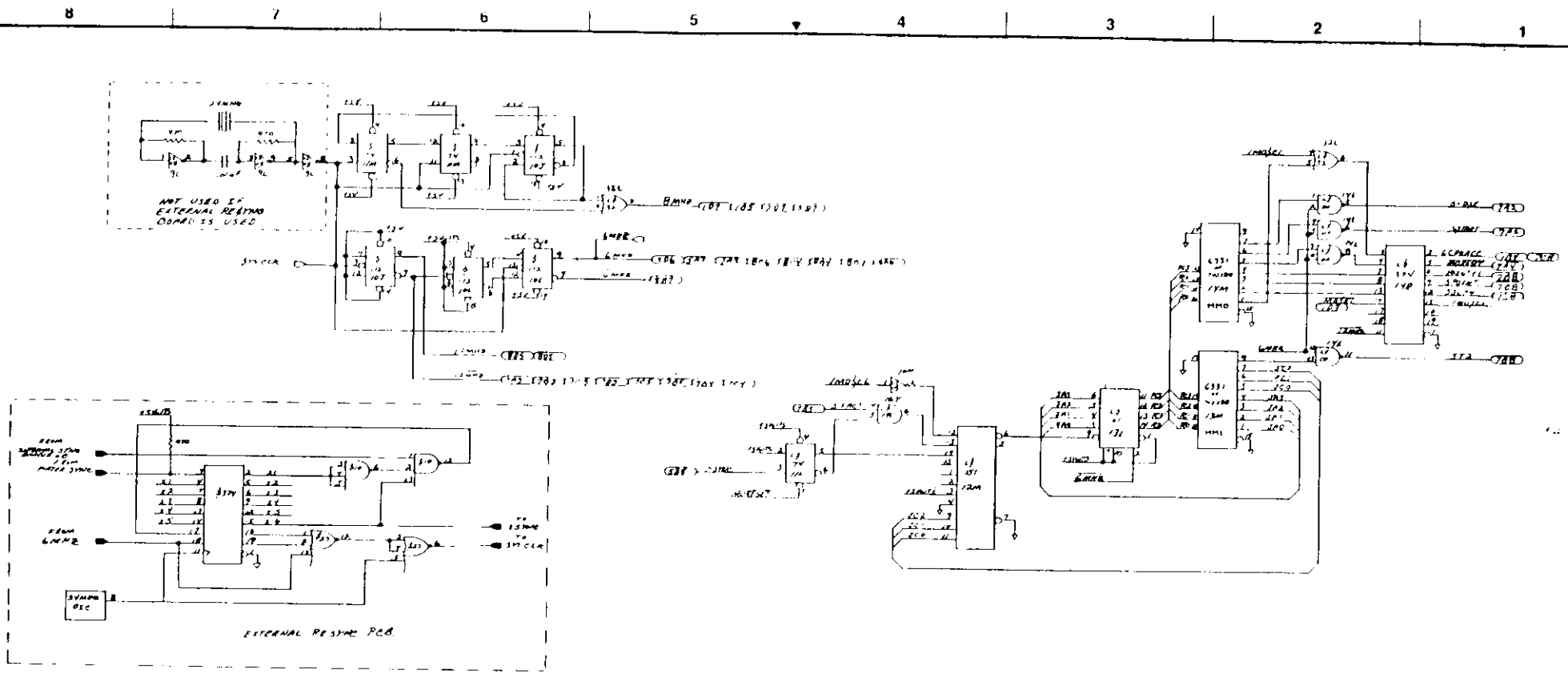
The background digital video is comprised of the TMS32061 (12Z). This device controls the video display and dynamic memory PD41264s (11W,10W,13W,12W). External synchronization is accomplished through the circuitry of the 74LS374 (15X).



CLOCK AND MICROCODE SCHEMATIC PAGE 6 of 10

Schematic Grid Location	Board Location	Function
D7	9L (opt.)	Internal clock generator
D6	11M,11M,10J	Divide by 3 ckt
C6	10J,10L,10L	Divide by 2 and divide by 2
C7,C6	external pcb	Resync logic to disk pcb
C4	12M	Microcode jump select
C3	13L	Microcode program counter
C3	14M,13M	Microcode program PROM
C1	14R	Microcode control driver

The generation of the various clocks required for the system are accomplished through the circuitry of 11M, 10J, and 10L. The input clock to this circuitry can be internally generated or externally generated - as it is with a disk player. The control of the dynamic digital moving objects is through the microcode sequencer, composed of 11L,12M,13L,14M,13M,12L, and 14R. This sequencer controls the addressing and enabling of data transfers of the circuitry, on page 7.


NOT USED IF EXTERNAL RESYNC CIRCUITS USED
EXTERNAL RESYNC PCB

HIGH SPEED OBJECTS SCHEMATIC PAGE 7 of 10

Schematic Grid Location	Board Location	Function
C8	22M	R/W control to object RAM
D7	13R	CPU address controlled driver
C7	21R	CPU address controlled driver
C7	15M	Next object address counter
B7	20M	Object address pointer reg
B7	20S	Object address pointer reg
D6,C6,B6	18S,18M,19M,19S	Object list and data RAMs
A6	21S	Vert line counter for active
A6	21W,20W	Adder for active line select
B5	22S	Active Object this line cont
D6,C6,B6	16S,17S,16M,17M	Object data line buffers
D5,C5,B5	15K,17L,19L,21L	Object image data buffers
D5,C5,B5	16L,18L,20L,22L	Object image shift reg
D4	18W,20S	Object Horz position reg
C4	22X	Odd line serial image buffer
B4	22X	Even line serial image buffer
D3	17Z,18Z,19Z	Object odd line horz position
C3	17Y,18Y,19Y	Object even line horz position
D2	20Z	Object odd line RAM
B2	20Y	Object even line RAM
C2	21Y	Active line output multiplexer
B2	20J	Odd and even line control
A2	16Z	Object load and shift control
A3	21Z	Odd even line control flip flop

The RAMs 6264(18S,18M,19M,19S) are the central point of the digital moving object system. The CPU and/or DMA device can access this RAM to read, write, and modify the data. The RAM is logically set up into different parts, which are: 1. Moving object display list 2. Moving object display data. The moving object display list defines the x/y location for the object and a pointer to the address within the RAM where the definition of the object is found. The microcode sequencer on page 6, controls the operation and tranfers of data within this page. The overall sequence of operation is as follows:

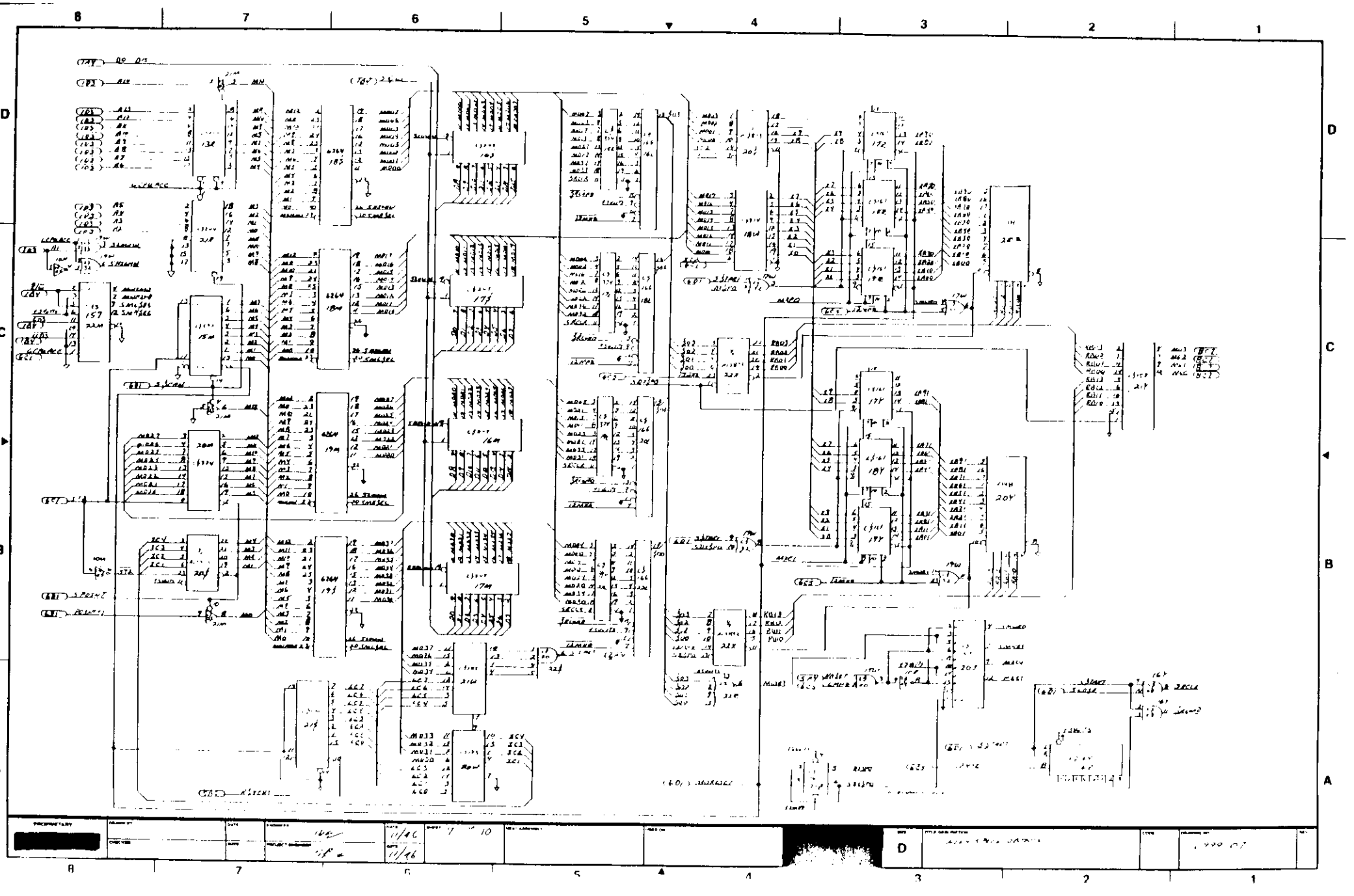
1. The display list is scanned sequentially by counter 15M. If, by a comparison of the current diplay line and the y position of the object (21S,21W,20W) it is found that the object should be visible (22S), then the line number of the object that is to be displayed, is stored in 20S. At the same time, the base address of the object is stored in 20M. Therefore, at this point in the sequence it has been determined that an object should be displayed, and its address is stored in registers.

2. The line number to be displayed of the object is added to the base address of the object, which forms an address to the RAM from where the data is to be retrieved. Data is retrieved in four 8 bit bytes which are the first, or left side, of the 16X16 object and are stored in registers 15K,17L,19L, and 21L.

3. The right side of the object is now addressed by adding a logic 1 to the previous address (20M,20S). This data is now stored in registers 15K,17L,19L, and 21L as in the previous step, but the data that was stored in these registers is transfered to the serial shift registers 16L,18L,20L, and 22L.

4. The object data is converted from parallel to serial and is applied to either the odd or even line buffer RAM (20Z or 20Y). This odd and even line buffer allows one line to be written to, while the other line is read from, resulting in a high speed buffer system. The address, the data is written into, is derived from the horizontal position registors 17Z,18Z,19Z and 17Y,18Y,19Y. Once the first eight pixels of four bits each is shifted into the RAM, the next or right side data, is transferred to the shift registers and the operation continues.

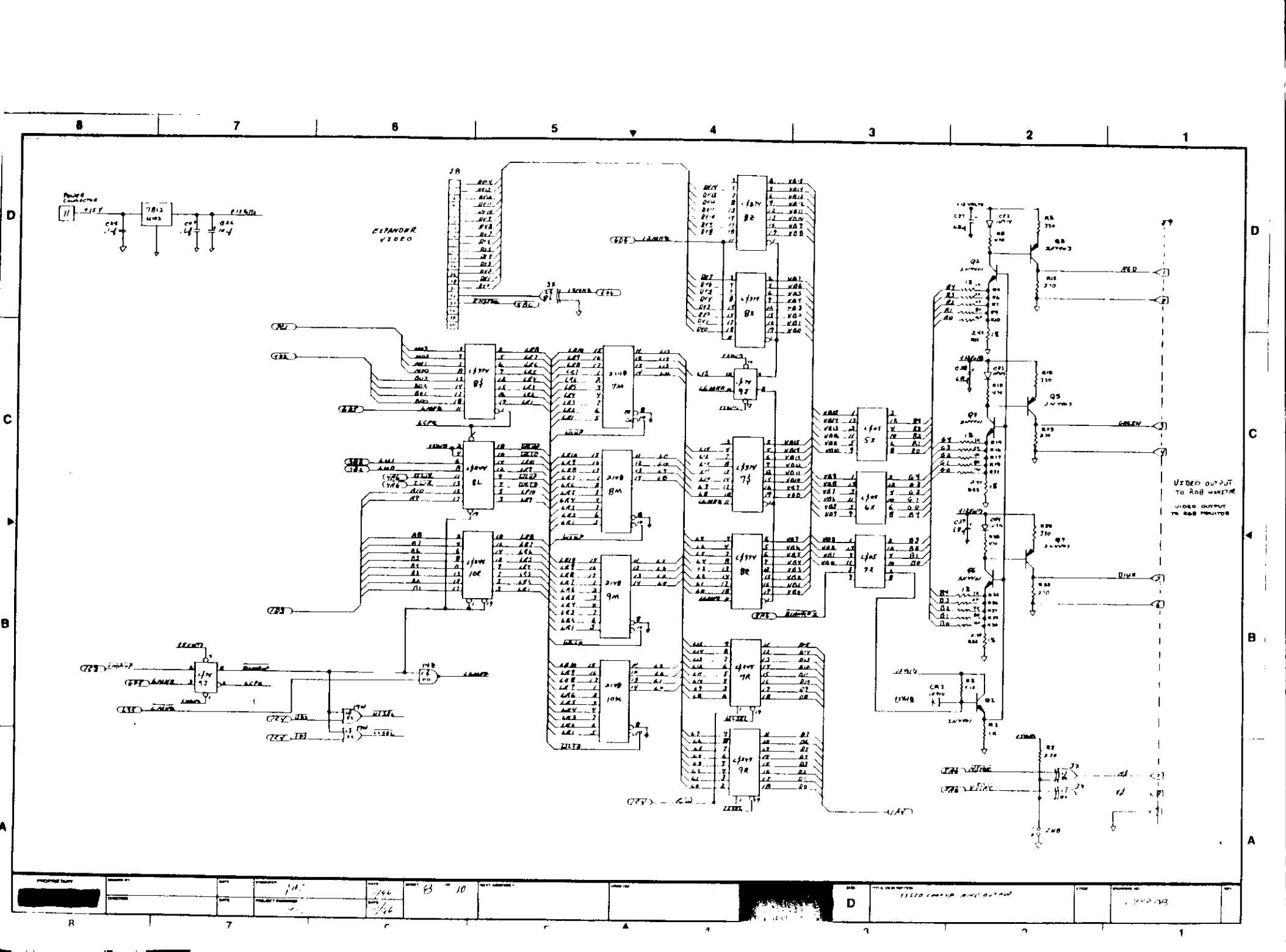
5. When the shift is complete for the right side data, the microcode accesses the RAM for the next entry in the display list. If an entry is not to be displayed, that entry is skipped and the operation continues to the next entry.



VIDEO LOOKUP AND OUTPUT SCHEMATIC PAGE 8 of 10

Schematic Grid Location	Board Location	Function
D7		+12 volt power for video out
B7	9J	Lookup table access control
C5	8S	Serial Video combiner buffer
C5	8L	Lookup R/W control multiplexer
B5	10R	Lookup address buffer
C5,B5	7M,8M,9M,10M	Lookup table RAM
D4	8Z,8X	Digital video input from disk
C4	9J	Digital video enable
C4,D4	7S,7R	Internal digital video buffer
B4,A4	7R,9R	Lookup table data line buffer
B3,C3	5X,6X,7X	Digital video level converter
D2	Q2,Q1	Red digital to analog driver
C2	Q4,Q3	Green digital to analog driver
B2	Q6,Q5	Blue digital to analog driver
B2	Q7	D to A bias and blanking
A2	3X	Sync output Polarity

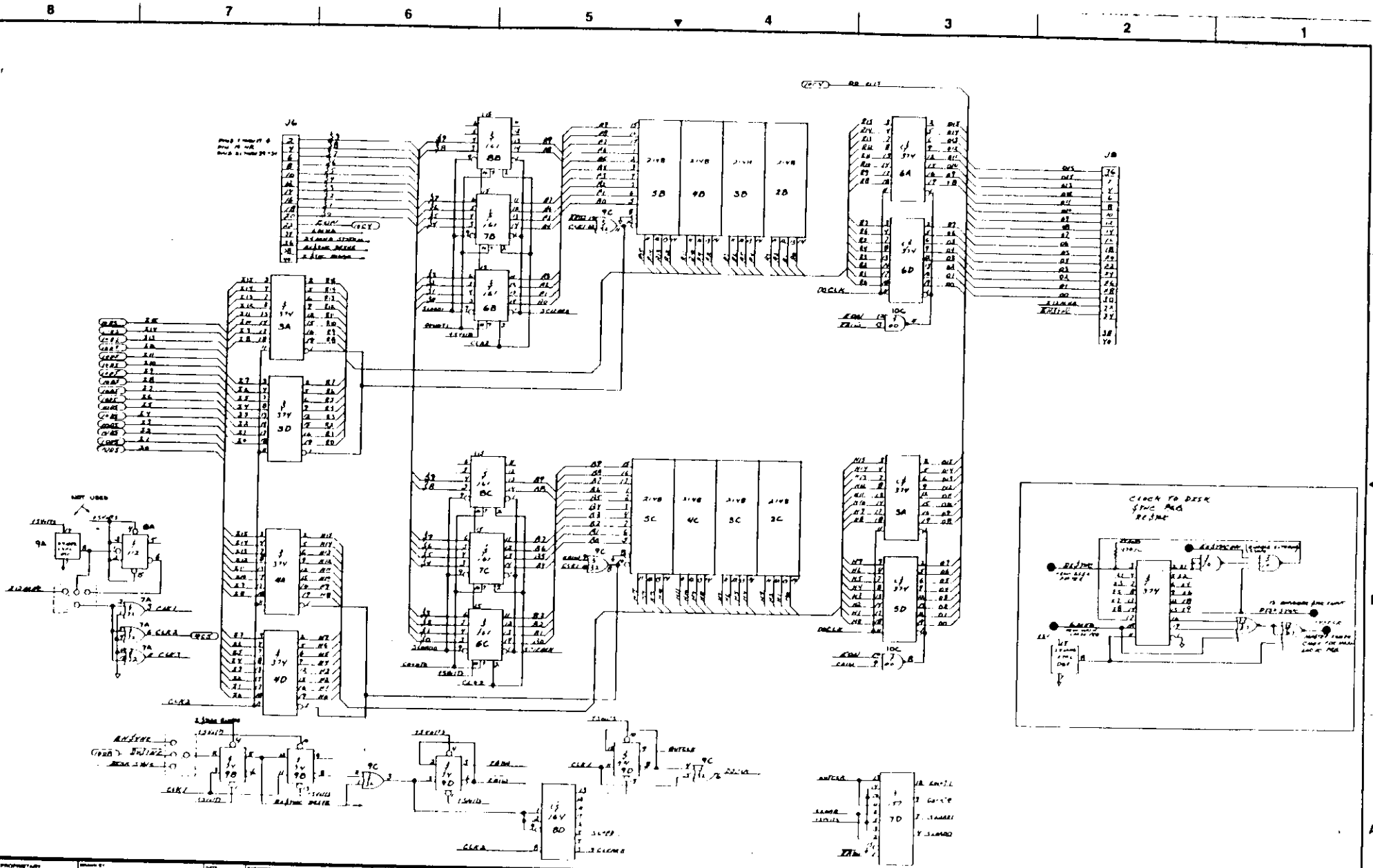
This page contains the VIDEO LOOKUP TABLE AND VIDEO OUTPUT DRIVERS. High speed moving object data is combined with background video data to form an 8 bit address to the lookup table (8S). The data at this address is the color information that should be displayed on the crt. The color information (in the form of 5 bits for each color: red, blue, and green) is placed in the lookup table by the CPU through address buffer (10R) and data buffers (7R) and (9R). Control of this data read and write operation is performed by (8L). Connector J8 is the external digital video input which accepts the output from the video expander pcb. This digital input is enabled by bit 15 of the lookup table through (9J) being a logic "0". The video output stages are a form of digital to analog converter which converts a weighted current amount, depending on the position of the active bit, into a voltage. This voltage swing is from approximately .8 volts to 3.5 volts.


EXPANDER VIDEO
VIDEO OUTPUT TO RGB MONITOR
VIDEO OUTPUT TO RGB MONITOR

VIDEO EXPANDER SCHEMATIC PAGE 9 of 10

Schematic Grid Location	Board Location	Function
C7	A3,D3	Digital video buffer odd line
B7	A4,D4	Digital video buffer even line
A7	B9	External sync enable
D6	B8,B7,B6	Odd line address counter
B6	C8,C7,C6	Even line address counter
A6	D9	Odd or even line flip flop
A5	D8	Line reset and start control
A4	D9	Output clock generation
D4	B5,B4,B3,B2	Odd video line RAM
B4	C5,C4,C3,C2	Even video line RAM
D3	A6,D6	Odd line output buffer
B3	A5,D5	Even line output buffer
A3	D7	Odd even RAM R/W control
B1	-	External resync pcb

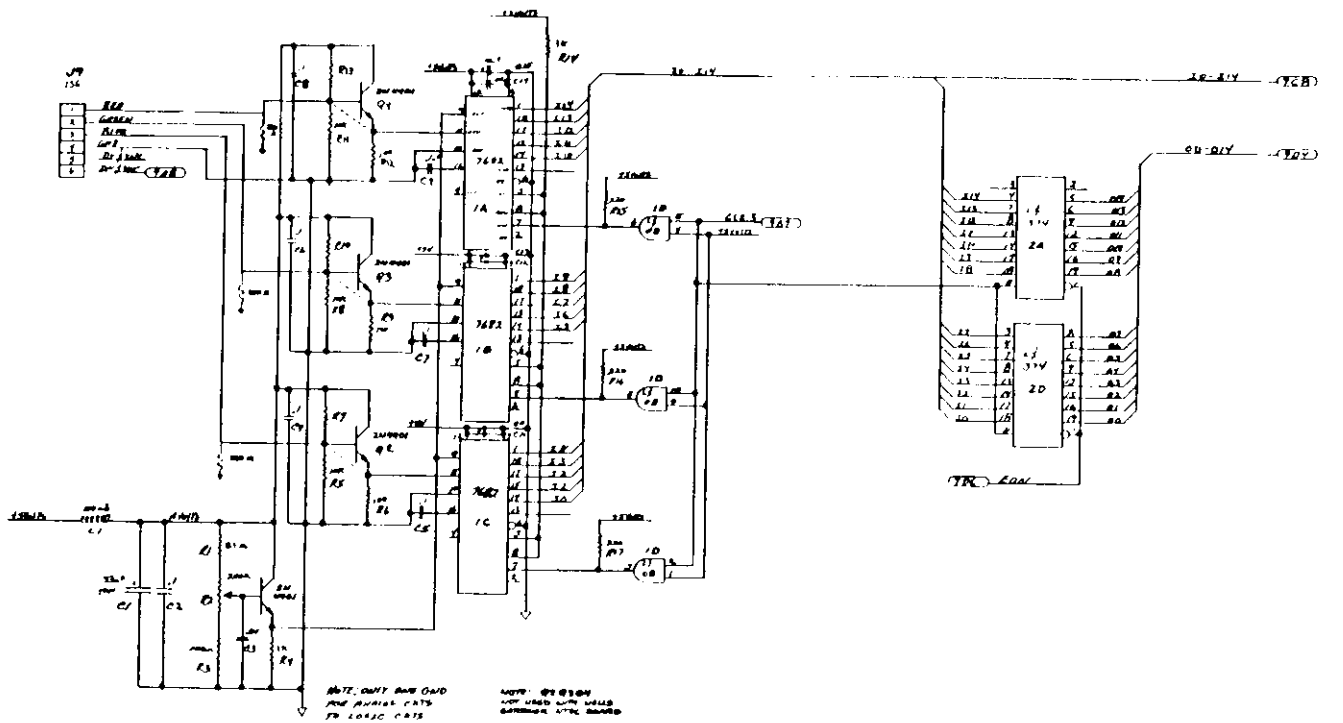
The Expander functions to store a line of video which has been converted to digital by the analog to digital converter, on page 10. This digital data is in a form of 5 bits per color (5 for each red, green and blue) for a total of 15 bits of data. This data is applied to an odd and even line buffer RAM system (B5,B4,B3,B2 and C5,C4,C3,C2) through buffer registers (A3,D3 and A4,D4). The data is stored sequentially by counters (B8,B7,B6 and C8,C7,C6) in the buffer RAMs at a 12mhz rate. At the start of each display line data stored in the buffer RAM during the previous line is available to be displayed during the current line. The address of the start location in the buffer RAM originates from the main logic pcb and is used to define the start position of the expanded line. When the data is read from the buffer RAM, it is read at a 6mhz rate which appears on the screen display as a normal line of data, only shifted in the left or right direction.


8
7
6
5
4
3
2
1
D
C
B
A
J6
J8
3A
3B
3C
3D
4A
4B
4C
4D
5A
5B
5C
5D
6A
6B
6C
6D
7A
7B
7C
7D
8A
8B
8C
8D
9A
9B
9C
10C
CLOCK TO DESK
SYNC PULSE
RESYNC
NOT USED
PROPRIETARY
D
9
10

A TO D CONVERTER EXPANDER SCHEMATIC PAGE 10 of 10

Schematic Grid Location	Board Location	Function
D7,C7	Q4,Q3,Q2	RGB analog video input buffers
B7	Q1	Analog voltage range control
D6,C6	A1,B1,C1	RGB analog to digital converters
C4	A2,D2	Expander bypass buffers

The input through P9 is from the NTSC to RGB converter pcb. This input is an analog voltage for the three colors: red, green, and blue. Each analog color voltage is converted to digital data by separate analog to digital converters (A1,B1,C1). The output of these converters form a 15 bit word that is made up of 5 bits of color for each red, green, and blue. This data word is then applied to the odd/even line buffers or directly to the output of the expander. The adjustment of R2 allows the dynamic range of the analog to digital converter to be set. This adjustment interacts with the contrast control on the NTSC converter board.



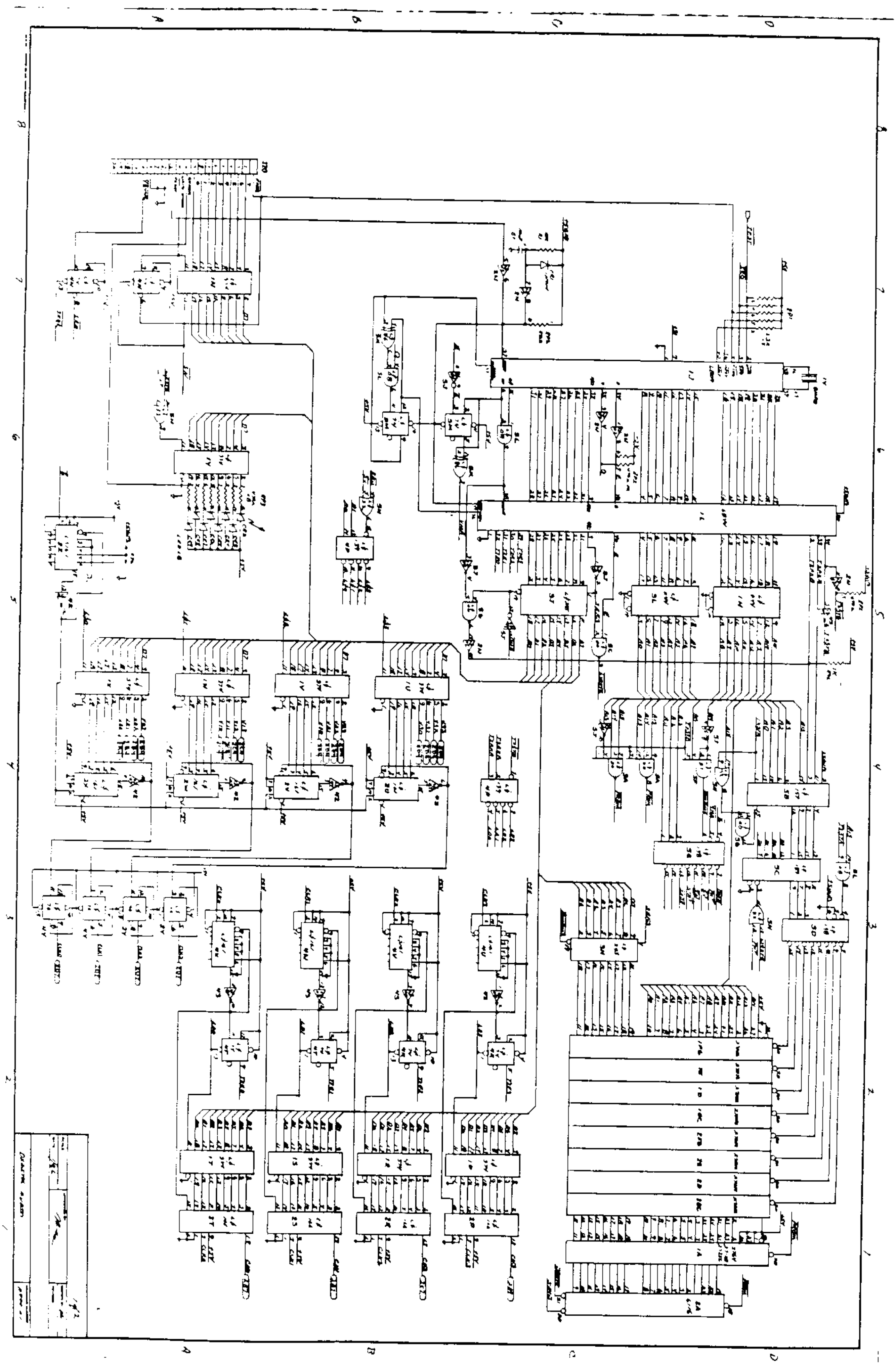
PROPRIETARY	DRAWN BY	DATE	DESIGNED	DATE	SHEET 10 OF 10	RELEASED	ISSUED FOR	SIZE D	A TO D CONVERTER EXPANDER
	CHECKED	DATE	PROJECT ENGINEER	DATE					

DIGITAL AUDIO SCHEMATIC PAGE 1 of 2

Schematic Grid Location	Board Location	Function
D7	J1	Audio system CPU
C7	N2	Power on reset circuit
A7	N1	Audio board command input buff
A6	Y1	Audio system status reg
A5	Z2	Low speed clock generator
D6	L1	DMA device
B6	M5	DMA grant and control
B5	P4	Address decode 1 of 4 channels
D5	1H,3L	Address line buffers
C5	3J	Data line buffer
D4	B5	DMA or CPU to ROM control
D3	C5	Bank address control RAM
D3	D5	ROM enable decoding
D3	E2	CPU address decoding
D4	A5	CPU ROM or RAM decoding
C3	H3	ROM and RAM data buss buffer
D2	F1,E1,D1,B1,F2,E2,D2,B2	Digital Audio data ROMs
D1	A1	Audio CPU program ROM
D1	A2	Audio CPU system RAM
B4,A4	U1,V1,W1,X1	Clock rate and volume control
B4,A4	U2,V2,W2,X2	Channel clock rate generator
A3	Y2,Y4	Channel clock rate buffers
B3	U4,V4,W4,X4	Channel reload control
B2	R4,T4	Channel reload flag flip flop
B2	P1,R1,S1,T1	Channel data buffer
B1	P2,R2,S2,T2	Channel parallel to serial

The heart of the digital audio system is a MC6809 central processing unit (J1) and the MC6844 DMA device (L1). The program data is stored in the ROM located at (A1), and the digital audio data is stored in ROMs at locations F1, E1, D1, B1, F2, E2, D2, and B2. This stored data is accessed by the DMA device, and then transferred to one of the four audio channels. Control of the DMA device is performed by the CPU, which sets up addresses and count data.

Each audio channel has a controllable clock rate for the conversion of parallel data to serial data. This clock rate determines the rate at which data is applied to the delta demodulator devices, located on page 2 of the audio logic diagram.

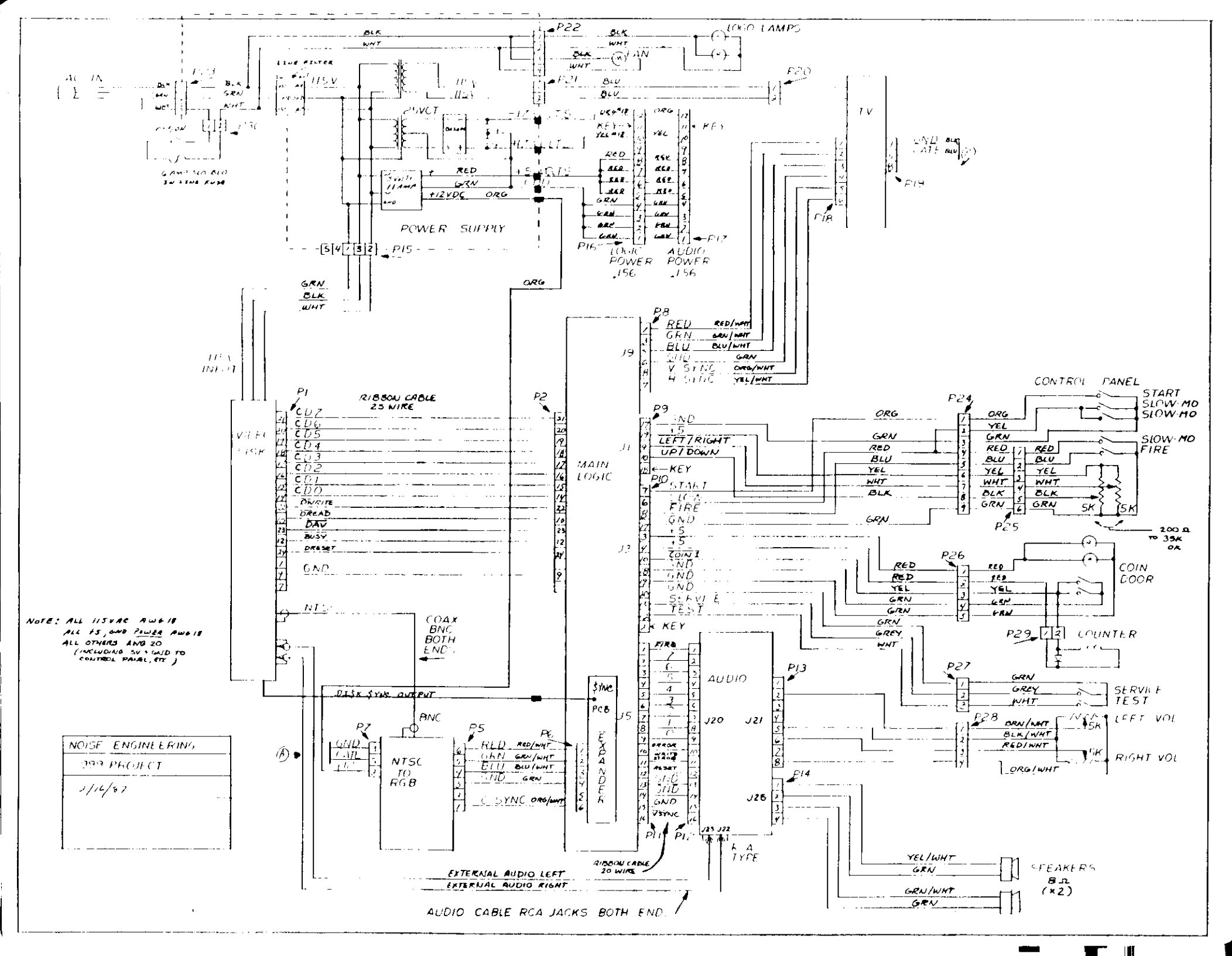


ANALOG AUDIO SCHEMATIC PAGE 2 of 2

Schematic Grid Location	Board Location	Function
D6,C6,B6	Y5,T5,Y6,T6	Serial digital to analog
D5,C5,B5	W5,W6	Channel low pass filters
D4,C4,B4	L6,L7,N7,N6	Channel volume control
D3,C3	K7,K6 (Opt.)	External volume control
D2,C2	E6	Power amplifier drivers
D2,C2	Q7,Q8,Q9,Q10	Power amplifier output drivers
A4	E6	External audio input buffers
B2	VR1,VR2	Audio power regulators

The conversion from serial digital data to analog data is accomplished by the MC3418 devices (Y5,T5,Y6,T6). Then the analog data is sent through a low pass filter circuit, MC3403s (W5,W6) to remove conversion noise. The amplitude of the analog signals are then controlled by the electronic attenuators CA3080 (L6,L7,N7,N6). External left and right audio from the video disk player is applied through amplifier buffers MC3403s (E6). This audio is combined with the digital generated audio output of the CA3080 and both are applied to the dual audio power amplifiers. The dual audio power amplifiers are made up of the MC3403 (E6) amplifier driver and transistors (Q7,Q8,Q9,Q10).

ANALOG AUDIO


AC IN
LINE FILTER
115V
POWER SUPPLY
P22
LOGO LAMPS
P21
P20
TV
P18
P19
P17
P16
LOOP POWER .156
AUDIO POWER .156
P15
P8
RED
GRN
BLU
GND
V SYNC
H SYNC
P9
P10
P1
P2
RIBBON CABLE 25 WIRE
MAIN LOGIC
J9
J1
J2
CD7
CD6
CD5
CD4
CD3
CD2
CD1
CD0
DWRITE
DREAD
DAV
BUSY
DRESET
GND
NTSC
COAX BNC BOTH ENDS
DISK SYNC OUTPUT
$YNC PCB EXPANDER
U5
P7
P5
P6
NTSC TO RGB
BNC
RED
GRN
BLU
GND
C SYNC
P24
P25
P26
P27
P28
P29
CONTROL PANEL
START
SLOW-MO
SLOW-MO
SLOW-MO FIRE
200 Ω TO 35K OR
COIN DOOR
COUNTER
SERVICE TEST
LEFT VOL
5K
RIGHT VOL
5K
P13
P14
P11
P12
AUDIO
J20
J21
J26
J25 J22
RA TYPE
RIBBON CABLE 20 WIRE
EXTERNAL AUDIO LEFT
EXTERNAL AUDIO RIGHT
AUDIO CABLE RCA JACKS BOTH END
SPEAKERS 8Ω (×2)
NOTE: ALL 115VAC AWG 18
ALL +5, GND POWER AWG 18
ALL OTHERS AWG 20
(INCLUDING 5V & GND TO CONTROL PANEL, ETC)
NOISE ENGINEERING
299 PROJECT
1/16/87