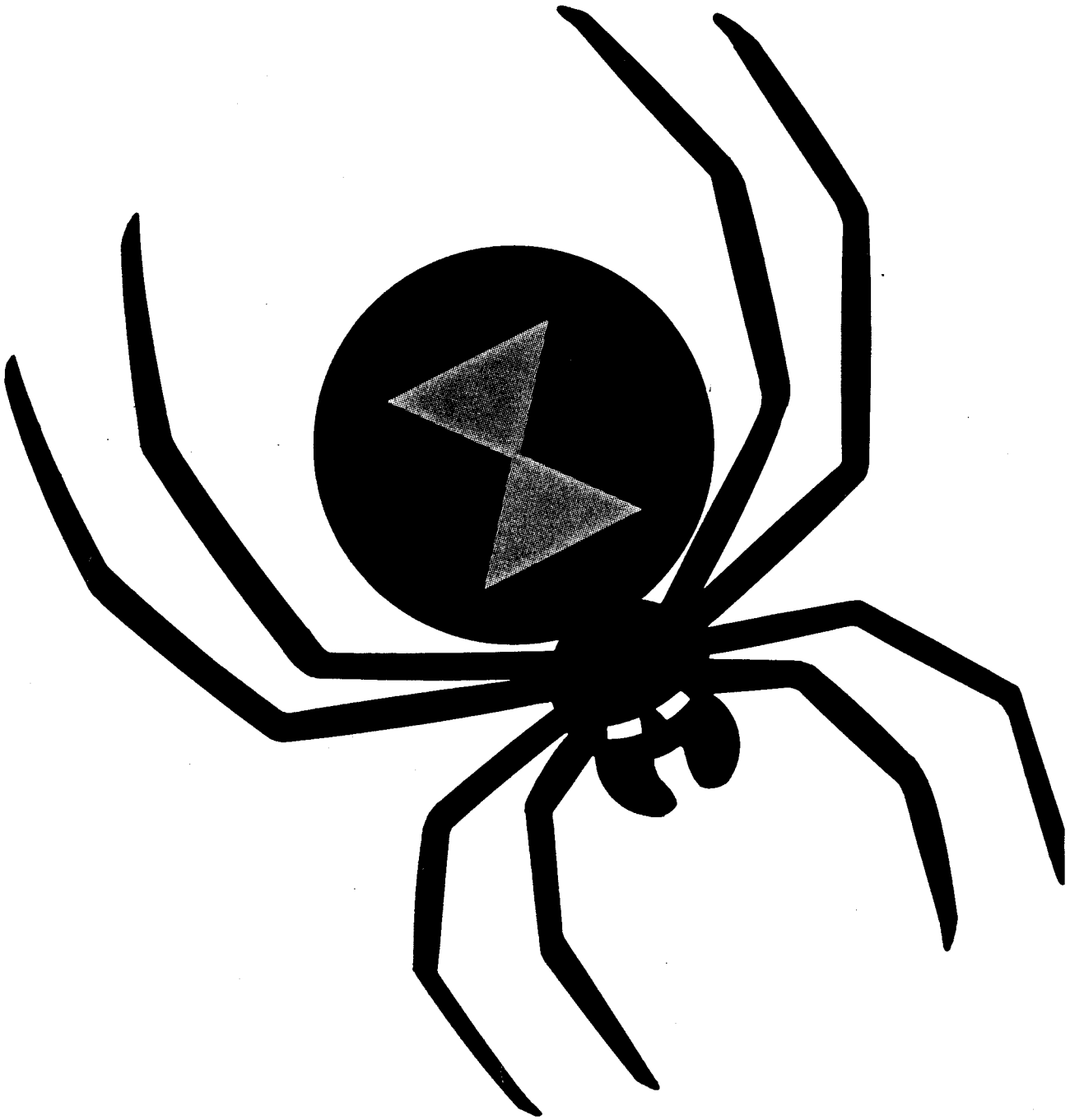
TM-234
1st printing

# BLACK WIDOW™

# Operators Manual

With Illustrated Parts Lists



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# Notice Regarding Non-ATARI Parts

**WARNING**

Use of non-ATARI parts or modifications of your ATARI game circuitry may adversely affect the safety of your game, and injure you or your players.

You may void the game warranty (printed on the inside back cover of this manual) if you do any of the following:

- Substitute non-ATARI parts in the game
- Modify or alter any circuits in the game by using kits or parts *not* supplied by Atari.


to licensed communications services is not permitted by the FCC (Federal Communications Commission).

If you suspect interference from an ATARI game at your location, check the following:

- All grounds (green wires) in the game are properly connected as shown in the game wiring diagram, and
- The power cord is properly plugged into a *grounded* 3-wire outlet.

If you are unable to solve the interference problem, please contact ATARI Customer Service. See page vi for service in your area.

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# Set-Up Procedures

## A. How to Use this Manual

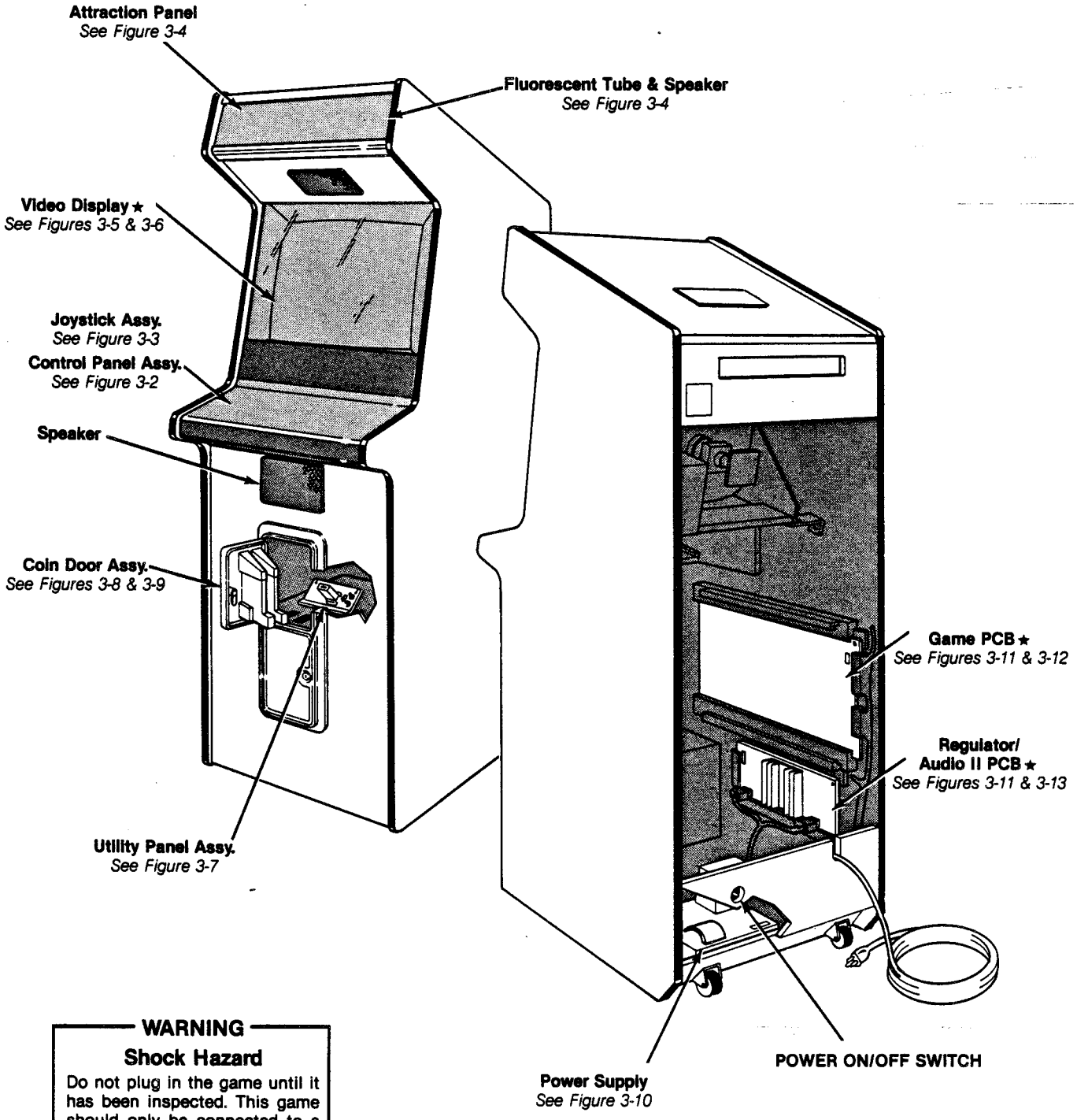
This manual, written for game operators and service technicians, describes the Black Widow Upright game.

Chapter 1 contains game specifications, inspection procedures, voltage plug and fuse information, switch locations, and option information.

Chapter 2 contains self-test procedures.

Chapter 3 contains illustrated parts lists. Figures 1-1 and 3-1 illustrate the Upright game cabinet. These figures refer you to other places in the manual for more information about specific cabinet parts.

Chapter 1




**WARNING**

**Shock Hazard**

Do not plug in the game until it has been inspected. This game should only be connected to a grounded 3-wire outlet. If you have only a 2-wire outlet, we recommend you hire a licensed electrician to install a grounded outlet. Players may receive an electrical shock if this game is not properly grounded!

★ *Item with a serial number label*

**Figure 1-1 Game Overview**

# B. Game Overview

Black Widow challenges you, the spider, to defend your web from mosquitoes, beetles, hornets, and other insects. Use two joysticks to avoid or shoot enemies and bugs. Watch out for the grenade, rocket bug, thunder bug, spoiler, and collect the grubstakes for extra points! Skill Step™, the Atari feature that allows players to start consecutive games at higher levels, offers players continual challenge.

All major parts of the Black Widow game are illustrated in Figure 1-1.

# C. Installation Specifications

Table 1-1 describes the physical, electrical, and environmental specifications of the game.

**Table 1-1 Installation Specifications**

| | |
|---|---|
| Power | 200 W |
| Temperature | 0° to +38° C (+32° to +100° F) |
| Humidity | Not to exceed 95% relative |
| Height | 184 cm (72½ in.) |
| Space Required | 64 x 80 cm (25½ x 31½ in.) |

# D. Inspecting the Game

Please inspect your game carefully to ensure that it was delivered to you in good condition.

**WARNING**

**Shock Hazard**

To avoid electrical shock, do not plug in the game until the procedures in Sections D and E have been completed!

Do not touch internal parts of the display with your hands or with metal objects held in your hands!

1. Examine the exterior of the game cabinet for dents, chips, or broken parts.
2. Remove the screws from the rear access panel. Unlock and open this panel and the coin door. Inspect the interior of the game as follows:
   a. Ensure that all plug-in connectors (on the game harnesses) are firmly plugged in. Replug any connectors found unplugged. Do not force connectors together. The connectors are keyed so they only fit in the proper orientation. A reversed edge connector may damage a PCB and will void your warranty.
   b. Ensure that all plug-in integrated circuits on the PCB are firmly plugged into their sockets.
   c. Remove the tie-wrap that secures the coiled power cord inside the cabinet. Inspect the power cord for any cuts or dents in the insulation. Repair or replace it as required. Place the square strain-relief plate in the wood slot at the bottom of the rear panel opening.
   d. Inspect major subassemblies, such as the power supply, control panel, and video display. Make sure they are mounted securely and that the green ground wires are connected.

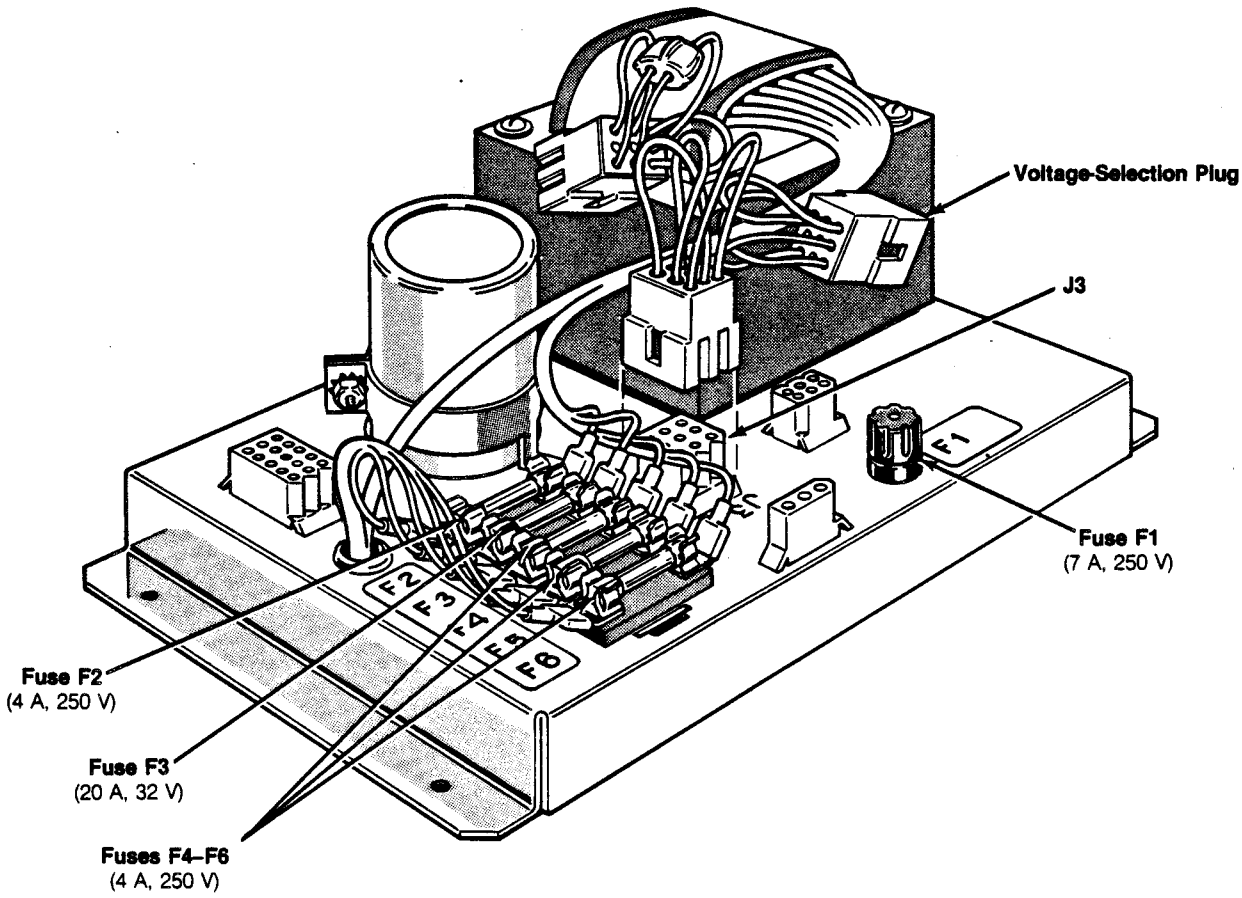
# E. Voltage-Plug Selection and Fuses

The power supply in your game contains six fuses. When you replace a fuse, use the identical type fuse with the same electrical rating (see Figure 1-2).

The power supply operates on the line voltage of many countries. The power supply comes with either one, two, or three voltage-selection plugs. Plug voltages and wire colors are 100 VAC (violet wire color), 120 VAC (yellow wire color), 220 VAC (blue wire color), and 240 VAC (brown wire color).

See Figure 1-2 for placement of the voltage-selection plug. Before plugging in your game, check your line voltage. Next, check the wire color on the voltage-selection plug. Make sure the voltage-selection plug is correct for the voltage of your location.

Now plug the game into a grounded 3-wire outlet.




Fuse cover not shown.

**Figure 1-2 Voltage-Selection Plug and Fuse Locations**

# F. Switch Locations

## Power On/Off Switch

The power on/off switch is located on the back of the cabinet on the lower left side (see Figure 1-3).

## Utility Panel Switches

The volume control, coin counter, self-test switch, and auxiliary coin switch are on the utility panel. The utility panel is located inside the upper coin door (see Figure 1-3). The volume control adjusts the level of sound produced by the game. The coin counter records the number of coins entered into the game. The self-test switch initiates and stops the self-test mode. The auxiliary coin switch is used to credit the game without activating a coin counter.

## Option Switches

Option switches for game price, number of lives, bonus, and difficulty selection are on the CPU printed-circuit board (PCB). These switches are at locations D4, B4, and P10/11 (see Figure 1-3).

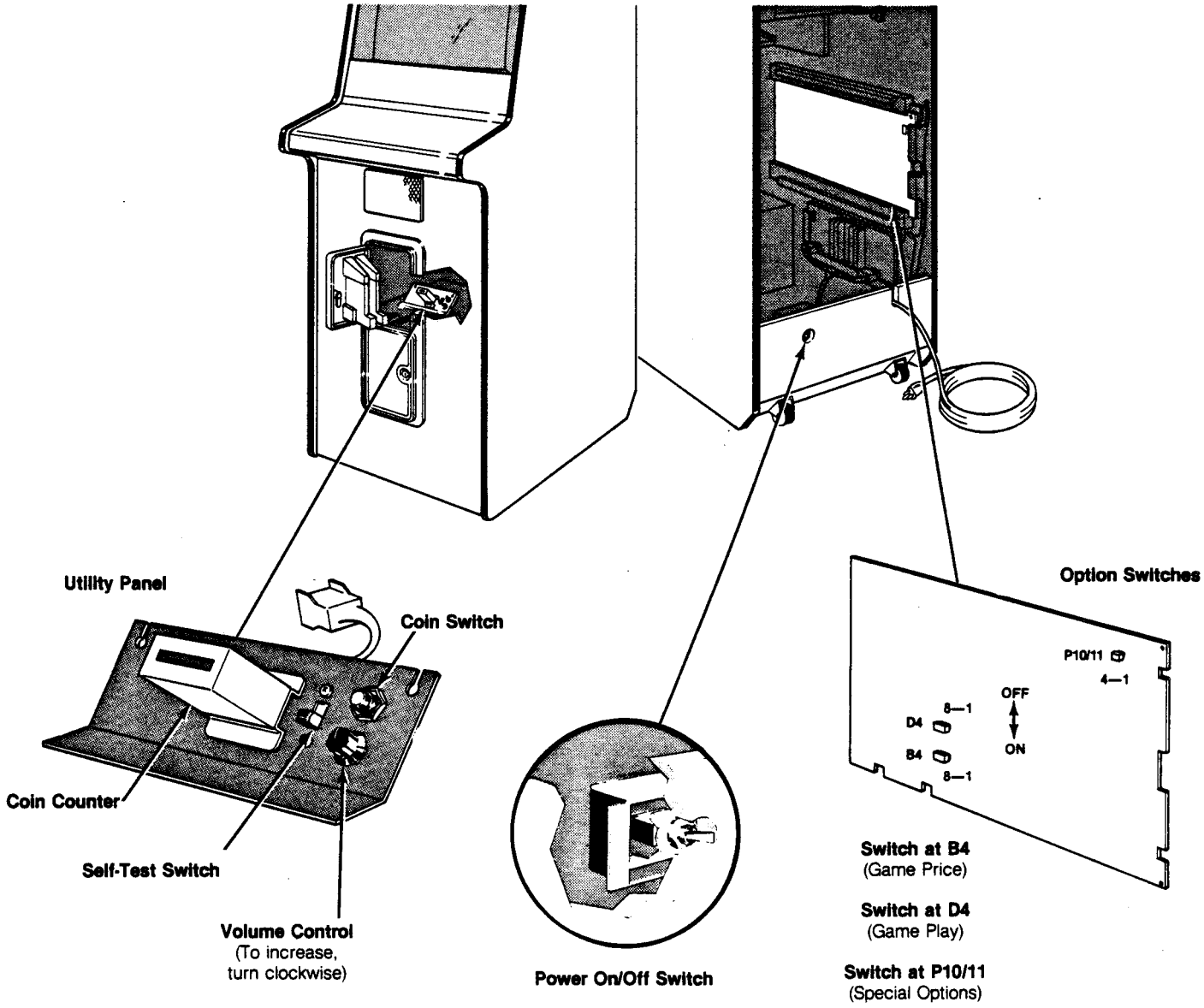



**Figure 1-3 Switch Locations**

# G. Selecting the Options

Settings of the option switches are explained in Tables 1-2, 1-3, and 1-4. Options preset at the factory are shown by the ◄ symbol. However, you may change the settings to suit your needs.

To verify option switch settings, turn the game *off* and back *on*. Then set the self-test switch to *on* and verify the option switch settings on the self-test display as described in Chapter 2, *A. Obtaining the Operator Information Display.*

Table 1-2 describes the settings for the 8-toggle switch at location D4. This switch selects the game price options, the coin mechanism multipliers, and the bonus play options.

The *coin mechanism* is a device on the inside of the coin door that inspects the coin to determine if the correct coin has been inserted. After this inspection, the mechanism either accepts or rejects the coin.

The *multipliers* (D4 switches 4-6) determine how much each coin mechanism will be worth to the game's logic. The coin door has two mechanisms.

The basic unit of measurement is a coin worth $.25 or 1 DM, which equals a multiplier of x1. Thus, if you have a 2 DM/1 DM coin door with two coin counters, set switch 8 at location D4 to *on* and switches 5 and 6 to *off.*

You may offer bonus play for certain combinations of coins inserted into the game. For example, with the game set at $.25 per play, players who deposit four successive quarters, then press the start switch, can recieve a bonus play. The bonus feature encourages players to insert more money than just the minimum required for one game. All coins must be inserted before pressing the start switch.

## Table 1-2 Switch Settings for Price Options

| Settings of 8-Toggle Switch on Black Widow CPU PCB *(at D4)* | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Option |
| Off | Off | | | | | | | 1 coin/1 credit◄ |
| On | On | | | | | | | 1 coin/2 credits |
| On | Off | | | | | | | 2 coins/1 credit |
| Off | On | | | | | | | Free play |
| | | Off | Off | | | | | Right coin mechanism x 1◄ |
| | | On | Off | | | | | Right coin mechanism x 4 |
| | | Off | On | | | | | Right coin mechanism x 5 |
| | | On | On | | | | | Right coin mechanism x 6 |
| | | | | Off | | | | Left coin mechanism x 1◄ |
| | | | | On | | | | Left coin mechanism x 2 |
| | | | | | Off | Off | Off | No bonus coins (0)*◄ |
| | | | | | Off | On | On | No bonus coins (6) |
| | | | | | On | On | On | No bonus coins (7) |
| | | | | | On | Off | Off | For every 2 coins inserted, logic adds 1 more coin (1) |
| | | | | | Off | On | Off | For every 4 coins inserted, logic adds 1 more coin (2) |
| | | | | | On | On | Off | For every 4 coins inserted, logic adds 2 more coins (3) |
| | | | | | Off | Off | On | For every 5 coins inserted, logic adds 1 more coin (4) |
| | | | | | On | Off | On | For every 3 coins inserted, logic adds 1 more coin (5) |

**The numbers in parentheses will appear on the BONUS ADDER line in the Operator Information Display (Figure 2-1) for these settings.*
*◄Manufacturer's recommended setting*

Table 1-3 describes the settings for the 4-toggle switch at location P10/11. This switch selects whether credited coins are counted on one or on both coin counters.

## Table 1-3 Switch Settings for Special Options

| Settings of 4-Toggle Switch on Black Widow CPU PCB *(at P10/11)* | | | | Option |
|---|---|---|---|---|
| 4 | 3 | 2 | 1 | |
| | | | On | Credits counted on one coin counter |
| | | | Off | Credits counted on two separate coin counters |

Table 1-4 describes the settings for the 8-toggle switch at location B4. This switch selects the game's starting level, bonus spiders, and difficulty level.

## Table 1-4 Switch Settings for Bonus and Difficulty Options

| Settings of 4-Toggle Switch on Black Widow CPU PCB *(at B4)* | | | | | | | | Option |
|---|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
| Off | Off | | | | | | | Maximum start at level 13 |
| On | Off | | | | | | | Maximum start at level 21◄ |
| Off | On | | | | | | | Maximum start at level 37 |
| On | On | | | | | | | Maximum start at level 53 |
| | | Off | Off | | | | | 3 spiders per game◄ |
| | | On | Off | | | | | 4 spiders per game |
| | | Off | On | | | | | 5 spiders per game |
| | | On | On | | | | | 6 spiders per game |
| | | | | Off | Off | | | Easy game play |
| | | | | On | Off | | | Medium game play◄ |
| | | | | Off | On | | | Hard game play |
| | | | | On | On | | | Demonstration mode |
| | | | | | | Off | Off | Bonus spider every 20,000 points◄ |
| | | | | | | On | Off | Bonus spider every 30,000 points |
| | | | | | | Off | On | Bonus spider every 40,000 points |
| | | | | | | On | On | No bonus |

◄*Manufacturer's recommended setting*

# Self-Test Procedure

This game will test itself and provide data to show that the game circuitry and controls are operating properly. Self-test data is presented visually on the video display and audibly through the speakers. No additional equipment is required.

We suggest that you perform the self-test procedure when you first set up the game, each time you collect money, when you change the game options, when you erase scores and times, or when you suspect a game failure.

Chapter 2

# A. Obtaining the Operator Information Display

Set the self-test switch to the on position (refer to Figure 1-3 for the location of the self-test switch). Patterns will appear on the display for a few seconds, then an operator information display will appear as shown in Figure 2-1. The operator information display shows the game statistics and certain game option information. The information display is also used to erase game scores and times as described in the following procedure.

All credits are cancelled when the self-test switch is turned on. If the message EAROM BUSY PLEASE WAIT appears, wait for it to disappear before proceeding.

**NOTE**

The BONUS ADDER number (0 through 7) displayed indicates the price option selected by the option switch at location D4. Refer to Table 1-2 in Chapter 1, Switch Settings for Price Options, for the price option settings represented by the BONUS ADDER number.

```
HOLD FIRE THEN PRESS START 1
        FOR TEST
    LIVES PER GAME 3
    MAX START WAVE 21
    GAMES PLAYED          1
    AVERAGE GAME TIME   124
    LEFT MECH X1
    RIGHT MECH X1
    BONUS ADDER 0
          MEDIUM
  BONUS SPIDER EVERY 20000
      1 COIN 1 PLAY
```

**Figure 2-1 Operator Information Display**

### To Erase Scores and Times:

1. Obtain an operator information display as shown in Figure 2-1 by setting the self-test switch to the on position.
2. Press the 1-player start button until the screen displays the appropriate instruction, i.e., HOLD FIRE THEN PRESS START 1 TO (CLEAR SCORES) (CLEAR TIMES) (CLEAR TIMES AND SCORES).
3. Hold FIRE joystick forward, then press the 1-player start button. The words EAROM BUSY PLEASE WAIT will appear on the screen until the entire table is erased. Wait until the display disappears before proceeding.
4. Set the self-test switch to the off position to erase the operator information display.

# B. Obtaining the Self-Test Display

The following information includes instructions for obtaining various self-test displays. These displays are provided to quickly check the game's operation and locate malfunctions in the game controls and circuitry. If there is a failure, the game produces audiovisual indications to help you find the problem.

**NOTE**

This procedure does not test the coin door lockout coils and coin counter. If the lockout coils do not energize when the game is on, suspect the lockout coil wiring, coin door harness, game PCB harness, latch R9, or driver Q2 of the game PCB. Troubleshoot using the game schematics.

### SCREEN 1

The screen 1 display shown in Figure 2-2 is obtained by setting the self-test switch to the on position. Then hold the FIRE joystick forward and press the 1-player start button. If the test passes, the display will go blank for a few seconds before displaying screen 1. This display indicates the condition of the ROM, RAM, and three other integrated circuits.

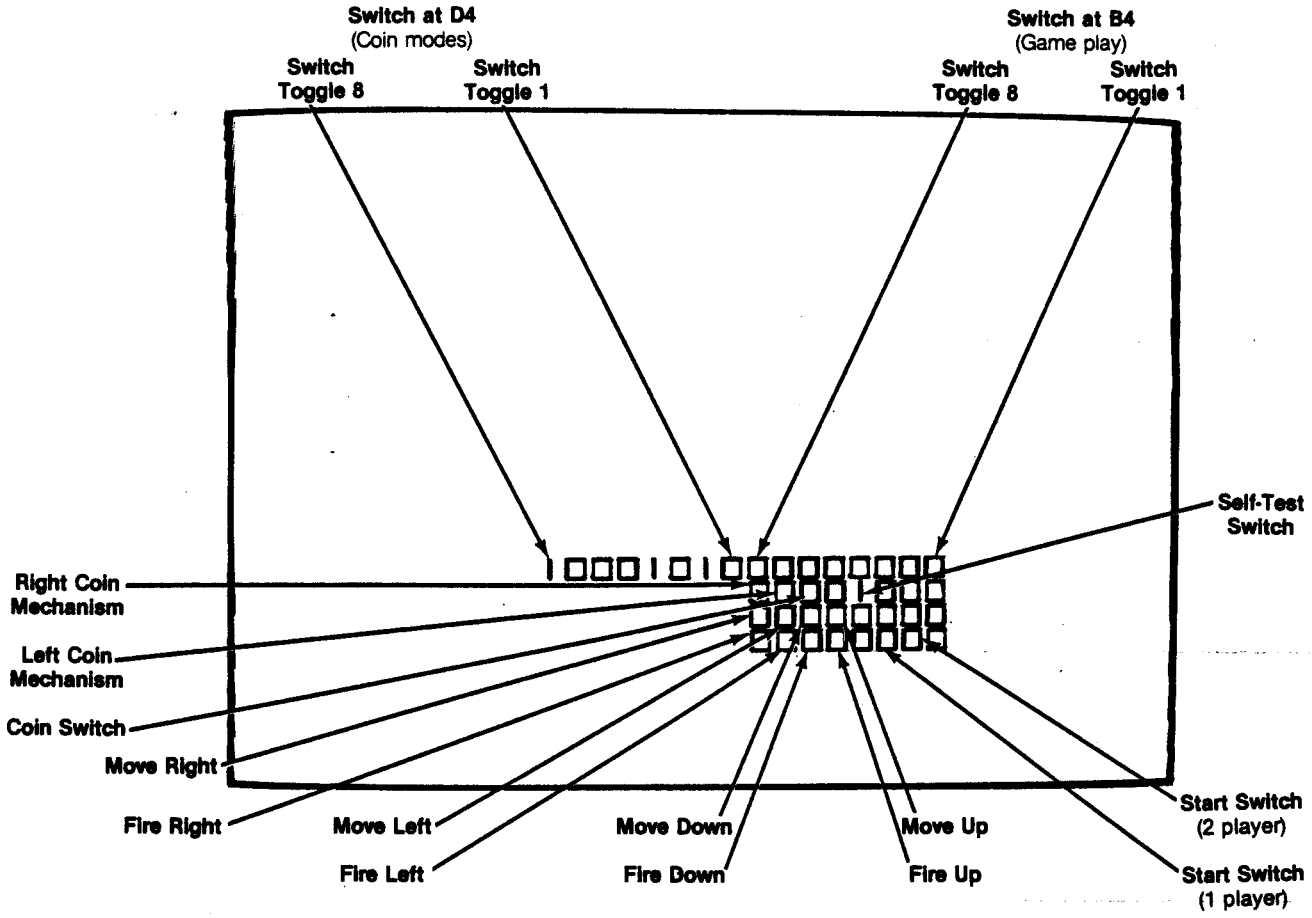



**Figure 2-2 Screen 1—Test Passes**

**RAM failure** is indicated by a sound and, if possible, an R displayed in the top center of the screen. Count the tones. One or two tones indicates RAM failure at game PCB location N/P1. Three or four tones indicate RAM failure at game PCB location K7 (see Table 2-1).

**Table 2-1 RAM Locations**

| Number of Tones | RAM Location on Game PCB |
|---|---|
| 1 or 2 | N/P1 |
| 3 or 4 | K7 |

**ROM failure** is indicated by one or more vertically arranged numbers displayed on the top half of the screen (see Figure 2-3 ). Use Table 2-2 to identify the bad ROM and determine its location.

**Table 2-2 ROM Locations**

| Screen Display | ROM Location on Game PCB |
|---|---|
| 0* | L7 |
| 1* | M/N7 |
| 2* | N/P7 |
| 3 | R7 |
| 4 | D1 |
| 5 | E/F1 |
| 6 | H1 |
| 7 | J1 |
| 8 | K/L1 |
| 9** | M1 |

**If this ROM is bad, you will hear a constant low tone and the program may be unable to display a screen image.*

***If this ROM is bad, the screen may be blank.*

**EAROM or CUSTOM I/O CHIP failure** is indicated by one letter in the top center of the screen. Use Table 2-3 to identify the bad IC and determine its location.

### Table 2-3 EAROM and Custom I/O Chip Locations

| Screen Display | Chip Location on Game PCB |
|---|---|
| E | EAROM at M2 |
| Q | Custom I/O chip at C/D3 |
| P | Custom I/O chip at B3 |

**SWITCH failure** is indicated by the associated 0 not changing to a 1 on the screen and no sound being produced when the switch is activated.

**SOUND failure** is indicated by no sound. Check the volume control on the utility panel, or troubleshoot using the game schematics.

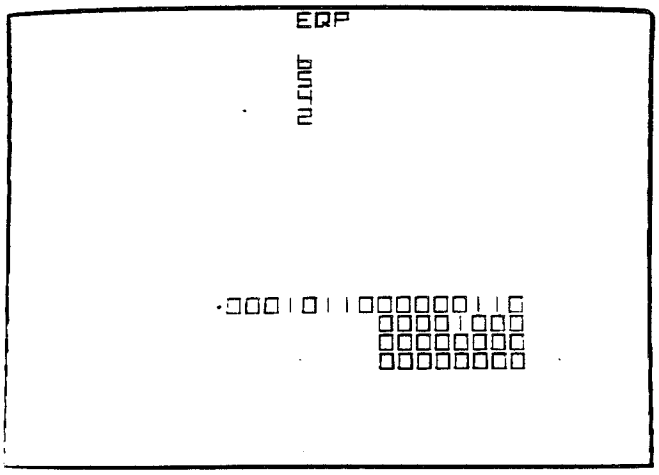


**Figure 2-3 Screen 1—Test Fails**

To see self-test screens 2 through 6, press the auxiliary coin switch on the utility panel once to advance to the next screen.

## SCREEN 2

A white diagonal grid pattern and a complete character set appear on the screen (see Figure 2-4). The edges of the grid pattern should touch the sides of the screen. If the display is not centered, symmetrical, or the proper size, adjust the X SIZE, Y SIZE, X CTR, Y CTR, X LIN, or Y LIN potentiometers on the game PCB (refer to the Schematic Package). If the characters are incorrect, check again for a 2 displayed in the preceding ROM failure test (Screen 1).

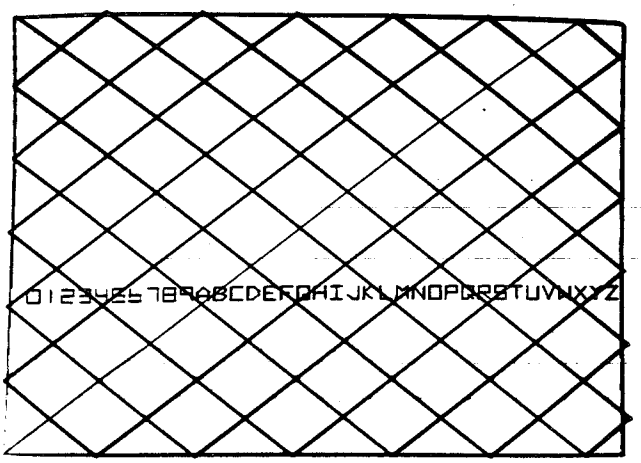


**Figure 2-4 Screen 2**

## SCREEN 3

A white box of decreasing size appears during this test. The box should shrink smoothly. There are seven stages, each with a tone. This pattern tests the binary and linear scaling circuitry. Troubleshoot using the game schematics.

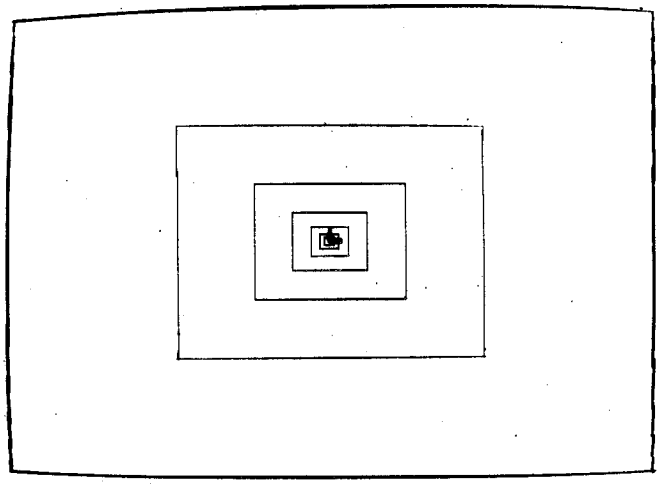


**Figure 2-5 Screen 3**

## SCREEN 4

A series of horizontal lines are visible in the middle of the screen. This is a raster test, used by the manufacturer only, to set the color levels.

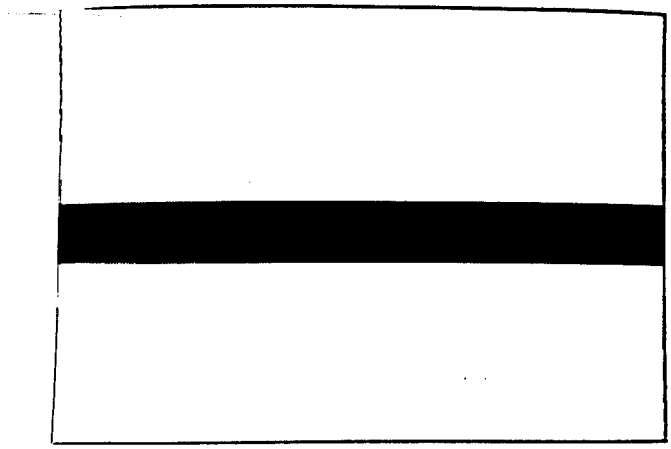


Figure 2-6 Screen 4

## SCREEN 5

This test checks the seven screen colors and six intensities of each color (see Figure 2-7). If the intensities do not progress from dim at the top of each color group to bright at the bottom, suspect a problem in the Z-axis of the game PCB or the video display. Use this pattern for the display tracking adjustments (refer to the color X-Y display manual).

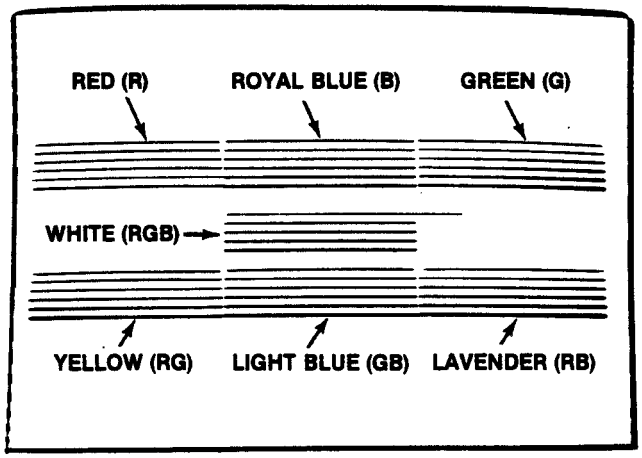



Figure 2-7 Screen 5

## SCREEN 6

A grid pattern touches the corners of the video display (see Figure 2-8). Press the 1-player start button to change colors. Use this pattern for the display purity and convergence adjustments (refer to the color X-Y display manual).

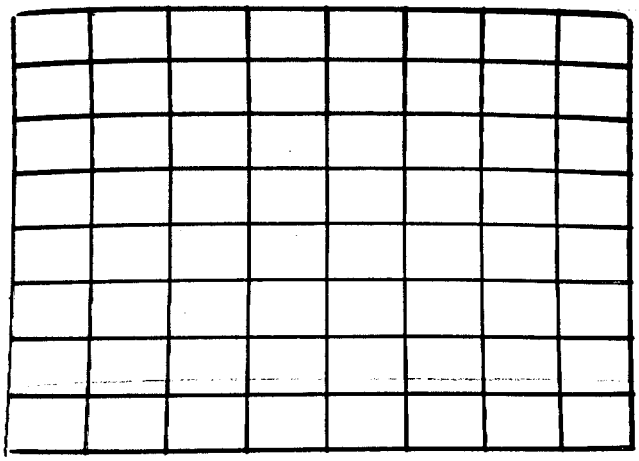


Figure 2-8 Screen 6

## SCREEN 7

Screen 7 display comprises a diagnostic program controlled by switches 2, 3, and 4 of the 4-toggle option switch at location P10/11 on the game PCB. This group of switches lets you choose one of six tests. These tests provide recurring sequences to make it easy for you to troubleshoot the vector-generator circuitry. The tests and their respective option switch settings are given in Table 2-4.

To display this screen, hold the auxiliary coin switch down, then press the 2-player start button. To exit from this screen, set the self-test switch to off.

During this test, the screen will either be blank or display vectors, depending on the settings of the switches at location P10/11 on the game PCB. Figure 2-9 shows these screens.

**Table 2-4 Vector-Generator Diagnostic Tests**

| Test | Action | Settings of 4-Position DIP Switch at P10/11 4 | 3 | 2 |
|---|---|---|---|---|
| Test 1 | Tests WDDIS every 4 msec (blank screen) | Off | Off | Off |
| Test 2 | Tests vector-generator halt instruction every .55 msec (blank screen) | On | Off | Off |
| Test 3 | Tests vector-generator long vector (and halt instruction) every 8.2 msec | Off | On | Off |
| Test 4 | Tests vector-generator jump instruction (and long vector and halt instruction) every 8.2 msec | On | On | Off |
| Test 5 | Tests vector-generator short vector instruction (and all of Test 4) every 8.6 msec | Off | Off | On |
| Test 6 | Tests vector-generator JSRL/RTSL instruction (and all of Test 5) every 10.2 msec | On | Off | On |
| Test 2 | Blank screen | Off | On | On |
| Test 2 | Blank screen | On | On | On |

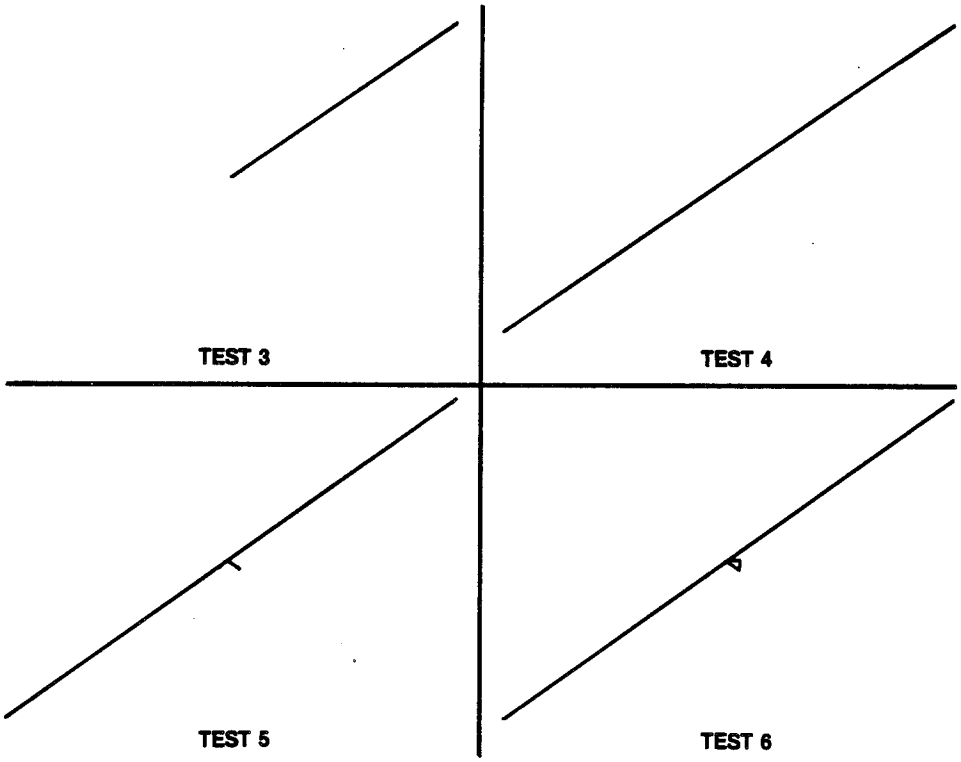



**Figure 2-9 Screen 7—Diagnostic Program Displays**

# Illustrated Parts Lists

This chapter provides information to order parts for your game. Common hardware (screws, nuts, washers, etc.) has been deleted from most of the parts lists. However, a parts list for the hardware needed to mount the game and Regulator/Audio II printed-circuit boards to the cabinet has been included.

The PCB parts lists are arranged in alphabetical order by component type. Each component subsection is arranged alphanumerically by reference designator.

Other parts lists are arranged alphanumerically by Atari part number. In these parts lists, all A- prefix numbers come first. Following these are numbers in sequence evaluated up to the hyphen, namely 00- through 99- then 000598- through approximately 201000-.

When ordering parts, please give the part number, part name, number of this manual, and serial number of your game (see Figure 1-1 for locations of serial numbers.) This will aid in filling your order rapidly and correctly. We hope the results will be less downtime and more profit from your game.

Atari Customer Service numbers are listed on the inside front cover of this manual for your convenience.

Chapter 3

# A. Cabinet-Mounted Assemblies

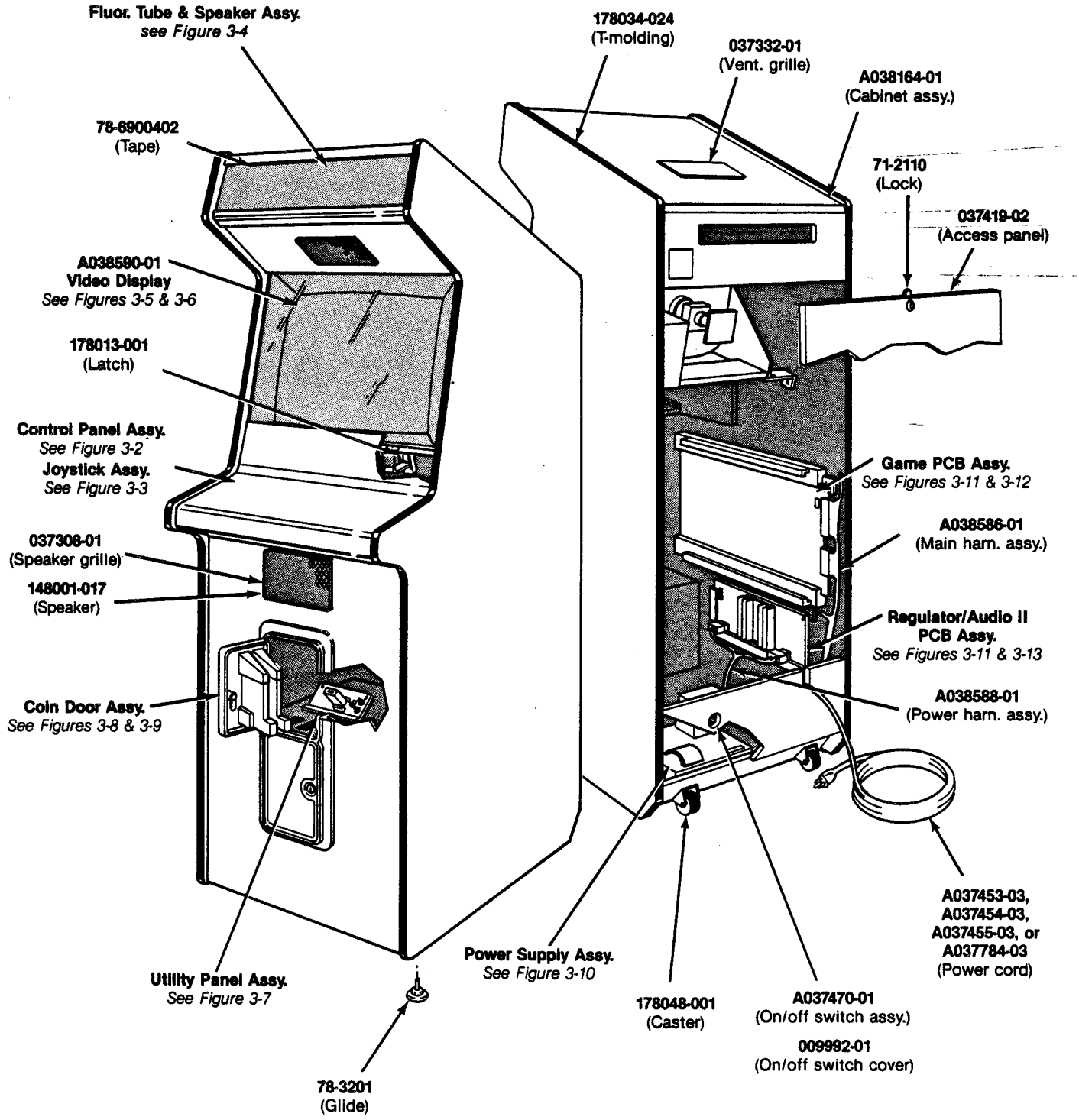



**Figure 3-1 Cabinet-Mounted Assemblies**

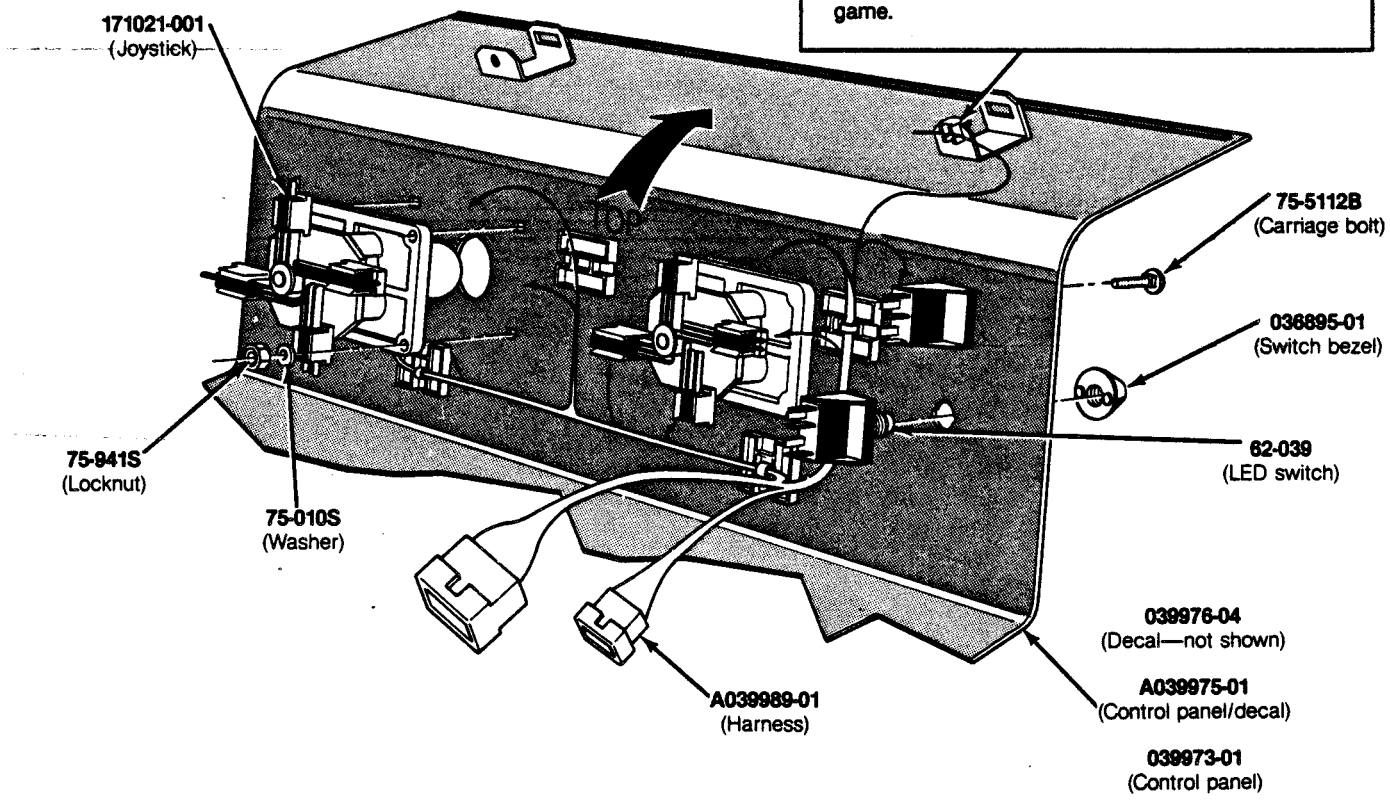
# Cabinet-Mounted Assemblies
# Parts List

| *Part No.* | *Description* |
|---|---|
| A002465-01 | Coin Counter |
| A037453-03 | Strain-Relief Power Cord *(U.S. and Canada)* |
| A037455-03 | Strain-Relief Power Cord *(Australia and New Zealand)* |
| A037470-01 | Power On/Off Switch/Mounting Plate Assembly |
| A037784-03 | Strain-Relief Power Cord *(United Kingdom, Ireland, Lebanon, Saudi Arabia, India, Hong Kong, Singapore, Egypt, Nigeria, Republic of South Africa, Zimbabwe)* |
| A038164-01 | Cabinet Assembly *(includes glides and PCB retainers, but not the rear access panel)* |
| A038586 | Main Harness Assembly |
| A038588-01 | Power Harness Assembly |
| A038590-01 | 19-Inch Wells-Gardner Color X-Y Video Display Assembly |
| A039990-01 | Main Conversion Harness Assembly *(not shown)* |
| | *The following four items are the technical information supplements to this game:* |
| SP-234 | Black Widow Schematic Package |
| ST-234-01 | Black Widow Label with Self-Test Procedure and Option Switch Settings |
| TM-183 | Service Manual for 19-Inch Wells Gardner Color X-Y Display |
| TM-234 | Black Widow Operators Manual |
| 71-2110 | Lock Mechanism *(for rear access panel)* |
| 78-3201 | Adjustable Glide |
| 78-6900402 | Vinyl Foam Single-Coated Adhesive Tape, ¼-Inch Wide x ⅛-Inch Thick |
| 009992-01 | On/Off Switch Cover |
| 037308-01 | Speaker Grille |
| 037332-01 | Ventilation Grille |
| 037419-02 | Rear Access Panel *(does not include lock)* |
| 038091-01 | Molded Coin Box *Acceptable substitute is part no. A037491-01* |
| 178013 | Spring Draw Latch |
| 178034-024 | ¾-Inch Black Plastic T-Molding |
| 178048-001 | 2-Inch Rigid Caster |

# B. Control Panel Assembly

**WARNING**

Players may receive an electrical shock if this control panel is not properly grounded! After servicing any parts on the panel, check that the ground wire is firmly attached to the metal tab on the inside of the control panel. Only then should you lock up the game.



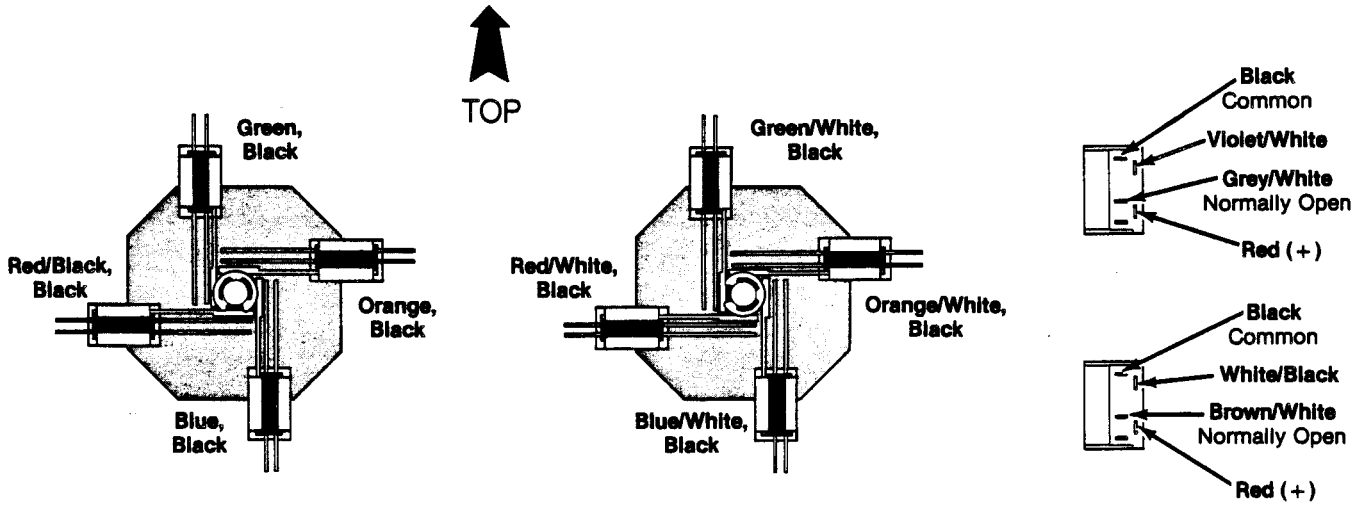




**Figure 3-2 Control Panel Assembly A039974-01 A**

# Control Panel Assembly
# Parts List

| *Part No.* | *Description* |
|---|---|
| A039975-01 | Control Panel with Decal |
| A039989-01 | Control Panel Harness Assembly |
| 62-039 | SPDT Momentary Pushbutton Start Switch with Red Light-Emitting Diode |
| 75-010S | #10 Flat Washer |
| 75-941S | #10-24 Hexagonal Locknut |
| 75-5112B | #10-24 x ¾-Inch Black Carriage Bolt |
| 78-6900402 | Vinyl Foam Single-Coated Adhesive Tape, ¼-Inch Wide x ⅛-Inch Thick |
| 036895-01 | Black Molded Switch Bezel |
| 039973-01 | Control Panel |
| 039976-04 | Control Panel Decal |
| 171021-001 | 8-Position Joystick |

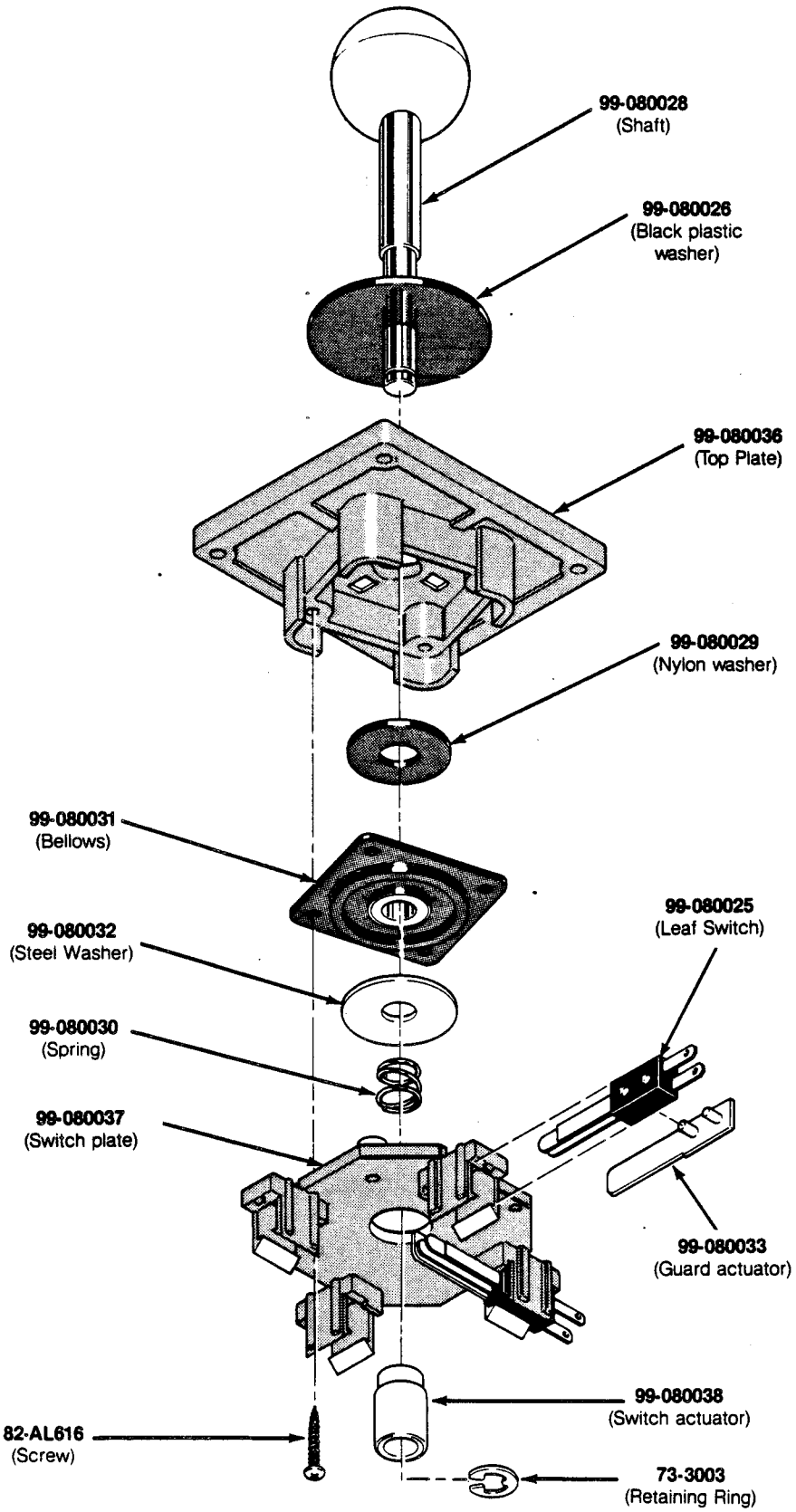
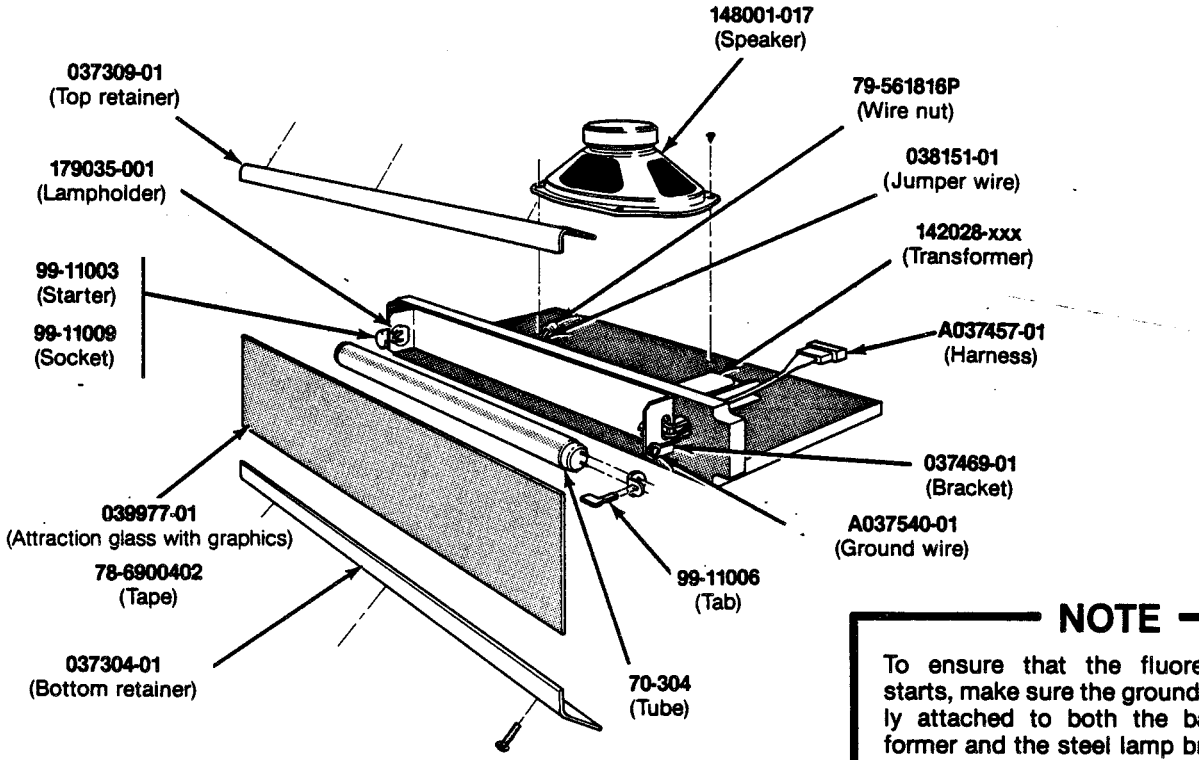



**Figure 3-3 8-Position Joystick Assembly 171021-001**

# 8-Position Joystick Assembly
# Parts List

| *Part No.* | *Description* |
|---|---|
| 73-3003 | Retaining Ring |
| 82-AL616 | #6 x 1-Inch Cross-Recessed Pan-Head Type BT Self-Tapping Steel Screw |
| 99-080025 | Leaf Switch |
| 99-080026 | 2-Inch Black Plastic Washer |
| 99-080028 | Metal Shaft |
| 99-080029 | Nylon Washer |
| 99-080030 | Spring |
| 99-080031 | Bellows |
| 99-080032 | Flat Steel Washer |
| 99-080033 | Plastic Guard/Actuator |
| 99-080036 | Top Plate |
| 99-080037 | Switch Mounting Plate |
| 99-080038 | Nylon Switch Actuator |

# C. Fluorescent Tube and Speaker



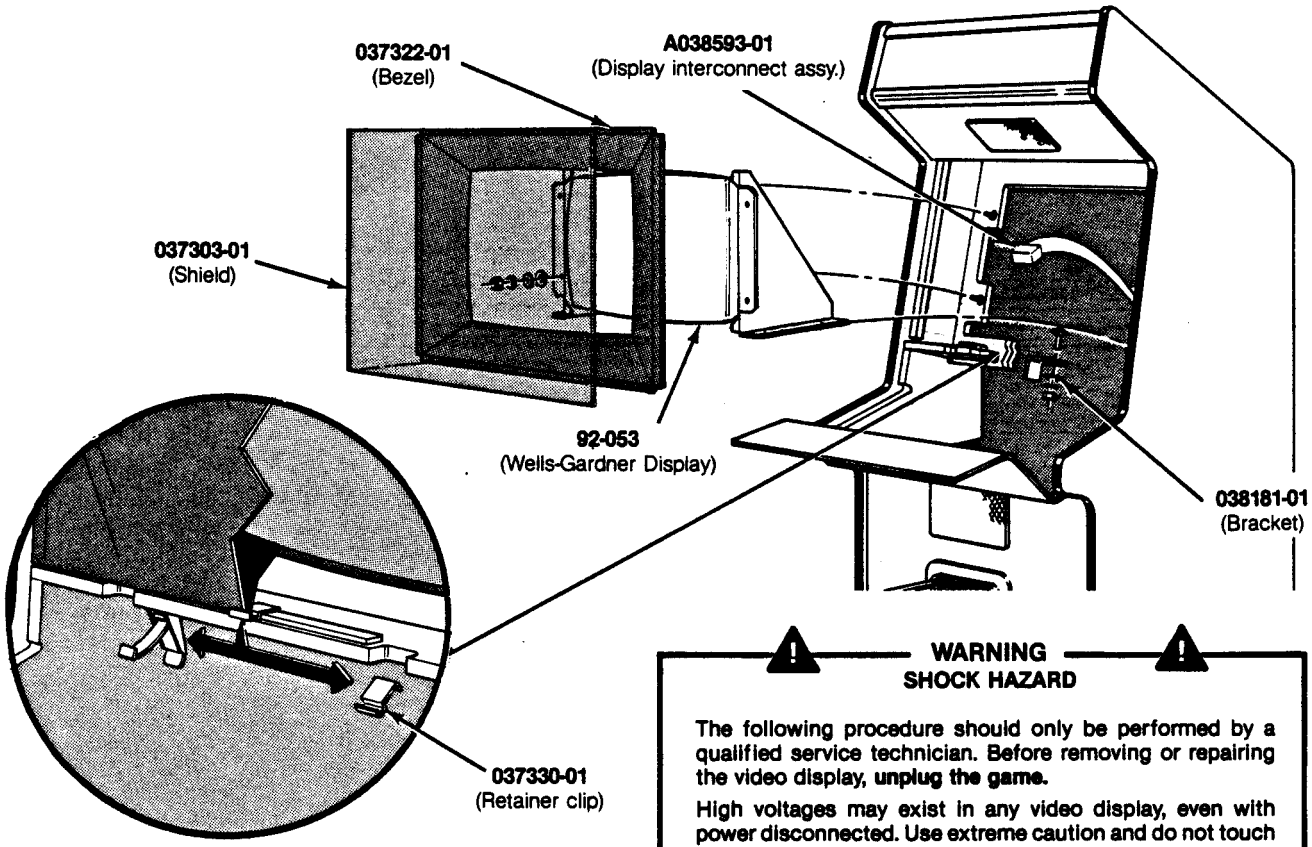

**NOTE**

To ensure that the fluorescent tube starts, make sure the ground wire is firmly attached to both the ballast transformer and the steel lamp bracket.

**Figure 3-4 Fluorescent Tube and Speaker A038161-01 & -02 A Parts List**

| *Part No.* | *Description* |
|---|---|
| A037457-01 | Tube and Speaker Harness Assembly |
| A037540-01 | Ground Wire with Ring Lug |
| 70-304 | 18-Inch, 15-W, Cool White Fluorescent Tube |
| 78-6900402 | Vinyl Foam Single-Coated Adhesive Tape, ¼-inch Wide x ⅛ inch Thick |
| 79-561816P | Spring-Connector Wire Nut for 16- to 18-Gauge Wires |
| 99-11003 | Fluorescent Lamp Starter |
| 99-11006 | Fluorescent Lamp Locking Tab *(tab consists of two pieces)* |
| 99-11009 | Starter Socket |
| 037304-01 | Bottom Attraction Glass Retainer |
| 037309-01 | Top Attraction Glass Retainer |
| 037469-01 | Steel Lamp Bracket |
| 038151-01 | 15-Inch Jumper Wire |
| 039977-01 | Attraction Glass with Graphics |
| 142028-001 | 60 Hz, 118 V, Ballast Transformer *(used on A038161-01 assembly)* |
| 142028-002 | 50 Hz, 118 V, Ballast Transformer *(used on A038161-02 assembly)* |
| 148001-017 | 6 x 9-Inch, 8Ω, 6-Ounce Oval Shielded High-Fidelity Speaker |
| 179035-001 | 2-Pin Fluorescent Lampholder |

# D. Video Displays




**WARNING**
**SHOCK HAZARD**

The following procedure should only be performed by a qualified service technician. Before removing or repairing the video display, **unplug the game.**

High voltages may exist in any video display, even with power disconnected. Use extreme caution and do not touch electrical parts of the display yoke area with your hands or with metal objects in your hands!

Discharge the high voltage from the cathode-ray tube as follows:

Attach one end of a large, well-insulated, 18-gauge jumper to ground. Momentarily touch the free end of the grounded jumper to the anode by sliding it under the anode cap. Wait two minutes and discharge the anode again.

**IMPLOSION HAZARD**

If you drop the display and the picture tube breaks, *it will implode!* Shattered glass can fly six feet or more from the implosion. Use care when replacing any display.

**Figure 3-5 Wells-Gardner Video Display Parts List**

| *Part No.* | *Description* |
|---|---|
| A038593-01 | Wells-Gardner Interconnect Assembly |
| 92-053 | 19-Inch Wells-Gardner Color X-Y CRT |
| 038181-01 | Video Display Support Bracket |
| 037303-01 | Display Shield |
| 037322-01 | Display Bezel |
| 037330-01 | Display Shield Retainer Clip |
| 038184-01 | Static Shield |

**WARNING**
**SHOCK HAZARD**

The following procedure should only be performed by a qualified service technician. Before removing or repairing the video display, **unplug the game.**

High voltages may exist in any video display, even with power disconnected. Use extreme caution and do not touch electrical parts of the display yoke area with your hands or with metal objects in your hands!

Discharge the high voltage from the cathode-ray tube as follows:

Attach one end of a large, well-insulated, 18-gauge jumper to ground. Momentarily touch the free end of the grounded jumper to the anode by sliding it under the anode cap. Wait two minutes and discharge the anode again.

**IMPLOSION HAZARD**

If you drop the display and the picture tube breaks, *it will implode!* Shattered glass can fly six feet or more from the implosion. Use care when replacing any display.

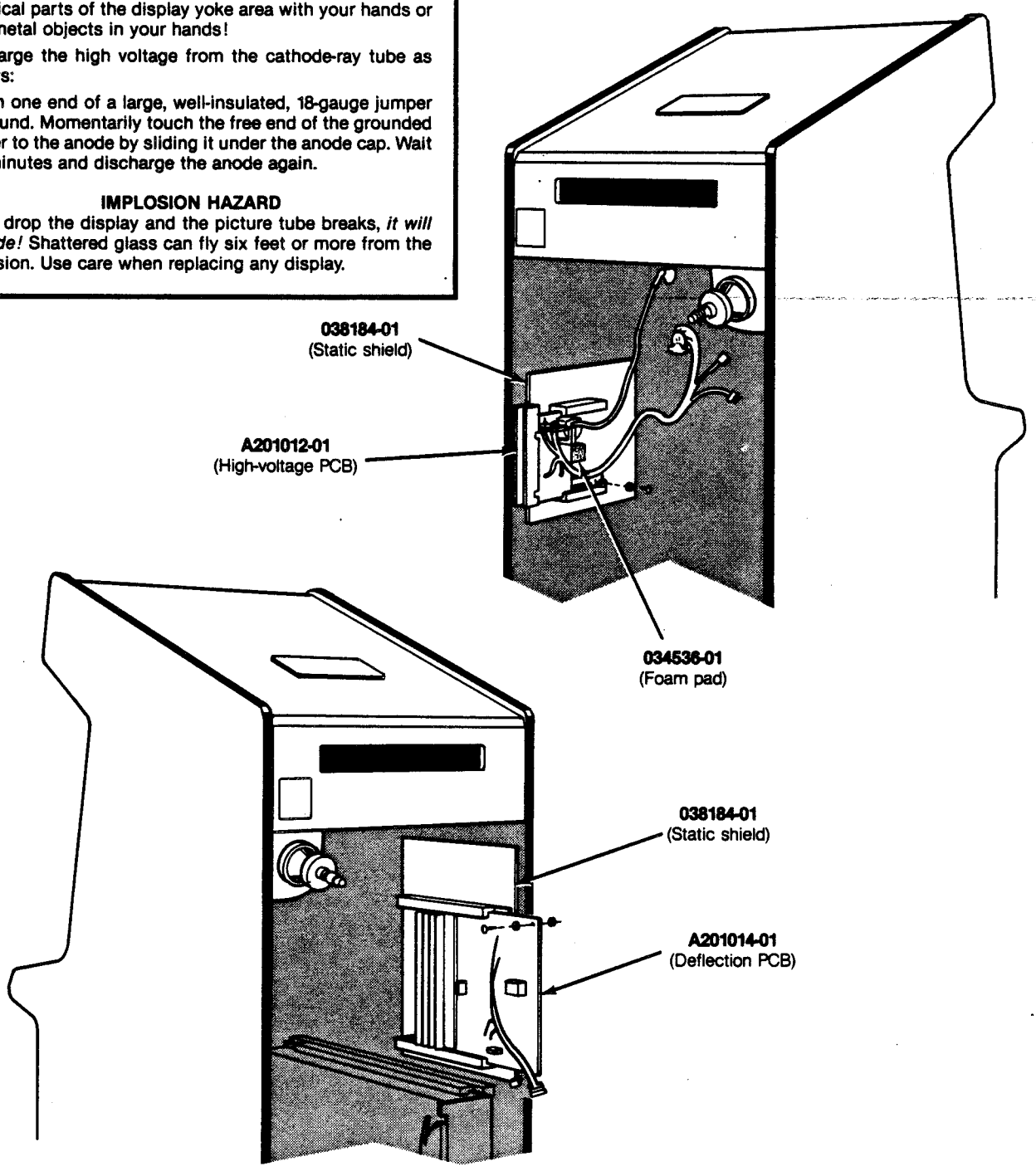
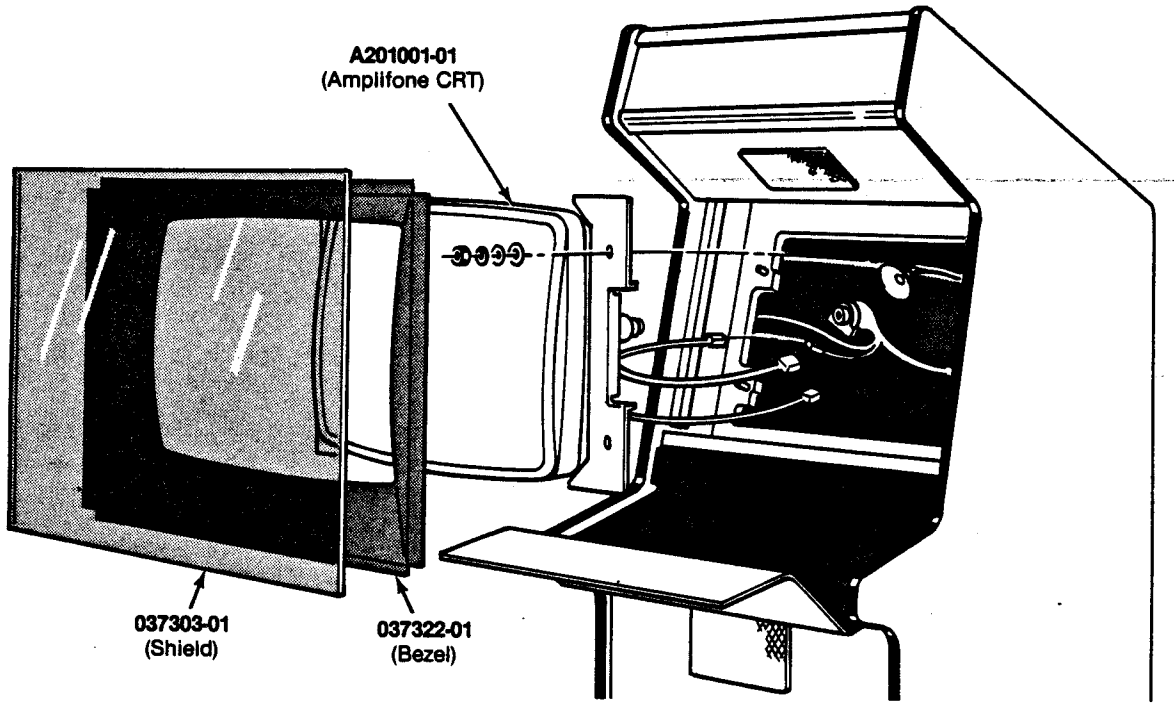



**Figure 3-6 Amplifone Video Display**

**NOTE**

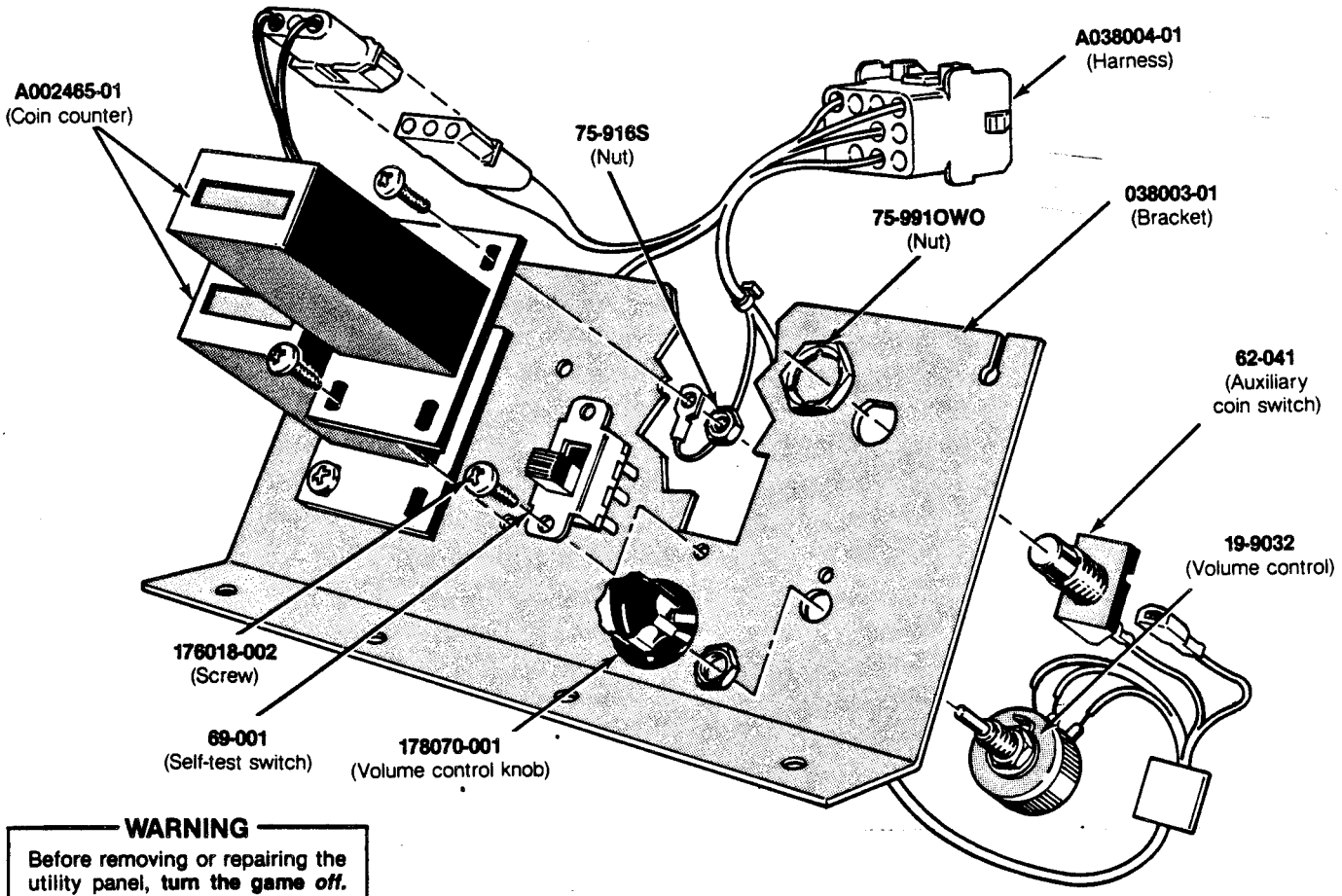
**Amplifone CRT (A201001-01) and Deflection PCB (A201014-01) are shipped as a matched, calibrated pair and should be used as such.**




## Figure 3-6 Amplifone Video Display Parts List

| *Part No.* | *Description (Reference Designations and Locations in Bold)* |
|---|---|
| | ***Amplifone Display Assembly A200000-01*** |
| A201001-01 | 19-Inch Amplifone Color X-Y CRT |
| A201012-01 | High-Voltage PCB |
| A201014-01 | Deflection PCB |
| 034536-02 | Foam Pad *(used with High-Voltage and Deflection PCBs)* |
| 037303-01 | Display Shield |
| 037322-01 | Display Bezel |
| 037330-01 | Display Shield Retainer Clip |
| 038184-01 | Static Shield |

# E. Utility Panel Assembly




**WARNING**

Before removing or repairing the utility panel, **turn the game *off.*** Players may receive an electrical shock if the utility panel is not properly grounded! After servicing any parts on the panel, make sure that the ground wire is firmly attached to the metal screw on the back of the coin counter.

**Figure 3-7 Utility Panel Assembly**

**Parts List**

| *Part No.* | *Description* |
|---|---|
| A002465-01 | 6 V Coin Counter |
| A038004-01 | Utility Panel Harness |
| 19-9032 | Volume Control |
| 62-041 | SPDT Momentary-Contact Pushbutton Auxiliary Coin Switch with Black Cap |
| 69-001 | DPDT Self-Test Switch |
| 75-916S | #6-32 Standard Machine Nut |
| 038003-01 | Utility Panel |
| 75-9910W0 | 15/32-32 Stamped Nut |
| 176018-002 | #6-32 x ½-Inch Pan Head Machine Screw |
| 178070-001 | Volume Control Knob |

# F. Coin Door Assemblies

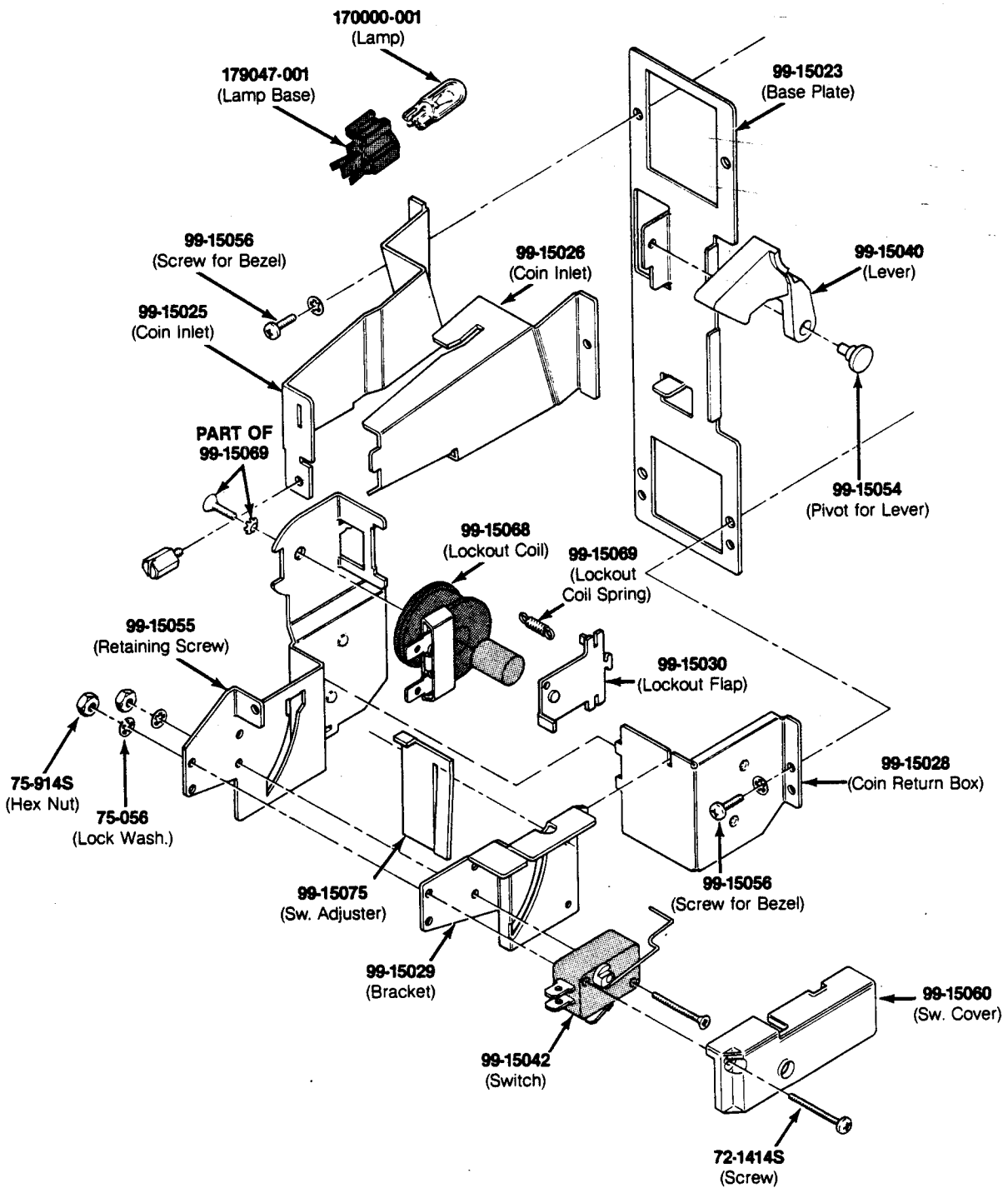
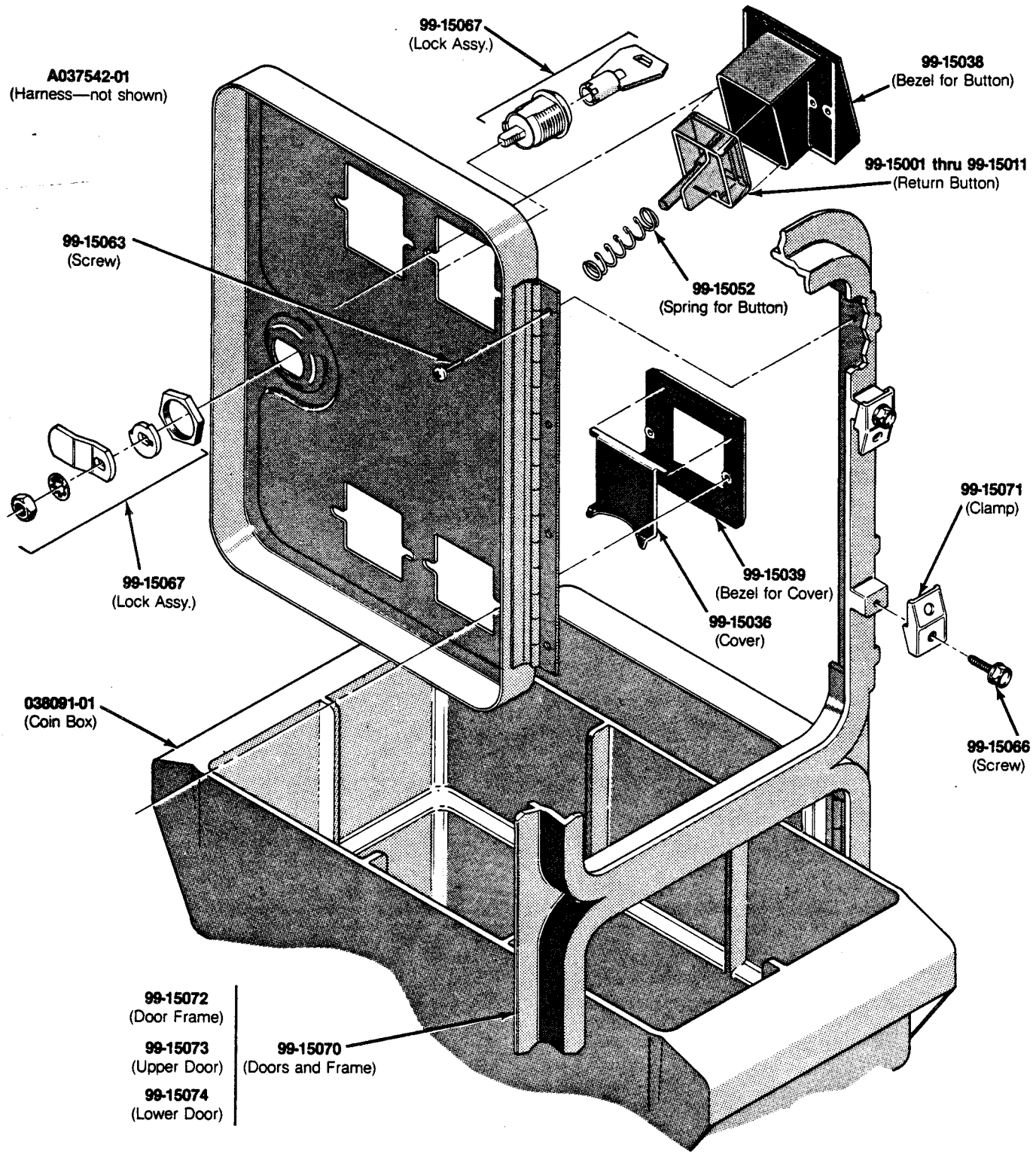



**Figure 3-8 Vertically Mounted Coin Door A037619-xxx D**




A037619-01 — U.S. 25¢/25¢ Coin Door
A037619-02 — U.S. 50¢/50¢ Coin Door
A037619-03 — Canadian 25¢/25¢ Coin Door
A037619-04 — British 10 P/10 P Coin Door
A037619-05 — British 10 P/50 P Coin Door
A037619-06 — British 20 P/50 P Coin Door
A037619-07 — Australian 20¢/20¢ Coin Door
A037619-08 — German 1 DM/1 DM Coin Door
A037619-09 — German 2 DM/1 DM Coin Door
A037619-10 — German 2 DM/5 DM Coin Door
A037619-11 — German 1 DM/5 DM Coin Door
A037619-12 — 5 Fr/5 Fr Coin Door
A037619-13 — Swiss 1 Fr/1 Fr Coin Door
A037619-14 — French 1 Fr/1 Fr Coin Door
A037619-15 — French 2 Fr/1 Fr Coin Door
A037619-16 — Swedish 1 Kr/1 Kr Coin Door
A037619-17 — Spanish 25 Pts/25 Pts Coin Door
A037619-18 — Italian 100 L/100 L Coin Door
A037619-19 — Hong Kong $1/$1 Coin Door
A037619-20 — Japanese 100Y/100Y Coin Door

**Figure 3-8 Vertically Mounted Coin Door, continued**
**A037619-xxx D**

# Vertically Mounted Coin Door
# Parts List

| *Part No.* | *Description* |
|---|---|
| A037542-01 | Harness Assembly |
| 72-1414S | #4-40 × 7/8-Inch Cross-Recessed Pan-Head Steel Machine Screw |
| 75-056 | #6 Internal-Tooth Zinc-Plated Steel Lock Washer |
| 75-914S | #4-40 Steel Machine Hex Nut |
| 75-3414S | #4-40 × 7/8-Inch 82° Cross-Recessed Flat-Head Steel Machine Screw |
| 99-15001 | Coin Return Button with U.S. 25¢ Price Plate |
| 99-15002 | Coin Return Button with U.S. $1 Price Plate |
| 99-15003 | Coin Return Button with German 1 DM Price Plate |
| 99-15004 | Coin Return Button with German 2 DM Price Plate |
| 99-15005 | Coin Return Button with German 5 DM Price Plate |
| 99-15006 | Coin Return Button with Belgian 5 Fr Price Plate |
| 99-15007 | Coin Return Button with French 1 Fr Price Plate |
| 99-15008 | Coin Return Button with Japanese 100 Yen Price Plate |
| 99-15009 | Coin Return Button with British 10 Pence Price Plate |
| 99-15010 | Coin Return Button with Australian 20¢ Price Plate |
| 99-15011 | Coin Return Button with Italian 100 Lire Price Plate |
| 99-15023 | Base Plate |
| 99-15025 | Left Half of Coin Inlet |
| 99-15026 | Right Half of Coin Inlet |
| 99-15027 | Side Plate of Coin Return Box |
| 99-15028 | Base Plate of Coin Return Box |
| 99-15029 | Switch Bracket |
| 99-15030 | Flap for Lockout Coil *(U.S. 25¢)* |
| 99-15036 | Metal Coin Return Cover |
| 99-15038 | Bezel for Coin Return Button |
| 99-15039 | Metal Bezel for Coin Return Cover |
| 99-15040 | Coin Return Lever |
| 99-15042 | Coin Switch for U.S. 25¢ |
| 99-15052 | Spring for Coin Return Button |
| 99-15054 | Pivot for Coin Return Lever |
| 99-15055 | Retaining Screw |
| 99-15056 | #4-40 × 5/16-Inch Cross-Recessed Pan-Head Steel Machine Screw |
| 99-15060 | Switch Cover |
| 99-15063 | Screw for Hinge |
| 99-15066 | Screw for Clamp |
| 99-15067 | Lock Assembly |
| 99-15068 | Lockout Coil |
| 99-15069 | Spring for Lockout Coil |
| 99-15070 | Doors and Frame |
| 99-15071 | Clamp for Frame |
| 99-15072 | Door Frame |
| 99-15073 | Upper Door |
| 99-15074 | Lower Door |
| 99-15075 | Switch Adjuster |
| 038091-01 | Coin Box *(Not included in assembly) Acceptable substitute is part number A037491-01* |
| 170000-001 | 6.3V Miniature Wedge-Base Incandescent Lamp |
| 171006-035 | Metal Coin Mechanism |
| 179047-001 | Lamp Base |

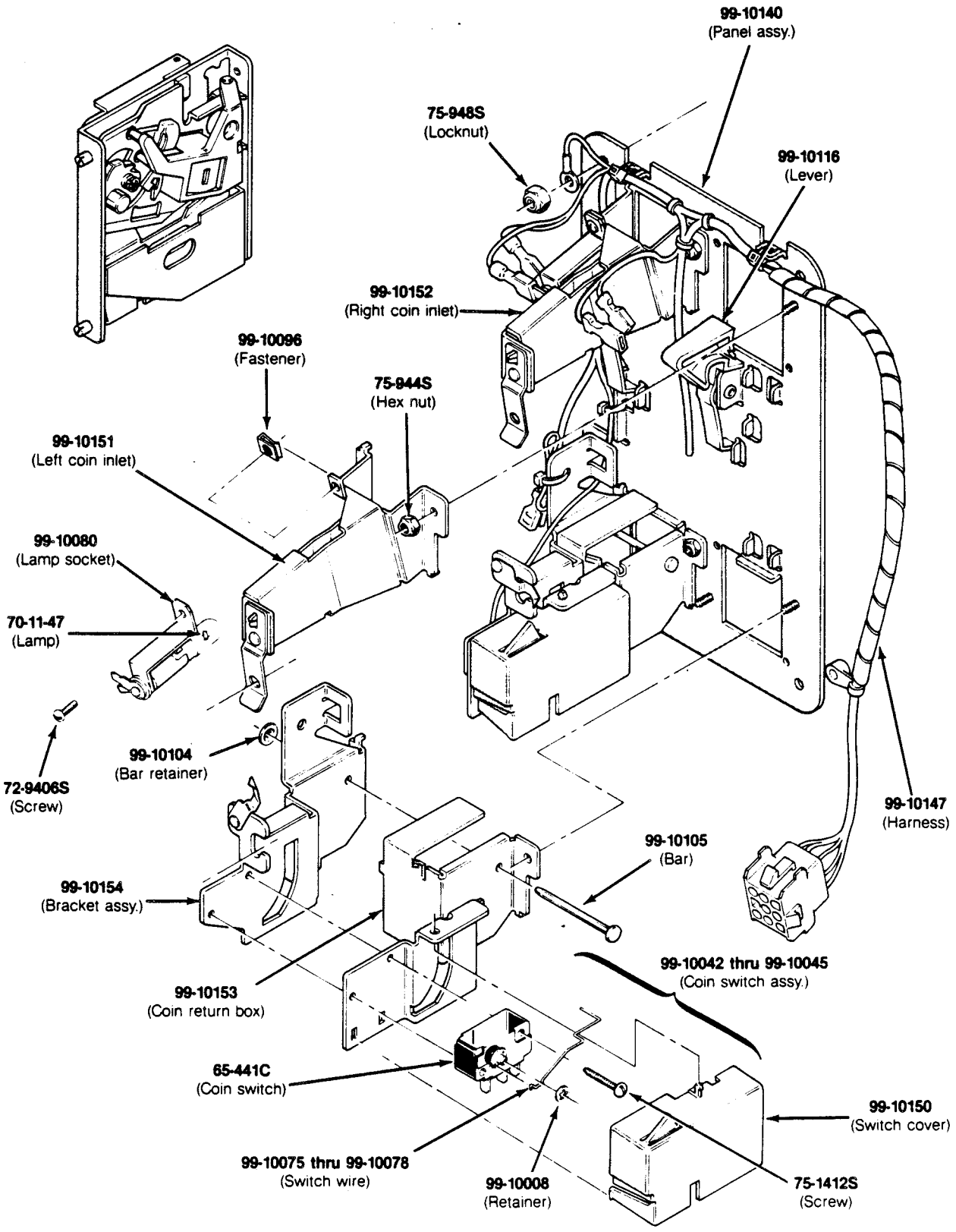



**Figure 3-9 American-Made Coin Door Assembly 171027-001 A**

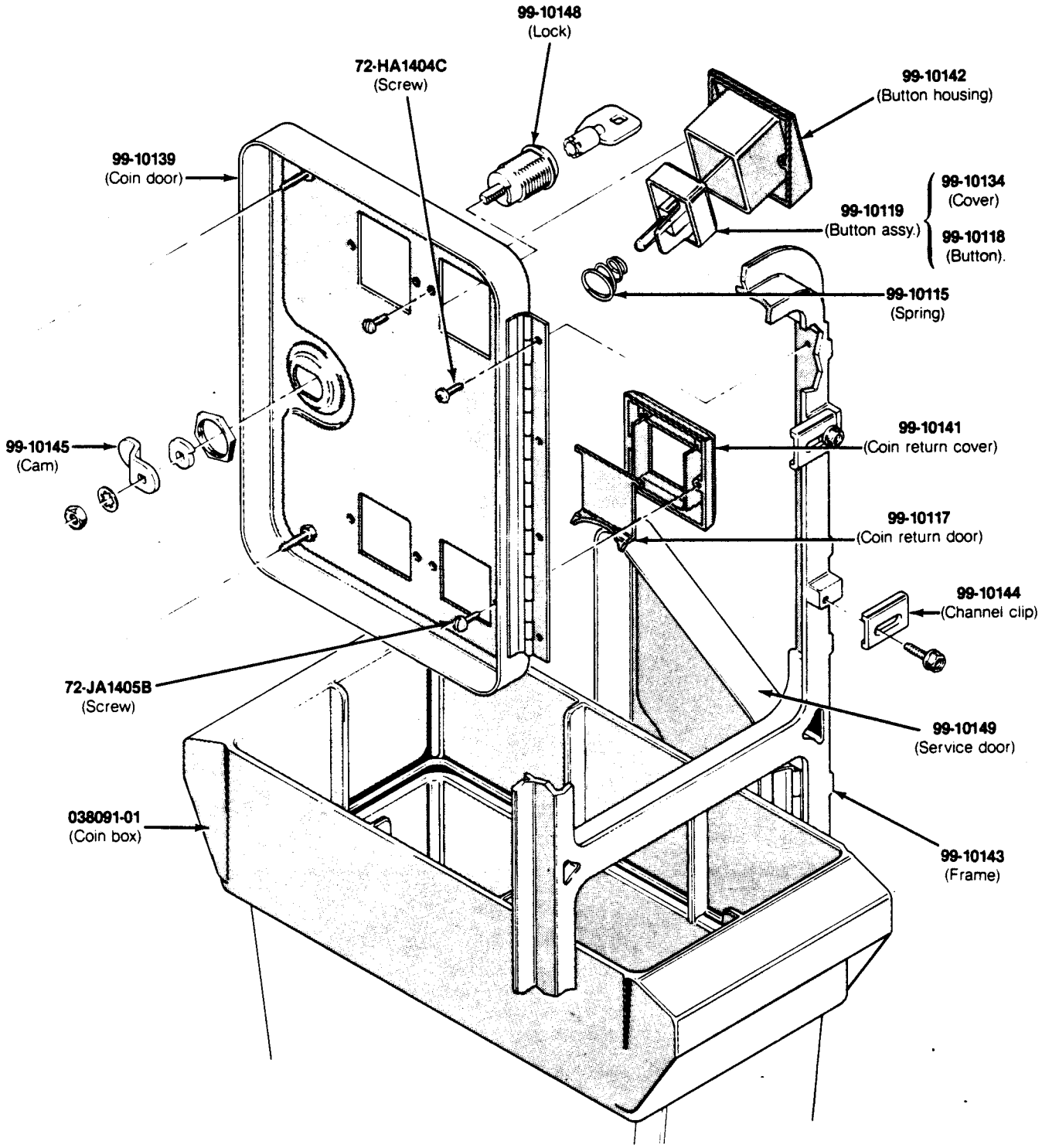



**Figure 3-9 American-Made Coin Door Assembly, continued**
**171027-001 A**

# American-Made Coin Door Assembly
# Parts List

| *Part No.* | *Description* |
|---|---|
| 171006-035 | Metal Coin Mechanism for U.S. $.25 |
| 65-441C | Coin Switch |
| 70-11-47 | Miniature Bayonet Lamp |
| 72-9406S | #4-40 x⅜-Inch Truss-Head Screw |
| 72-HA1404C | #4-40 x ¼-Inch Pan-Head Screw |
| 72-JA1405B | #4-40 x .31-Inch Pan-Head Screw |
| 75-1412S | #4-40 x ¾-Inch Pan-Head Screw |
| 75-944S | #4-40 Locknut |
| 99-10008 | Retainer |
| 99-10042 | Coin Switch Assembly for Belgian 5 Fr and U.S. $.25 |
| 99-10043 | Coin Switch Assembly for German 1 DM, Japanese 100 Yen, Swiss 1 Fr |
| 99-10044 | Coin Switch Assembly for German 2 DM, Italian 100 L, U.S. $1.00 |
| 99-10045 | Coin Switch Assembly for Australian $.20, German 5 DM, British 10 P |
| 99-10068 | Coin Return Chute |
| 99-10075 | Switch wire (included in coin switch assembly) |
| 99-10076 | Switch wire (included in coin switch assembly) |
| 99-10077 | Switch wire (included in coin switch assembly) |
| 99-10078 | Switch wire (included in coin switch assembly) |
| 99-10080 | Lamp socket |
| 99-10081 | Key holder |
| 99-10096 | Fastener |
| 99-10104 | Bar retainer |
| 99-10105 | Bar |
| 99-10115 | Spring |
| 99-10116 | Plastic Coin Return Lever |
| 99-10117 | Steel Coin Return Door |
| 99-10118 | Amber Coin Return Button |
| 99-10119 | Amber Coin Button for U.S. $.25 |
| 99-10134 | Coin Button Cover |
| 99-10139 | Coin Door |
| 99-10140 | Coin Door Inner-Panel Assembly |
| 99-10141 | Diecast Coin Return Cover |
| 99-10142 | Diecast Button Housing |
| 99-10143 | Coin Door Frame |
| 99-10144 | Coin Door Channel Clip |
| 99-10145 | Offset Cam |
| 99-10146 | Coin Inlet Chute Assembly |
| 99-10147 | American-Made Coin Door Harness |
| 99-10148 | Lock Assembly |
| 99-10149 | Service Door |
| 99-10150 | Switch Cover |
| 99-10151 | Left Coin Inlet |
| 99-10152 | Right Coin Inlet |
| 99-10153 | Coin Return Box |
| 99-10154 | Bracket Assembly |

# G. Power Supply Assembly

**WARNING**

Fuse cover must be in place during game operation.

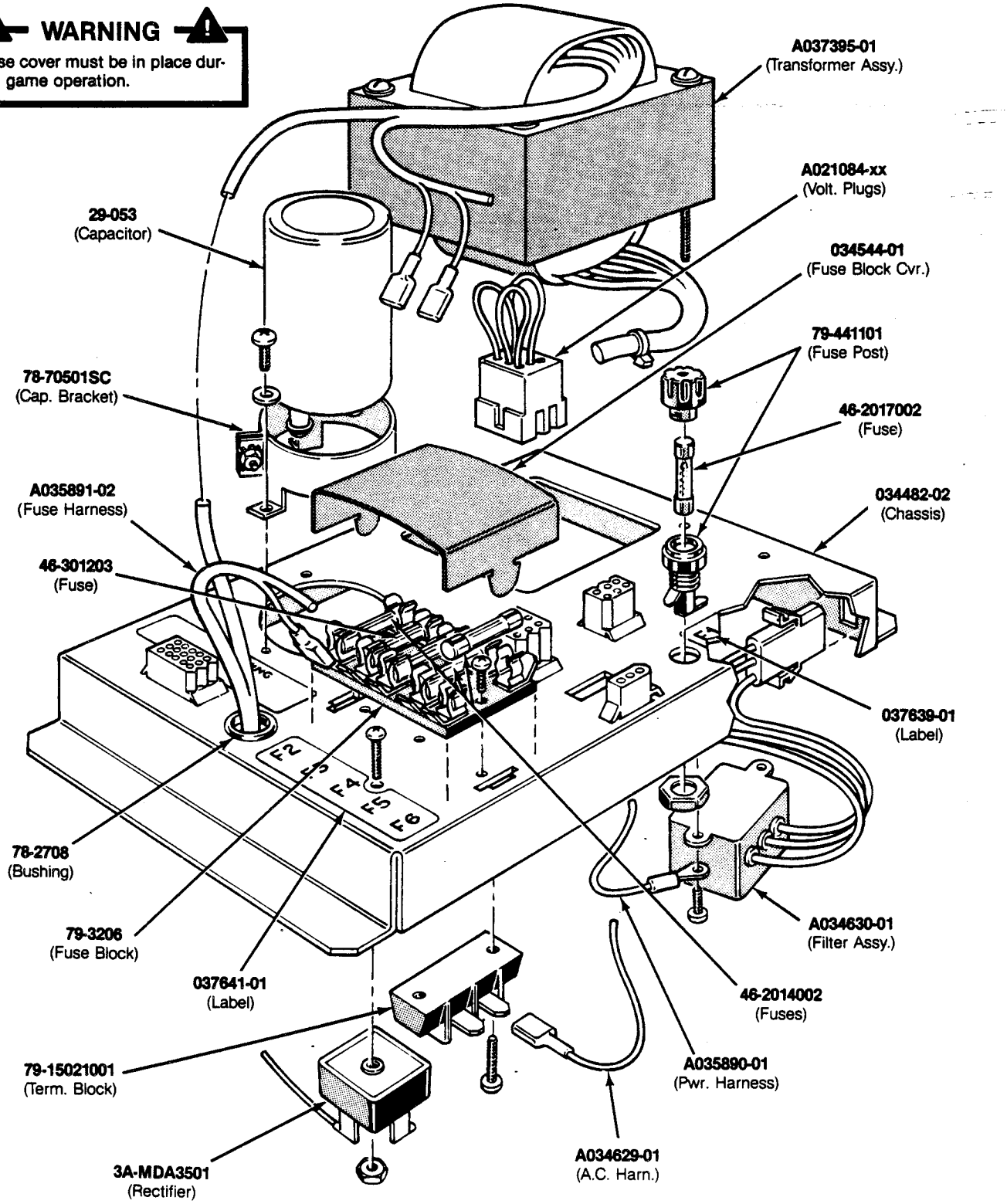



**Figure 3-10 Color X-Y Power Supply Assembly A037396-xx D**

# Color X-Y Power Supply Assembly Parts List

| *Part No.* | *Description (Reference Designations in Bold)* |
|---|---|
| A021084-01 | Voltage Plug for 100 V *(violet)* |
| A021084-02 | Voltage Plug for 120 V *(yellow)* |
| A021084-04 | Voltage Plug for 220 V *(blue)* |
| A021084-05 | Voltage Plug for 240 V *(brown)* |
| A034629-01 | AC Harness Assembly |
| A034630-01 | RFI Filter Assembly **(FL1)** |
| A035890-01 | Power Harness Assembly |
| A035891-02 | Fuse Harness Assembly |
| A037395-01 | Color X-Y Transformer Assembly **(T1)** |
| 29-053 | 27,000 µF 15 VDC Electrolytic Capacitor **(C1)** |
| 3A-MDA3501 | Type-MDA 3501 Bridge Rectifier **(CR1)** |
| 46-2014002 | 4 A, 250 V, 3AG Slow-Blow Glass Cartridge-Type Fuse **(F2, F4–F6)** |
| 46-2017002 | 7 A, 250 V, 3AG Slow-Blow Glass Cartridge-Type Fuse **(F1)** |
| 46-301203 | 20 A, 32 V, 3AG Slow-Blow Glass Cartridge-Type Fuse **(F3)** |
| 78-2708 | Nylon Type 6/6 Hole Bushing with ⅝-Inch Inside Diameter × $^{55}/_{64}$-Inch Outside Diameter × ¼-Inch Thick |
| 78-70501SC | 2-Inch Diameter Capacitor Mounting Bracket |
| 79-15021001 | 2-Circuit Single-Row Terminal Block |
| 79-3206 | 5-Position 3AG Fuse Block with ¼-Inch Quick-Disconnect Terminals |
| 79-441101 | Panel-Mounting Non-Indicating 3AG Cartridge-Type Fuse Post |
| 034482-02 | Power Supply Chassis Base |
| 034544-01 | Fuse Block Cover |
| 037243-01 | Metal Base Plate *(not shown in illustration)* |
| 037639-01 | Label for Fuse Value **(F1)** |
| 037641-01 | Label for Fuse Values **(F2–F6)** |

**NOTE**

**A037396-01 power supply assembly has the 120 V plug**
**A037396-02 has the 100 V, 220 V, and 240 V plugs**
**A037396-03 has the 220 V and 240 V plugs**

| Line Voltage Range | Voltage Selection Plug Wire Color |
|---|---|
| 90-110 VAC (100) | Violet |
| 105-135 VAC (120) | Yellow |
| 200-240 VAC (220) | Blue |
| 220-260 VAC (240) | Brown |

# H. Printed-Circuit Boards

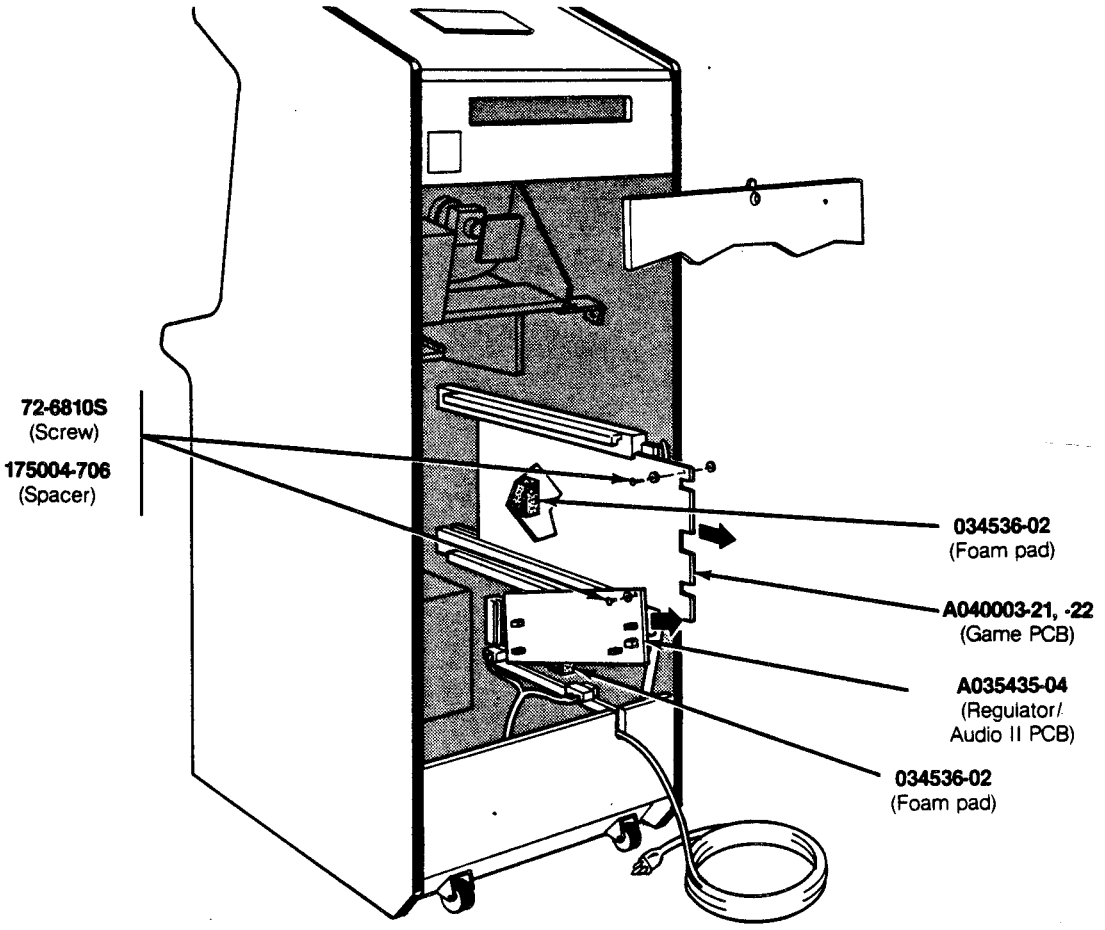



**Figure 3-11 PCB Mounting Hardware Parts List**

| *Part No.* | *Description* |
|---|---|
| 72-6810S | #8 x ⅝-Inch Phillips-Head Screw (secures PCB to cabinet) |
| 175004-706 | #8 Spacer (secures PCB to cabinet) |
| 034536-02 | Foam Pad |

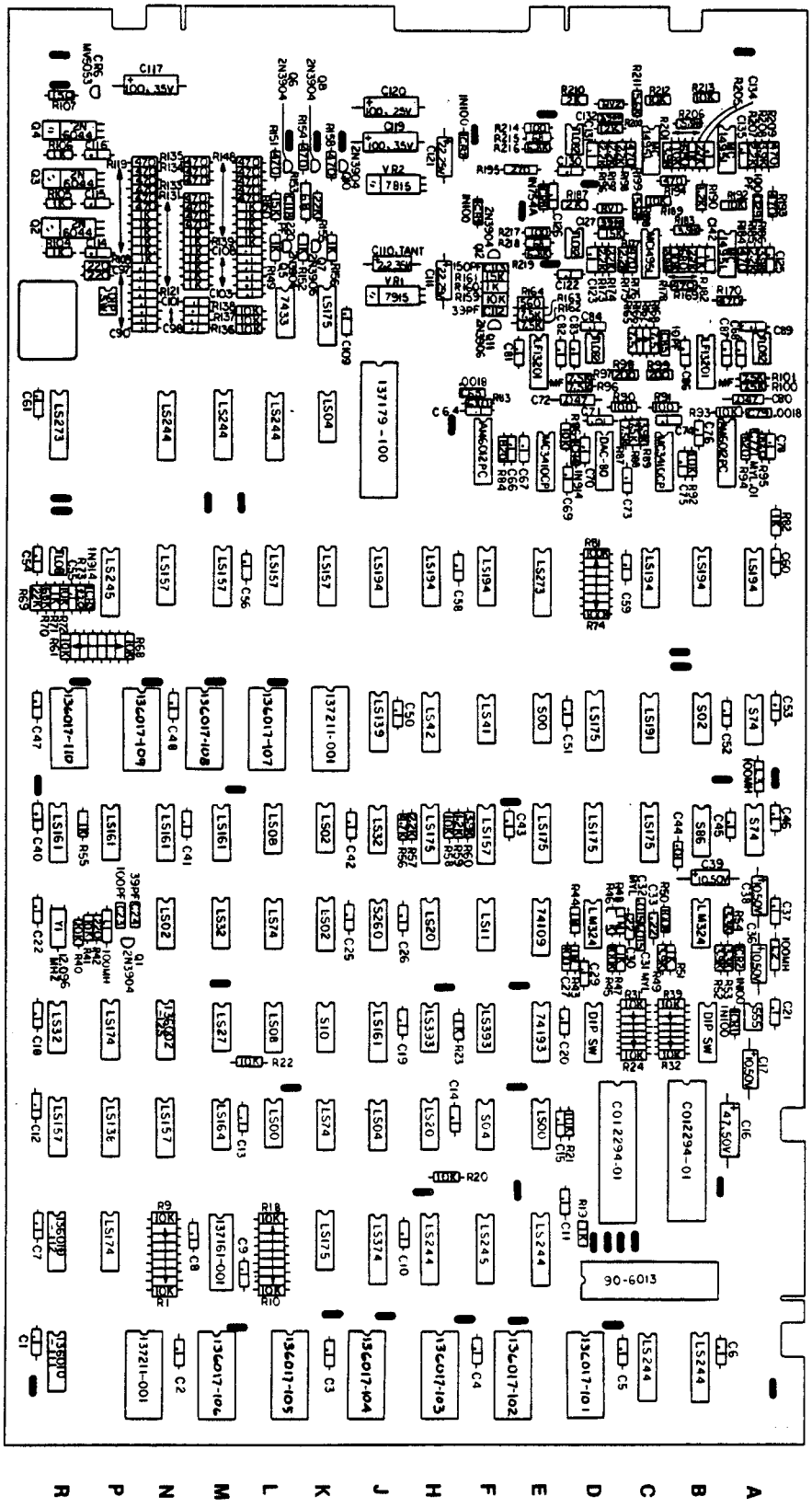



**Figure 3-12 Black Widow Game Printed-Circuit Board Assembly**

# Black Widow Printed-Circuit Board Assembly Parts List

| *Designator* | *Description* | *Part No.* |
|---|---|---|
| | **Capacitors** | |
| C1–C15 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C16 | 47 μF, 50 V Aluminum Electrolytic Fixed Axial-Lead Capacitor | 24-500476 |
| C17 | 10 μF, 50 V Aluminum Electrolytic Fixed Axial-Lead Capacitor | 24-500106 |
| C18–C22 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C23 | 100 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor | 128002-101 |
| C24 | 39 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor | 128002-390 |
| C25, C26 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C27 | 100 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor | 128002-101 |
| C29 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C30 | 0.22 μF, 25 V, Ceramic-Disc Radial-Lead Capacitor | 122008-224 |
| C31, C32 | 0.015 μF, ± 10%, 100 V Radial-Lead Epoxy-Dipped Mylar Capacitor | 21-101153 |
| C33 | 0.22 μF, 25 V, Ceramic-Disc Radial-Lead Capacitor | 122008-224 |
| C35 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C36 | 10 μF, 50 V Aluminum Electrolytic Fixed Axial-Lead Capacitor | 24-500106 |
| C37 | 0.1 μF, 50 V Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C38, C39 | 10 μF, 50 V Aluminum Electrolytic Fixed Axial-Lead Capacitor | 24-500106 |
| C40–C43 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C44 | 0.01 μF, 25 V, Ceramic-Disc Radial-Lead Capacitor | 122005-103 |
| C45–C63 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C64 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C65 | 0.0018 μF, ± 10%, 1 kV, Ceramic-Disc Radial-Lead Capacitor | 27-102182 |
| C66 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C67 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C69 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C70 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C71 | 0.01 μF, 25 V, Ceramic-Disc Radial-Lead Capacitor | 122005-103 |
| C72 | 0.047 μF, ± 10%, 50 V, Axial-Lead Epoxy-Dipped Polycarbonate Capacitor | 122010-473 |
| C73–C75 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C76 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C77 | 0.01 μF, ± 10%, 100 V, Radial-Lead Epoxy-Dipped Capacitor | 21-101103 |
| C78 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C79 | 0.0018 μF, ± 10%, 1 kV Radial-Lead Ceramic-Disc Capacitor | 27-102182 |
| C80 | 0.047 μF, ± 10%, 50 V, Axial-Lead Epoxy-Dipped Polycarbonate Capacitor | 122010-473 |
| C81–C84 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C85 | 10 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor | 128002-100 |
| C86–C101 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C103–C109 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C110 | 2.2 μF, ± 10%, 35 V Tantalum Capacitor | 122000-225 |
| C111 | 22 μF, 25 V Electrolytic Fixed Axial-Lead Capacitor | 24-250226 |
| C112 | 39 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor | 128002-390 |
| C113 | 150 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor | 128002-151 |

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# Black Widow Game Printed-Circuit Board Assembly Parts List, continued

| Designator | Description | Part No. |
|---|---|---|
| C114-C116 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C117 | 100 μF, 35 V Aluminum Electrolytic Fixed Axial-Lead Capacitor | 24-350107 |
| C118 | 220 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor | 128002-221 |
| C119, C120 | 100 μF, 35 V Aluminum Electrolytic Fixed Axial-Lead Capacitor | 24-350107 |
| C121 | 22 μF, 25 V Electrolytic Fixed Axial-Lead Capacitor | 24-250226 |
| C122-C126 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C127 | 39 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor | 128002-390 |
| C129 | 100 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor | 128002-101 |
| C130, C131 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| C132 | 39 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor | 128002-390 |
| C134, C135 | 0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor | 122002-104 |
| | **Diodes** | |
| CR1, CR2 | Type-1N100, 100 V Switching Diode | 31-1N100 |
| CR3, CR4 | Type-1N914, 75 V Switching Diode | 31-1N914 |
| CR5 | Type-1N100, 100 V Switching Diode | 31-1N100 |
| CR6 | Type-MV5053 Light-Emitting Diode | 38-MV5053 |
| CR7 | Type-1N100, 100 V Switching Diode | 31-1N100 |
| CR8 | Type-1N754A, 6.8 V Zener Diode | 131002-001 |
| | **Inductors** | |
| L1-L3 | 100 μH, ± 10%, Hot-Molded Plastic Fixed R.F. Choke (Acceptable substitute is part no. 41-3003) | 141002-001 |
| | **Integrated Circuits** | |
| A4 | Type-555 Integrated Circuit | 37-555 |
| A6, A7 | Type-74S74 Integrated Circuit | 37-74S74 |
| A8 | Type-74LS194 Integrated Circuit | 37-74LS194 |
| A10 | Type-TL082 Integrated Circuit | 37-TL082CP |
| A/B9 | 12-Bit Digital-to-Analog Converter | 137158-002 |
| A/B11 | Type-MC1495L Integrated Circuit | 37-1495 |
| A/B12 | Type-MC1495L Integrated Circuit | 37-1495 |
| B1 | Type-74LS244 Integrated Circuit | 37-74LS244 |
| B3 | Audio I/O N-Channel MOS/LSI Custom Chip | C012294-01 |
| B5 | Type-LM324 Integrated Circuit | 37-LM324 |
| B6 | Type-74S86 Integrated Circuit | 137002-001 |
| B7 | Type-74S02 Integrated Circuit | 37-74S02 |
| B8 | Type-74LS194 Integrated Circuit | 37-74LS194 |
| B10 | Type-LF13201 Integrated Circuit | 37-13201 |
| C1 | Type-74LS244 Integrated Circuit | 37-74LS244 |
| C2 | Microprocessor | 90-6013 |
| C6 | Type-74LS175 Integrated Circuit | 37-74LS175 |
| C7 | Type-74LS191 Integrated Circuit | 37-74LS191 |
| C8 | Type-74LS194 Integrated Circuit | 37-74LS194 |
| C9 | 10-Bit Digital-to-Analog Converter | 137160-003 |

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## Black Widow Game Printed-Circuit Board Assembly Parts List, continued

| *Designator* | *Description* | *Part No.* |
|---|---|---|
| C11, C12 | Type-MC1495L Integrated Circuit | 37-1495 |
| C/D3 | Audio I/O N-Channel MOS/LSI Custom Chip | C012294-01 |
| D5 | Type-LM324 Integrated Circuit | 37-LM324 |
| D6, D7 | Type-74LS175 Integrated Circuit | 37-74LS175 |
| D9 | 8-Bit Digital-to-Analog Converter | 137159-001 |
| D10 | Type-TL082 Integrated Circuit | 37-TL082CP |
| D/E11, D/E12 | Type-TL082 Integrated Circuit | 37-TL082CP |
| E2 | Type-74LS244 Integrated Circuit | 37-74LS244 |
| E3 | Type-74LS00 Integrated Circuit | 37-74LS00 |
| E4 | Type-74193 Integrated Circuit | 37-74193 |
| E5 | Type-74109 Integrated Circuit | 37-74109 |
| E6 | Type-74LS175 Integrated Circuit | 37-74LS175 |
| E7 | Type-74S00 Integrated Circuit | 37-74S00 |
| E8 | Type-74LS273 Integrated Circuit | 37-74LS273 |
| E9 | 10-Bit Digital-to-Analog Converter | 137160-003 |
| E10 | Type-LF13201 Integrated Circuit | 37-13201 |
| F2 | Type-74LS245 Integrated Circuit | 37-74LS245 |
| F3 | Type-74S04 Integrated Circuit | 37-74S04 |
| F4 | Type-74LS393 Integrated Circuit | 37-74LS393 |
| F5 | Type-74LS11 Integrated Circuit | 137149-001 |
| F6 | Type-74LS157 Integrated Circuit | 37-74LS157 |
| F7 | Type-74LS14 Integrated Circuit | 37-74LS14 |
| F8 | Type-74LS194 Integrated Circuit | 37-74LS194 |
| F9 | 12-Bit Digital-to-Analog Converter | 137158-002 |
| H2 | Type-74LS244 Integrated Circuit | 37-74LS244 |
| H3 | Type-74LS20 Integrated Circuit | 37-74LS20 |
| H4 | Type-74LS393 Integrated Circuit | 37-74LS393 |
| H5 | Type-74LS20 Integrated Circuit | 37-74LS20 |
| H6 | Type-74LS175 Integrated Circuit | 37-74LS175 |
| H7 | Type-74LS42 Integrated Circuit | 37-74LS42 |
| H8 | Type-74LS194 Integrated Circuit | 37-74LS194 |
| J2 | Type-74LS374 Integrated Circuit | 37-74LS374 |
| J3 | Type-74LS04 Integrated Circuit | 37-74LS04 |
| J4 | Type-74LS161 Integrated Circuit | 37-74LS161 |
| J5 | Type-74S260 Integrated Circuit | 37-74S260 |
| J6 | Type-74LS32 Integrated Circuit | 37-74LS32 |
| J7 | Type-74LS139 Integrated Circuit | 37-74LS139 |
| J8 | Type-74LS194 Integrated Circuit | 37-74LS194 |
| J9 | Vector Generator | 137179-001 |
| K2 | Type-74LS175 Integrated Circuit | 37-74LS175 |
| K3 | Type-74LS74 Integrated Circuit | 37-74LS74 |
| K4 | Type-74S10 Integrated Circuit | 137236-001 |
| K5, K6 | Type-74LS02 Integrated Circuit | 37-74LS02 |
| K8 | Type-74LS157 Integrated Circuit | 37-74LS157 |

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# Black Widow Game Printed-Circuit Board Assembly Parts List, continued

| *Designator* | *Description* | *Part No.* |
|---|---|---|
| K9 | Type-74LS04 Integrated Circuit | 37-74LS04 |
| K10 | Type-74LS175 Integrated Circuit | 37-74LS175 |
| L3 | Type-74LS00 Integrated Circuit | 37-74LS00 |
| L4 | Type-74LS08 Integrated Circuit | 37-74LS08 |
| L5 | Type-74LS74 Integrated Circuit | 37-74LS74 |
| L6 | Type-74LS08 Integrated Circuit | 37-74LS08 |
| L10 | Type-7433 Integrated Circuit | 37-7433 |
| M4 | Type-74LS27 Integrated Circuit | 37-74LS27 |
| M3 | Type-74LS164 Integrated Circuit | 37-74LS164 |
| M5 | Type-74LS32 Integrated Circuit | 37-74LS32 |
| M6 | Type-74LS161 Integrated Circuit | 37-74LS161 |
| M8 | Type-74LS157 Integrated Circuit | 37-74LS157 |
| M9 | Type-74LS244 Integrated Circuit | 37-74LS244 |
| N3 | Type-74LS157 Integrated Circuit | 37-74LS157 |
| N5 | Type-74LS02 Integrated Circuit | 37-74LS02 |
| N6 | Type-74LS161 Integrated Circuit | 37-74LS161 |
| N8 | Type-74LS157 Integrated Circuit | 37-74LS157 |
| N9 | Type-74LS244 Integrated Circuit | 37-74LS244 |
| P2 | Type-74LS174 Integrated Circuit | 37-74LS174 |
| P3 | Type-74LS138 Integrated Circuit | 137177-001 |
| P4 | Type-74LS174 Integrated Circuit | 37-74LS174 |
| P6 | Type-74LS161 Integrated Circuit | 37-74LS161 |
| P8 | Type-74LS245 Integrated Circuit | 37-74LS245 |
| R3 | Type-74LS157 Integrated Circuit | 37-74LS157 |
| R4 | Type-74LS32 Integrated Circuit | 37-74LS32 |
| R6 | Type-74LS161 Integrated Circuit | 37-74LS161 |
| R8 | Type-TL082 Integrated Circuit | 37-TL082CP |
| R9 | Type-74LS273 Integrated Circuit | 37-74LS273 |
| | **Miscellaneous** | |
| B4 | 8-Station Single-Throw, Dual-Inline-Package Bit Switch | 66-118P1T |
| D4 | 8-Station Single-Throw, Dual-Inline-Package Bit Switch | 66-118P1T |
| P10 | 4-Station Single-Throw, Dual-Inline-Package Bit Switch | 66-114P1T |
| VR1 | -15 V Voltage Regulator | 37-7915 |
| VR2 | + 15 V Voltage Regulator | 37-7815 |
| Y1 | 12.096 MHz, ±0.005% Crystal | 144000-001 |
| | Nylon Snap-In Fastener | 81-4302 |
| | Test Point (Acceptable substitute is part no. 020670-01) | 179051-002 |
| | **Read-Only Memories** | |
| D1 | Programmable Read-Only Memory | 136017-101 |
| E/F1 | Programmable Read-Only Memory | 136017-102 |
| H1 | Programmable Read-Only Memory | 136017-103 |
| J1 | Programmable Read-Only Memory | 136017-104 |

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# Black Widow Game Printed-Circuit Board Assembly Parts List, continued

| *Designator* | *Description* | *Part No.* |
|---|---|---|
| K/L1 | Programmable Read-Only Memory | 136017-105 |
| L7 | Programmable Read-Only Memory | 136017-107 |
| M1 | Programmable Read-Only Memory | 136017-106 |
| M2 | Electrically-Alterable Read-Only Memory | 137161-001 |
| M/N7 | Programmable Read-Only Memory | 136017-108 |
| N4 | Programmable Read-Only Memory | 136002-125 |
| N/P7 | Programmable Read-Only Memory | 136017-109 |
| R1 | Programmable Read-Only Memory | 136010-111 |
| R2 | Programmable Read-Only Memory | 136010-112 |
| R7 | Programmable Read-Only Memory | 136017-110 |
| | **Random-Access Memories** | |
| K7 | Random-Access Memory | 137211-001 |
| N/P1 | Random-Access Memory | 137211-001 |
| | **Resistors** | |
| R1-R18 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R19 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R20-R22 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R23 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R24-R41 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R42 | 220 kΩ, ±5%, ¼ W Resistor | 110000-221 |
| R43, R44 | 1 MΩ, ±5%, ¼ W Resistor | 110000-105 |
| R45 | 100 kΩ, ±5%, ¼ W Resistor | 110000-104 |
| R46 | 22 kΩ, ±5%, ¼ W Resistor | 110000-223 |
| R47 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R48 | 1 MΩ, ±5%, ¼ W Resistor | 110000-105 |
| R49 | 3.9 kΩ, ±5%, ¼ W Resistor | 110000-392 |
| R50 | 100 kΩ, ±5%, ¼ W Resistor | 110000-104 |
| R51 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R52 | 3.9 kΩ, ±5%, ¼ W Resistor | 110000-392 |
| R53, R54 | 3.3 kΩ, ±5%, ¼ W Resistor | 110000-332 |
| R55 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R56 | 4.7 kΩ, ±5%, ¼ W Resistor | 110000-472 |
| R57 | 2.2 kΩ, ±5%. ¼ W Resistor | 110000-222 |
| R58 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R59 | 1.2 kΩ, ±5%, ¼ W Resistor | 110000-122 |
| R60 | 3.9 kΩ, ±5%, ¼ W Resistor | 110000-392 |
| R61-R68 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R69 | 22 kΩ, ±5%, ¼ W Resistor | 110000-223 |
| R70 | 68 kΩ, ±5%, ¼ W Resistor | 110000-683 |
| R71 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R72 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R73 | 220 kΩ, ±5%, ¼ W Resistor | 110000-221 |

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# Black Widow Game Printed-Circuit Board Assembly Parts List, continued

| Designator | Description | Part No. |
|---|---|---|
| R74-R81 | 100 kΩ, ±5%, ¼ W Resistor | 110000-104 |
| R82 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R83 | 680 Ω, ±5%, ¼ W Resistor | 110000-681 |
| R84 | 820 Ω, ±5%, ¼ W Resistor | 110000-821 |
| R86 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R87, R88 | 7.5 kΩ, ±1%, ⅛ W Resistor | 110003-752 |
| R89 | 3.9 kΩ, ±5%, ¼ W Resistor | 110000-392 |
| R90, R91 | 100 Ω, ±5%, ¼ W Resistor | 110000-101 |
| R92, R93 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R94, R95 | 820 Ω, ±5%, ¼ W Resistor | 110000-821 |
| R96, R97 | 7.5 kΩ, ±1%, ⅛ W Resistor | 110003-752 |
| R98, R99 | 500 Ω Vertical PCB-Mounting Cermet Trimpot (Acceptable substitute is part no. 19-315501) | 119002-501 |
| R100, R101 | 7.5 kΩ, ±1%, ⅛ W Resistor | 110003-752 |
| R102, R103 | 220 kΩ, ±5%, ¼ W Resistor | 110000-221 |
| R104-R106 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R107 | 150 Ω, ±5%, ¼ W Resistor | 110000-151 |
| R108-R113 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R114-R119 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R121-R127 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R128-R131 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R133-R135 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R136-R138 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R139-R143 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R144-R148 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R149 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R150 | 15 kΩ, ±5%, ¼ W Resistor | 110000-153 |
| R151 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R153 | 68 Ω, ±5%, ¼ W Resistor | 110001-680 |
| R152 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R154 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R155 | 22 kΩ, ±5%, ¼ W Resistor | 110000-223 |
| R156 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R158 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R159 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R160 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R161 | 15 kΩ, ±5%, ¼ W Resistor | 110000-153 |
| R162, R163 | 7.5 kΩ, ±1%, ⅛ W Resistor | 110003-752 |
| R164 | 560 Ω, ±5%, ¼ W Resistor | 110000-561 |
| R165-R168 | 7.5 kΩ, ±1%, ⅛ W Resistor | 110003-752 |
| R169, R170 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R173-R175 | 2.2 kΩ, ±5%. ¼ W Resistor | 110000-222 |
| R176 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R177 | 15 kΩ, ±5%, ¼ W Resistor | 110000-153 |
| R178 | 3.9 kΩ, ±5%, ¼ W Resistor | 110000-392 |

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# Black Widow Game Printed-Circuit Board Assembly Parts List, continued

| *Designator* | *Description* | *Part No.* |
|---|---|---|
| R179 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R180 | 680 Ω, ±5%, ¼ W Resistor | 110000-681 |
| R181 | 2.7 kΩ, ±5%, ¼ W Resistor | 110000-272 |
| R182 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R183 | 3.9 kΩ, ±5%, ¼ W Resistor | 110000-392 |
| R184 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R185 | 2.2 kΩ, ±5%. ¼ W Resistor | 110000-222 |
| R186 | 3.9 kΩ, ±5%, ¼ W Resistor | 110000-392 |
| R187 | 2 kΩ Vertical PCB-Mounting Cermet Trimpot (Acceptable substitute is part no. 19-315202) | 119002-202 |
| R188 | 5.6 kΩ, ±5%, ¼ W Resistor | 110000-562 |
| R189 | 10 kΩ Vertical PCB-Mounting Cermet Trimpot (Acceptable substitute is part no. 19-315103) | 119002-103 |
| R190 | 1.2 kΩ, ±5%, ¼ W Resistor | 110000-122 |
| R192 | 10 kΩ Vertical PCB-Mounting Cermet Trimpot (Acceptable substitute is part no. 19-315103) | 119002-103 |
| R193, R194 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R195 | 270 Ω, ±5%, ¼ W Resistor | 110001-271 |
| R196–R198 | 2.2 kΩ, ±5%. ¼ W Resistor | 110000-222 |
| R199 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R200 | 12 kΩ, ±5%, ¼ W Resistor | 110000-123 |
| R201 | 3.9 kΩ, ±5%, ¼ W Resistor | 110000-392 |
| R202 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R203 | 680 Ω, ±5%, ¼ W Resistor | 110000-681 |
| R204 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R205 | 2.7 kΩ, ±5%, ¼ W Resistor | 110000-272 |
| R206 | 3.9 kΩ, ±5%, ¼ W Resistor | 110000-392 |
| R207 | 2.2 kΩ, ±5%. ¼ W Resistor | 110000-222 |
| R208 | 3.9 kΩ, ±5%, ¼ W Resistor | 110000-392 |
| R209 | 470 Ω, ±5%, ¼ W Resistor | 110000-471 |
| R210 | 2 kΩ Vertical PCB-Mounting Cermet Trimpot (Acceptable substitute is part no. 19-315202) | 119002-202 |
| R211 | 5.6 kΩ, ±5%, ¼ W Resistor | 110000-562 |
| R212, R213 | 10 kΩ Vertical PCB-Mounting Cermet Trimpot (Acceptable substitute is part no. 19-315103) | 119002-103 |
| R214 | 100 Ω, ±5%, ¼ W Resistor | 110000-101 |
| R215 | 68 Ω, ±5%, ¼ W Resistor | 110000-680 |
| R216 | 6.8 kΩ, ±5%, ¼ W Resistor | 110000-682 |
| R217 | 100 Ω, ±5%, ¼ W Resistor | 110000-101 |
| R218 | 68 Ω, ±5%, ¼ W Resistor | 110000-680 |
| R219 | 6.8 kΩ, ±5%, ¼ W Resistor | 110000-682 |
| RV1, RV2 | Voltage Dependent Resistor | 110004-001 |

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# Black Widow Game Printed-Circuit Board Assembly Parts List, continued

| *Designator* | *Description* | *Part No.* |
|---|---|---|
| | **Sockets** | |
| B3 | 40-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C40 |
| C2 | 40-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C40 |
| C/D3 | 40-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C40 |
| D1 | 24-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C24 |
| E/F1 | 24-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C24 |
| H1 | 24-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C24 |
| J1 | 24-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C24 |
| J9 | 40-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C40 |
| K7 | 24-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C24 |
| K/L1 | 24-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C24 |
| L7 | 24-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C24 |
| M1 | 24-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C24 |
| M2 | 22-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C22 |
| M/N7 | 24-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C24 |
| N/P1 | 24-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C24 |
| N/P7 | 24-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C24 |
| R7 | 24-Contact Medium-Insertion-Force Integrated Circuit Socket | 79-42C24 |
| | **Transistors** | |
| Q1 | Type-2N3904, 60 V, 1 W NPN Transistor | 34-2N3904 |
| Q2-Q4 | Type-2N6044 Darlington NPN Transistor | 34-2N6044 |
| Q5, Q6 | Type-2N3904, 60 V, 1 W NPN Transistor | 34-2N3904 |
| Q7 | Type-2N3906 PCB Switching and Amplifying Transistor | 33-2N3906 |
| Q8 | Type-2N3904, 60 V, 1 W NPN Transistor | 34-2N3904 |
| Q10 | Type-2N3904, 60 V, 1 W NPN Transistor | 34-2N3904 |
| Q11 | Type-2N3906 PCB Switching and Amplifying Transistor | 33-2N3906 |
| Q12 | Type-2N3904, 60 V, 1 W NPN Transistor | 34-2N3904 |

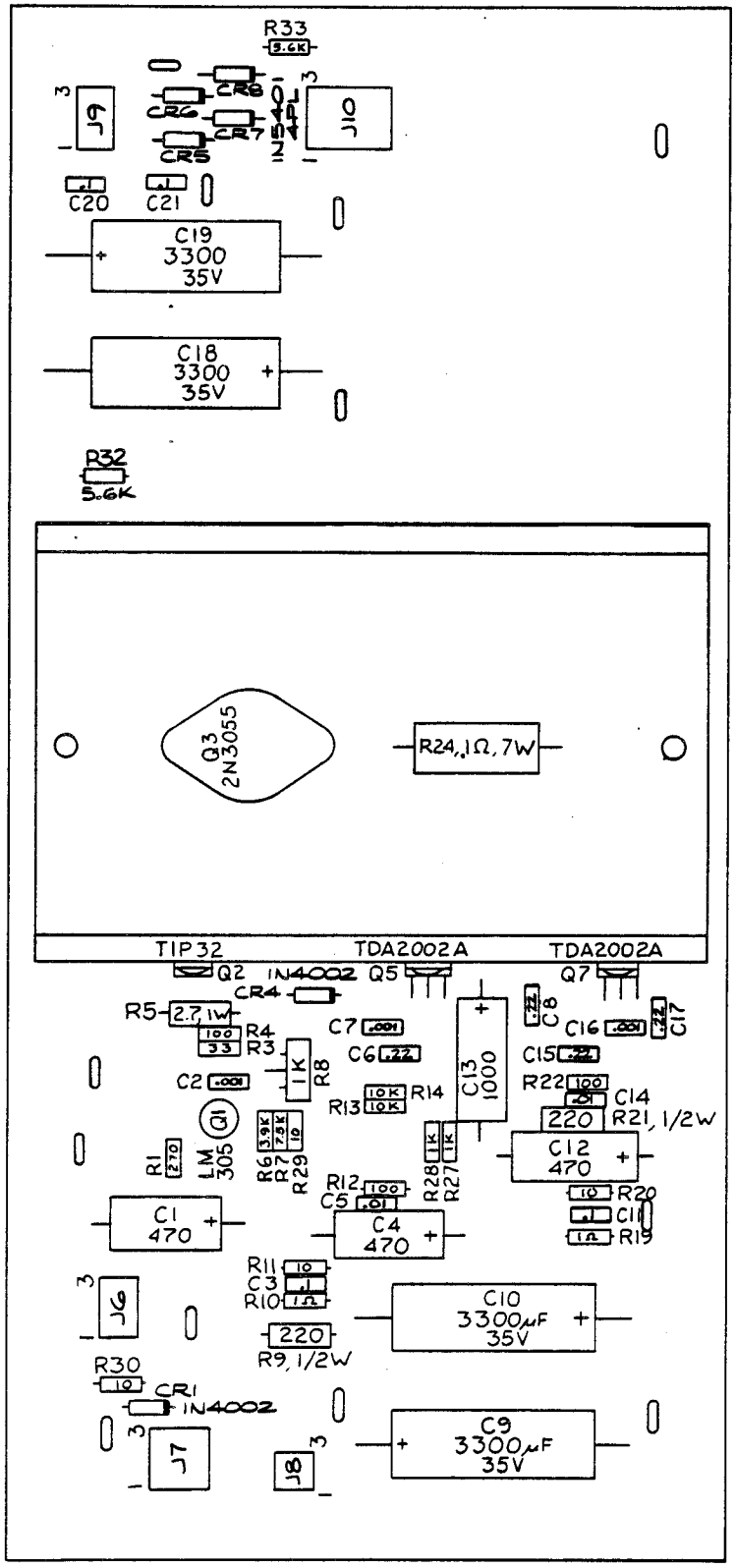


**Figure 3-13 Regulator/Audio II PCB Assembly**
**A035435-04 D**

# Regulator/Audio II PCB Assembly
# Parts List

| *Designator* | *Description* | *Part No.* |
|---|---|---|
| | **Capacitors** | |
| C1 | 470 μF, 25 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor | 24-250477 |
| C2 | 0.001 μF, 50 V, Ceramic-Disc Axial-Lead Capacitor | 122002-102 |
| C3 | 0.1 μF, +80%, -20%, 50 V, Ceramic-Disc Capacitor | 122001-104 |
| C4 | 470 μF, 25 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor | 24-250477 |
| C5 | 0.01 μF, 25 V Minimum, Ceramic-Disc Axial-Lead Capacitor (Acceptable substitute is part no. 122005-103) | 100015-103 |
| C6 | 0.22 μF, 25 V, Ceramic-Disc Axial-Lead Capacitor | 122004-224 |
| C7 | 0.001 μF, 50 V, Ceramic-Disc Axial-Lead Capacitor | 122002-102 |
| C8 | 0.22 μF, 25 V, Ceramic-Disc Axial-Lead Capacitor | 122004-224 |
| C9, C10 | 3300 μF, 35 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor | 24-350338 |
| C11 | 0.1 μF, +80%, -20%, 50 V, Ceramic-Disc Capacitor | 122001-104 |
| C12 | 470 μF, 25 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor | 24-250477 |
| C13 | 1000 μF, 25 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor | 24-250108 |
| C14 | 0.01 μF, 25 V Minimum, Ceramic-Disc Axial-Lead Capacitor (Acceptable substitute is part no. 122005-103) | 100015-103 |
| C15 | 0.22 μF, 25 V, Ceramic-Disc Axial-Lead Capacitor | 122004-224 |
| C16 | 0.001 μF, 50 V, Ceramic-Disc Axial-Lead Capacitor | 122002-102 |
| C17 | 0.22 μF, 25 V, Ceramic-Disc Axial-Lead Capacitor | 122004-224 |
| C18, C19 | 3300 μF, 35 V, Aluminum Electrolytic Fixed Axial-Lead Capacitor | 24-350338 |
| C20, C21 | 0.1 μF, +80%, -20%, 50 V, Ceramic-Disc Capacitor | 122001-104 |
| | **Diodes** | |
| CR1 | Type-1N4002, 1 A, 100 V Silicon Rectifier Diode | 31-1N4002 |
| CR4 | Type-1N4002, 1 A, 100 V Silicon Rectifier Diode | 31-1N4002 |
| CR5-CR8 | Type-1N5401, 3 A, 100 V Silicon Rectifier Diode | 31-1N5401 |
| | **Integrated Circuits** | |
| Q1 | Type-LM305, 5 V, Linear Voltage Regulator | 37-LM305 |
| Q5 | Type-TDA2002A, 8 W, Linear Audio Amplifier Integrated Circuit | 137151-002 |
| Q7 | Type-TDA2002A, 8 W, Linear Audio Amplifier Integrated Circuit | 137151-002 |
| | **Resistors** | |
| R1 | 270 Ω, ±5%, ¼ W Resistor | 110000-271 |
| R3 | 33 Ω, ±5%, ¼ W Resistor | 110000-330 |
| R4 | 100 Ω, ±5%, ¼ W Resistor | 110000-101 |
| R5 | 2.7 Ω, ±5%, 1 W Resistor | 110009-027 |
| R6 | 3.9 kΩ, ±5%, ¼ W Resistor | 110000-392 |
| R7 | 7.5 kΩ, ±5%, ¼ W Resistor | 110000-752 |
| R8 | 1 kΩ Vertical PCB-Mounting Cermet Potentiometer (Acceptable substitute is part no. 119002-102) | 19-315102 |
| R9 | 220 Ω, ±5%, ½ W Resistor | 110001-221 |

*(Continued on next page)*

# Regulator/Audio II PCB Assembly
# Parts List, continued

| *Designator* | *Description* | *Part No.* |
|---|---|---|
| R10 | 1 Ω, ±5%, ¼ W Resistor | 110000-010 |
| R11 | 10 Ω, ±5%, ¼ W Resistor | 110000-100 |
| R12 | 100 Ω, ±5%, ¼ W Resistor | 110000-101 |
| R13, R14 | 10 kΩ, ±5%, ¼ W Resistor | 110000-103 |
| R19 | 1 Ω, ±5%, ¼ W Resistor | 110000-010 |
| R20 | 10 Ω, ±5%, ¼ W Resistor | 110000-100 |
| R21 | 220 Ω, ±5%, ½ W Resistor | 110001-221 |
| R22 | 100 Ω, ±5%, ¼ W Resistor | 110000-101 |
| R24 | 0.1 Ω, ±3%, 7 W Wirewound Resistor | 19-100P1015 |
| R27, R28 | 1 kΩ, ±5%, ¼ W Resistor | 110000-102 |
| R29, R30 | 10 Ω, ±5%, ¼ W Resistor | 110000-100 |
| R32, R33 | 5.6 kΩ, ±5%, ¼ W Resistor | 110000-562 |
| | **Transistors** | |
| Q2 | Type-TIP32 PNP Power Transistor | 33-TIP32 |
| Q3 | Type-2N3055 NPN Silicon Transistor | 34-2N3055 |
| | **Mechanical Parts** | |
| J6 | 6-Position Connector Receptacle | 79-58306 |
| J7 | 9-Position Connector Receptacle | 79-58308 |
| J8 | 4-Position Connector Receptacle | 79-58354 |
| J9 | 6-Position Connector Receptacle | 79-58306 |
| J10 | 12-Position Connector Receptacle | 79-58346 |
| Q2 | #6-32 x ¼-Inch Binder-Head Nylon Screw | 75-F60405 |
| Q3 | #6-32 Nut/Washer Assembly | 75-99516 |
| Q3 | Thermally Conductive Silicon Insulator | 78-16008 |
| Q2 | Thermally Conductive Silicon Insulator | 78-16014 |
| Q5, Q7 | #6 x ⅜-Inch Cross-Recessed Pan-Head Thread-Forming Type-AB Zinc-Plated-Steel Screw | 72-6606S |
| | Heat Sink | 034531-01 |
| | Test Point (Acceptable substitute is part no. 020670-01) | 179051-001 |

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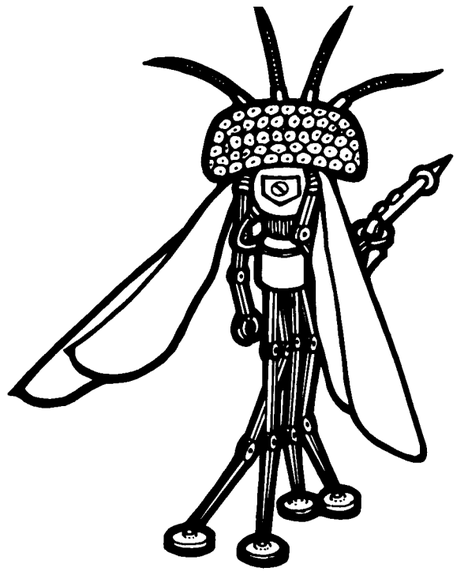
*NOTE*

*This staple temporarily holds the schematic package together. Remove the staple before using the schematics.*



# Schematic Package Supplement to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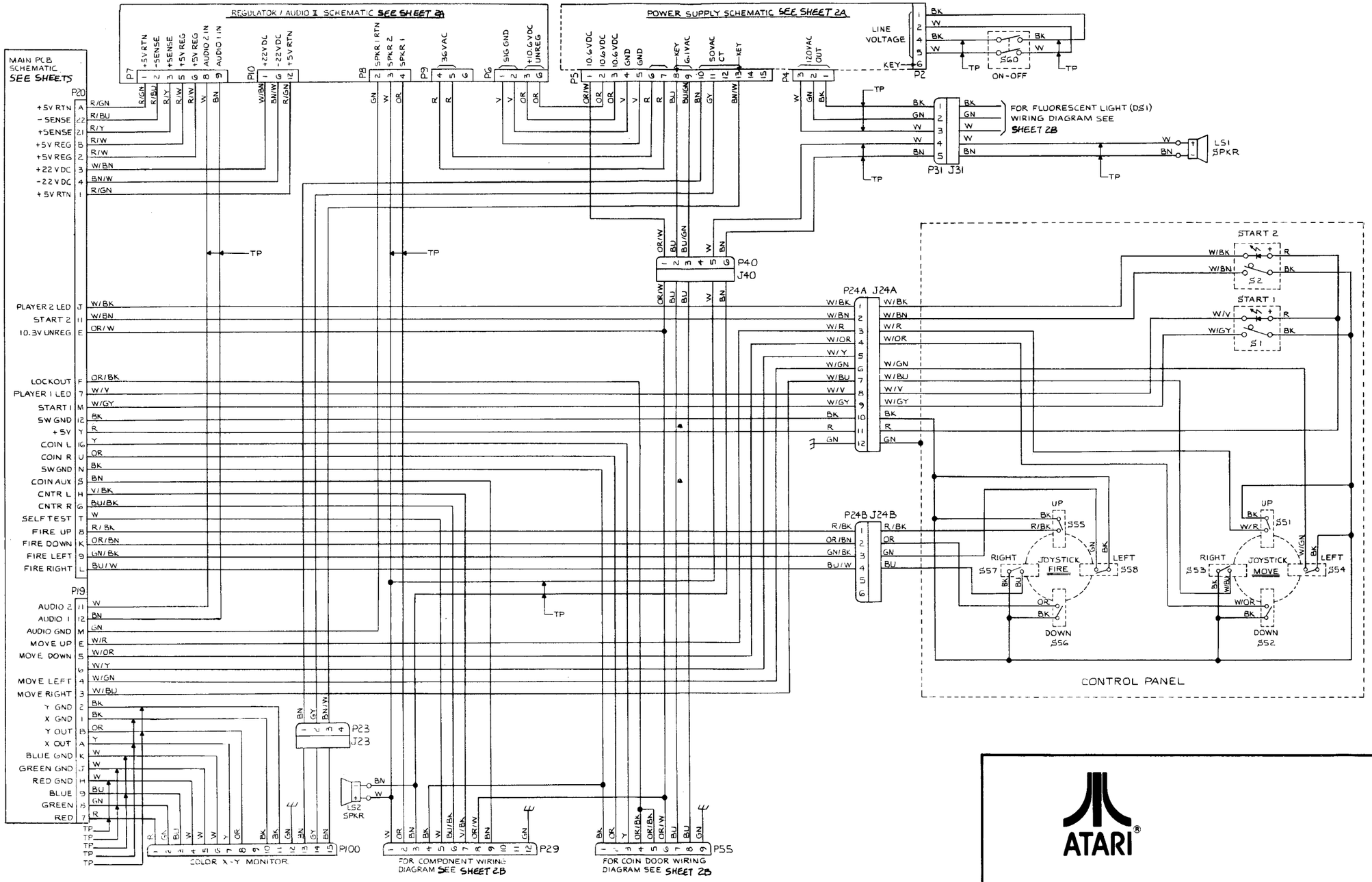


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# Black Widow Main Wiring Diagram



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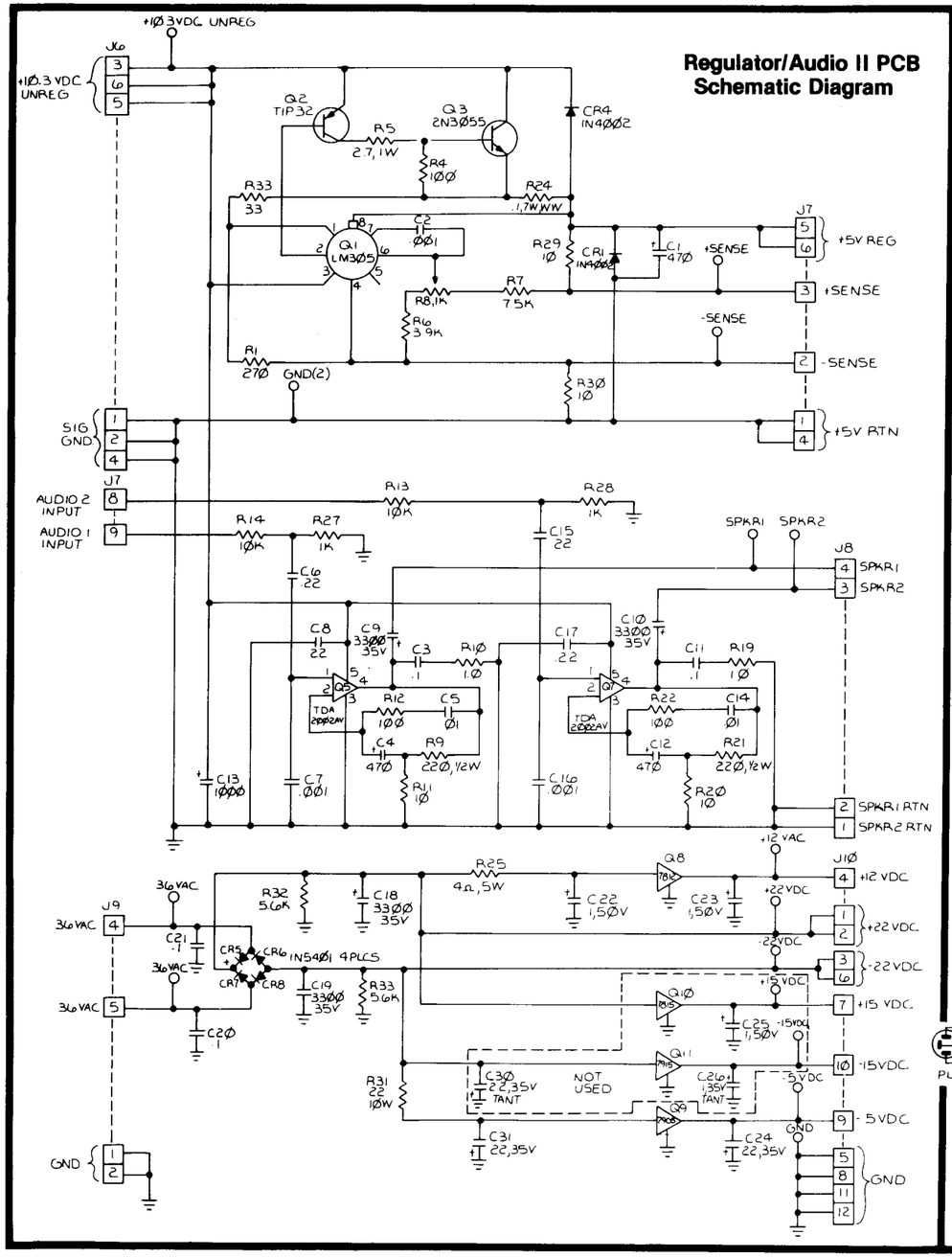
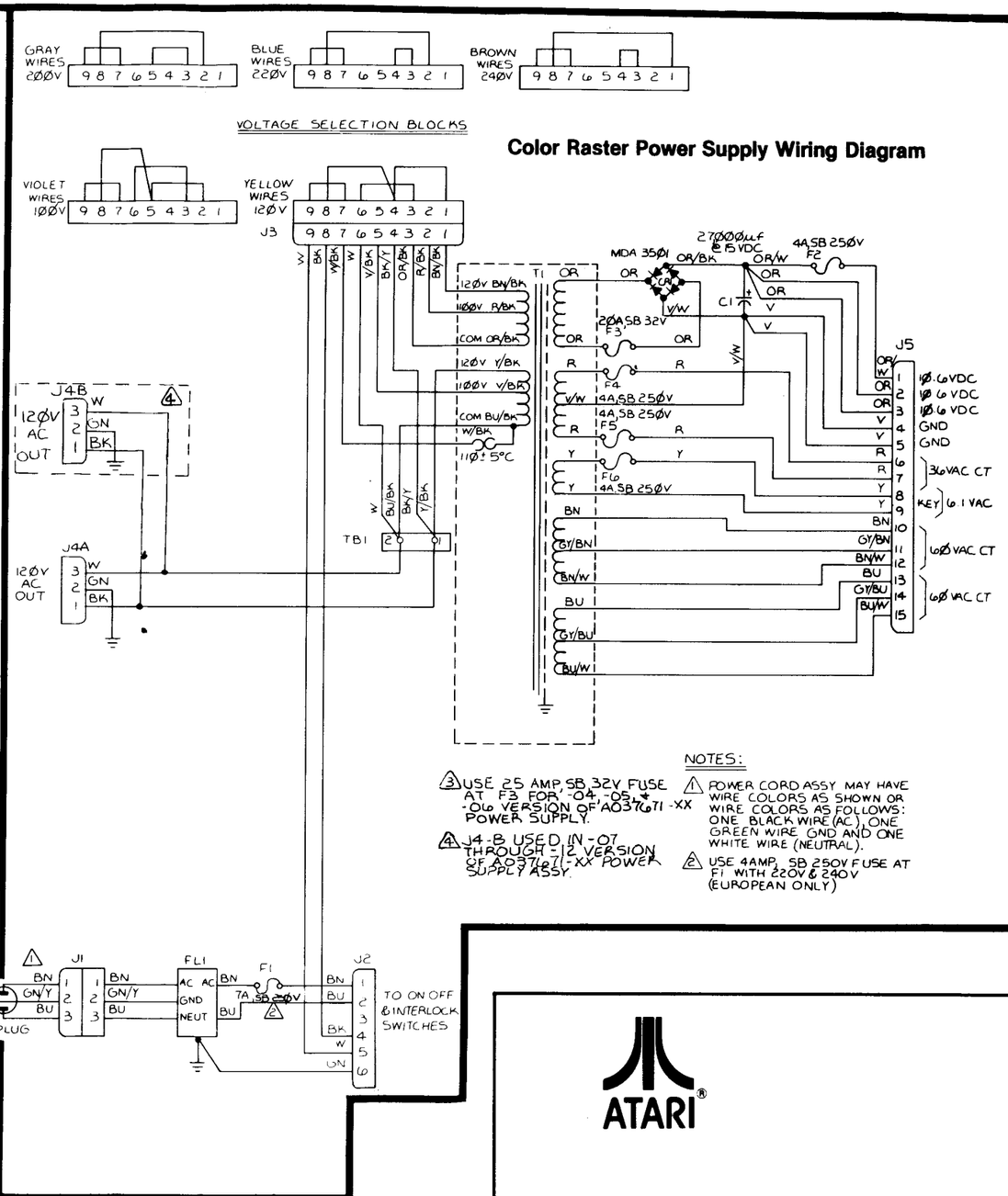
## Regulator/Audio II PCB Schematic Diagram




## Color Raster Power Supply Wiring Diagram




NOTES:

1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE GND AND ONE WHITE WIRE (NEUTRAL).
2. USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY)
3. USE 25 AMP, SB 32V FUSE AT F3 FOR -04, -05, + -06 VERSION OF A037671-XX POWER SUPPLY.
4. J4-B USED IN -07 THROUGH -12 VERSION OF A037671-XX POWER SUPPLY ASSY.

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# Regulator/Audio II PCB and Power Supply



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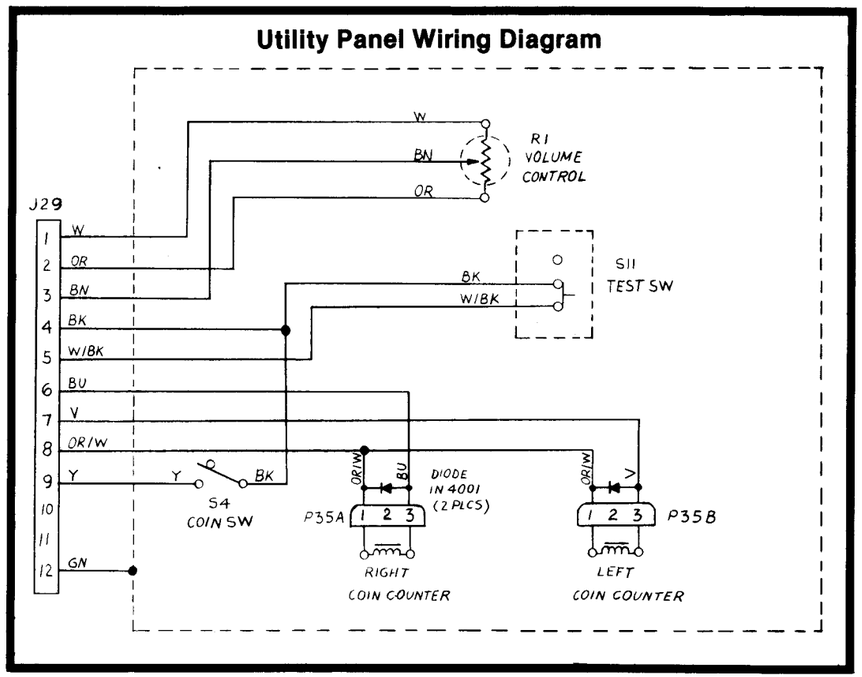
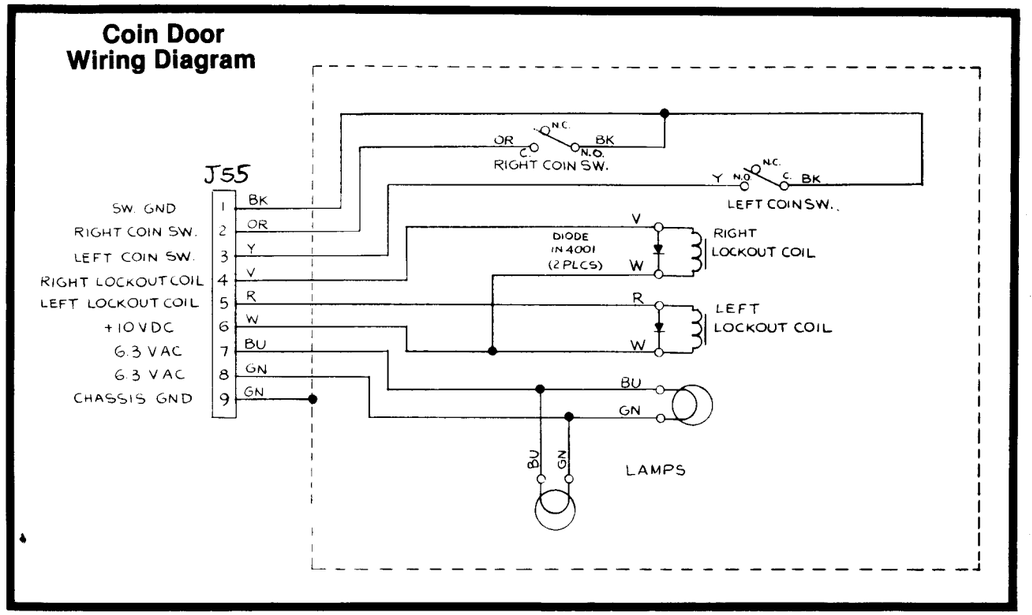
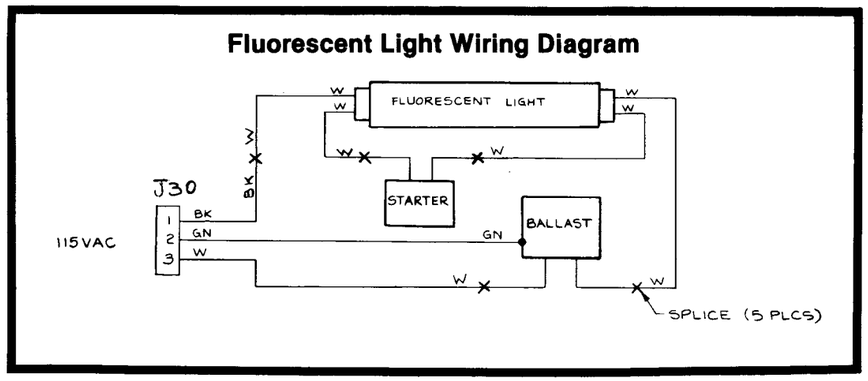
## Utility Panel Wiring Diagram




## Coin Door Wiring Diagram




## Fluorescent Light Wiring Diagram

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# Black Widow Game Wiring Interfaces



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| HEXA-DECIMAL ADDRESS | ADDRESS BUS | | | | | | | | | | | | | | | | R/W | DATA BUS | | | | | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| E000-EFFF | 1 | 1 | 1 | | A | A | A | A | A | A | A | A | A | A | A | A | R | D | D | D | D | D | D | D | D | $\overline{\text{ROM 5}}$ |
| D000-DFFF | 1 | 1 | 0 | 1 | A | A | A | A | A | A | A | A | A | A | A | A | R | D | D | D | D | D | D | D | D | $\overline{\text{ROM 4}}$ |
| C000-CFFF | 1 | 1 | 0 | 0 | A | A | A | A | A | A | A | A | A | A | A | A | R | D | D | D | D | D | D | D | D | $\overline{\text{ROM 3}}$ |
| B000-BFFF | 1 | 0 | 1 | 1 | A | A | A | A | A | A | A | A | A | A | A | A | R | D | D | D | D | D | D | D | D | $\overline{\text{ROM 2}}$ |
| A000-AFFF | 1 | 0 | 1 | 0 | A | A | A | A | A | A | A | A | A | A | A | A | R | D | D | D | D | D | D | D | D | $\overline{\text{ROM 1}}$ |
| 9000-9FFF | 1 | 0 | 0 | 1 | A | A | A | A | A | A | A | A | A | A | A | A | R | D | D | D | D | D | D | D | D | $\overline{\text{ROM 0}}$ |
| 8800 | 1 | 0 | 0 | 0 | 1 | | | | | | | | | | | | R | D | | | | | | | | CABINET 1 |
| | | | | | | | | | | | | | | | | | | | D | | | | | | | $\overline{\text{START 2}}$ |
| | | | | | | | | | | | | | | | | | | | | D | | | | | | $\overline{\text{START 1}}$ |
| | | | | | | | | | | | | | | | | | | | | | D | | | | | SPARE |
| | | | | | | | | | | | | | | | | | | | | | | D | | | | $\overline{\text{FIRE UP}}$ |
| | | | | | | | | | | | | | | | | | | | | | | | D | | | $\overline{\text{FIRE DOWN}}$ |
| | | | | | | | | | | | | | | | | | | | | | | | | D | | $\overline{\text{FIRE LEFT}}$ |
| | | | | | | | | | | | | | | | | | | | | | | | | | D | $\overline{\text{FIRE RIGHT}}$ |
| 89C0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | | | | | | | W | | | | | | | | | SPARE WT |
| 8980 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | | | | | | | W | | | | | | | | | WDCLR |
| 8940 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A | A | A | A | A | A | W | D | D | D | D | D | D | D | D | EAROMWR |
| 8900 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | | | | | | | W | | | | | D | D | D | D | EAROMCON |
| 88C0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | | | | | | W | | | | | | | | | INTACK |
| 8880 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | | | | | | | W | | | | | | | | | VORST |
| 8840 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | | | | | | | W | | | | | | | | | VGGO |
| 8800 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | | | | | | W | D | | | | | | | | $\overline{\text{INVERT Y}}$ |
| | | | | | | | | | | | | | | | | | | | D | | | | | | * | $\overline{\text{INVERT X}}$ |
| | | | | | | | | | | | | | | | | | | | | D | | | | | | $\overline{\text{PLAYER 2 LED}}$ |
| | | | | | | | | | | | | | | | | | | | | | D | | | | | $\overline{\text{PLAYER 1 LED}}$ |
| | | | | | | | | | | | | | | | | | | | | | | D | | | | $\overline{\text{COIN LOCKOUT}}$ |
| | | | | | | | | | | | | | | | | | | | | | | | D | | * | BANK SEL |
| | | | | | | | | | | | | | | | | | | | | | | | | D | | COIN CNTR-L |
| | | | | | | | | | | | | | | | | | | | | | | | | | D | COIN CNTR-R |
| 8000 | 1 | 0 | 0 | 0 | 0 | | | | | | | | | | | | R | D | | | | | | | | OPTION 2 |
| | | | | | | | | | | | | | | | | | | | D | | | | | | | OPTION 1 |
| | | | | | | | | | | | | | | | | | | | | D | | | | | | OPTION 0 |
| | | | | | | | | | | | | | | | | | | | | | D | | | | | SPARE |
| | | | | | | | | | | | | | | | | | | | | | | D | | | | $\overline{\text{MOVE UP}}$ |
| | | | | | | | | | | | | | | | | | | | | | | | D | | | $\overline{\text{MOVE DOWN}}$ |
| | | | | | | | | | | | | | | | | | | | | | | | | D | | $\overline{\text{MOVE LEFT}}$ |
| | | | | | | | | | | | | | | | | | | | | | | | | | D | $\overline{\text{MOVE RIGHT}}$ |
| 7800 | 0 | 1 | 1 | 1 | 1 | | | | | | | | | | | | R | D | | | | | | | | 3 KHZ |
| | | | | | | | | | | | | | | | | | | | D | | | | | | | HALT |
| | | | | | | | | | | | | | | | | | | | | D | | | | | | $\overline{\text{SA}}$ |
| | | | | | | | | | | | | | | | | | | | | | D | | | | | $\overline{\text{SELF-TEST}}$ |
| | | | | | | | | | | | | | | | | | | | | | | D | | | | $\overline{\text{COIN-AUX}}$ |
| | | | | | | | | | | | | | | | | | | | | | | | D | | | $\overline{\text{COIN L}}$ |
| | | | | | | | | | | | | | | | | | | | | | | | | | D | $\overline{\text{COIN R}}$ |
| 7000 | 0 | 1 | 1 | 1 | 0 | | | | | | | | | | | | R | D | D | D | D | D | D | D | D | $\overline{\text{EAROMRD}}$ |
| 6800 | 0 | 1 | 1 | 0 | 1 | | | | | | | | | | | | R/$\overline{\text{W}}$ | D | D | D | D | D | D | D | D | I/O1 |
| 6000 | 0 | 1 | 1 | 0 | 0 | | | | | | | | | | | | R/$\overline{\text{W}}$ | D | D | D | D | D | D | D | D | $\overline{\text{I/O0}}$ |
| 5000-5FFF | 0 | 1 | 0 | 1 | A | A | A | A | A | A | A | A | A | A | A | A | R | D | D | D | D | D | D | D | D | $\overline{\text{VROM 3}}$ |
| 4000-4FFF | 0 | 1 | 0 | 0 | A | A | A | A | A | A | A | A | A | A | A | A | R | D | D | D | D | D | D | D | D | $\overline{\text{VROM 2}}$ |
| 3000-3FFF | 0 | 0 | 1 | 1 | A | A | A | A | A | A | A | A | A | A | A | A | R | D | D | D | D | D | D | D | D | $\overline{\text{VROM 1}}$ |
| 2800-2FFF | 0 | 0 | 1 | 0 | 1 | A | A | A | A | A | A | A | A | A | A | A | R | D | D | D | D | D | D | D | D | $\overline{\text{VROM 0}}$ |
| 2000-27FF | 0 | 0 | 1 | 0 | 0 | A | A | A | A | A | A | A | A | A | A | A | R/$\overline{\text{W}}$ | D | D | D | D | D | D | D | D | $\overline{\text{VRAM}}$ |
| 0000-07FF | 0 | 0 | 0 | 0 | 0 | A | A | A | A | A | A | A | A | A | A | A | R/$\overline{\text{W}}$ | D | D | D | D | D | D | D | D | $\overline{\text{RAM}}$ |

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**Black Widow Memory Map**



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# Descriptions of Black Widow Printed Circuit Board Names

**A10, A13-A15**

Address bits on Microprocessor Address Bus lines A10 and A13-A15 are generated by Microprocessor C2. Bits on lines A13-A15, together with those on AB11-AB12, are the input bits to Address Decoders R1-R2. A10 is exclusive-ORed with BANK SEL by gate B6 to produce the A10 input bit for Random-Access Memory N/P1.

**AB0-AB12**

Address bits on Buffered Microprocessor Address Bus lines AB0-AB12 are software-generated by Microprocessor C2 and buffered by B1 and C1. These signals are the input bits to Read-Only Memories D1, E/F1, H1, J1, K/L1, and M1; and to Random-Access Memory N/P1.

Address bits AB6-AB8 are the select input signals for Address Decoder P3.

Address bits AB11-AB12 and A13-A15 are the input bits for Address Decoders R1 and R2.

Address bits AB0-AB13 are applied with bits from AVG0-AVG12 to Vector Address Selectors K8, M8, L8, and N8 to produce the data on lines AM0-AM12.

Bits AB0-AB3 are control signals to custom audio chips B3 and C/D3 in the Option Switch Input and Audio Output circuit.

Bits AB0-AB5 are the input signals to latch P2 in the High-Score Table circuit where they are used to produce the A1-A5 address input for EAROM M2.

**$\overline{AB13}$**

$\overline{AB13}$ is from AB13, inverted by J3, and applied to Vector Address Selector M8. When $\overline{VMEM}$ is low, $\overline{AB13}$ and $\overline{AB12}$ select the specific Vector Memory Read-Only Memory.

**AM0-AM13**

Address bits on Multiplexed Address Bus lines AM0-AM13 are software-generated by Vector Address Selectors K8, L8, M8, and N8. When $\overline{VMEM}$ is low, the Multiplexed Address Bus is from Buffered Microprocessor Address Bus AB0 through AB12 and $\overline{AB13}$. When $\overline{VMEM}$ is high, AM0-AM12 is from Vector-Generator Address Bus lines AVG0-AVG13.

Signals AM0-AM11 are the input address signals to Vector Read-Only Memories L7, M/N7, N/P7, R7 and to Vector Random-Access Memory K7. In addition, AM11-AM13 are the select input signals for Vector Address Decoder J7. AM0-AM7 are input signals for multiplexers N3 and R3 of the State Machine circuit.

**AUD 1-AUD 2**

The Audio 1 and Audio 2 signals are game PCB output signals that are generated by custom audio chips B3 and C/D3 of the Option Switch Input and Audio Output circuit. AUD 1 is the inverse of AUD 2. These signals are applied to the Audio/Regulator II PCB and ultimately drive speakers 1 and 2.

**AVG0-AVG13**

Address bits on Vector-Generator Address Bus lines AVG0-AVG13 are software-generated by Vector Address Controller J9. When $\overline{VMEM}$ is high, these signals are passed through the Vector Address Selectors on lines AM0-AM13 to the Vector Read-Only Memory and the Vector Random-Access Memory.

**BANK SEL**

The Bank Select signal is developed from data on line DB2. When latch R9 of the Coin Door and Control Panel Output circuit is clocked by $\overline{LATCH}$, R9 latches the data on DB2 to pin 2 of R9, producing the BANK SEL signal. BANK SEL is exclusive-ORed with the address bit A10 by gate B6 to produce input address bit A10 for Random-Access Memory N/P1.

**BLANK**

Blank is an active high-level signal generated by counter M3 in the Z Intensity and Blanking circuit and ORed with Z BLANK by gate M5 of the R-G-B Output circuit. When high, BLANK turns off transistors Q6, Q8, and Q10, which kills the RED, GREEN, and BLUE output signals to the display.

**BLUE**

Blue is a game PCB output signal developed from the data on line DVY0. When the data bit on DVY0 is high and latch K10 of the R-G-B Output circuit is clocked by $\overline{STATCLK}$, the data on DVY0 is inverted and latched to pin 11 of K10. If both BLANK and Z BLANK are low, this data bit is again inverted by gate L10 to turn on Q10. Transistor Q10 generates the BLUE signal for the display.

**$\overline{BUFFEN}$**

Buffer Enable is an active low-level signal developed from $\overline{B\Phi 2}$ by Vector Address Selector K8. $\overline{BUFFEN}$ is the enable input signal for Vector Memory Data Buffer P8. When low, $\overline{BUFFEN}$ allows P8 to pass data.

**BΦ2**

The active high-level Phase 2 Clock signal is hardware-generated from the internal clock circuitry of Microprocessor C2, buffered by B1, and applied to AND gate K4. Gate K4 ANDs together BΦ2, $\overline{R/WB}$, and 3 MHz to produce $\overline{WRITE}$. BΦ2 is also used as the clock signal for custom audio chips B3 and C/D3 of the Option Switch Input and Audio Output circuit.

**$\overline{B\Phi 2}$**

The active low-level Phase 2 Clock signal is generated at pin 12 of F3 by inverting BΦ2. $\overline{B\Phi 2}$ is applied to Vector Address Selector K8 to produce $\overline{BUFFEN}$.

**$\overline{CENTER}$**

Center is an active-low level signal software-generated by gating $\overline{CNTR}$ with $\overline{HALT}$ by Center Flag gate L6. When low, $\overline{CENTER}$ closes switches E10 of the Y-Axis Output circuit and B10 of the X-Axis Output circuit to center the beam on the display.

**CNTR**

The active high-level Center Flag signal is software-generated by latch E5 of the Center Flag circuit. CNTR is set high when VGCK, $\overline{STROBE3}$, and $\overline{OP2}$ are low. CNTR is applied to gate J5 of the Normalization Flag circuit to develop the clear signal for latch A6. CNTR is ORed with VCTR by GO Flag gate M5 to generate the GO signal.

**$\overline{CNTR}$**

The active low-level Center Flag signal is software-generated by latch E5 of the Center Flag circuit. When clocked by the 12-MHZ signal, E5 latches $\overline{STOP}$ to pin 9 to produce $\overline{CNTR}$. $\overline{CNTR}$ is gated with $\overline{HALT}$ by Center Flag gate L6 to generate $\overline{CENTER}$.

**COIN CNTR-L**

Coin Counter Left is a game PCB output signal developed from the data bit on line DB1. When clocked by $\overline{LATCH}$, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB1 to pin 6 of R9. From here, the signal is current amplified and inverted by Q4 and applied to the game Utility Panel to activate the Left Coin Counter.

**COIN CNTR-R**

Coin Counter Right is a game PCB output signal developed from the data bit on line DB0. When clocked by $\overline{LATCH}$, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB0 to pin 5 of R9. From here, the signal is current amplified and inverted by Q3 and applied to the game Utility Panel to activate the Right Coin Counter.

**COIN LOCKOUT**

Coin Lockout is a game PCB output signal developed from the data on line DB3. When clocked by $\overline{LATCH}$, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB3 to pin 9 of R9. From here, the signal is current amplified and inverted by Q2 and applied to the Right and Left Lockout Coils of the game Coin Door.

**D0-D7**

Microprocessor Data Bus lines D0-D7 form a bi-directional data bus between the Microprocessor, the Read-Only Memory, and the Option Switch Input circuits.

**DB0-DB7**

Buffered Microprocessor Data Bus lines DB0-DB7 form a buffered bi-directional data bus between microprocessor data-bus buffer F2 and Vector Memory Data Buffer P8; Coin-Door and Control Panel Input circuit buffers L9, M9, and N9; High-Score Table latches K2 and J2; and High-Score Table buffer H2.

**$\overline{DIS\ DAT}$**

Disable Data is an active low-level signal generated by test equipment connected to the $\overline{DIS\ DAT}$ test point. $\overline{DIS\ DAT}$ is ANDed with the ROM signal by gate E3 to produce the enable signal for buffer E2 of the Read-Only Memory circuit. When enabled, buffer E2 passes data from the selected Read-Only Memory to the Microprocessor Data Bus.

**$\overline{DISRST}$**

Display Reset is an active low-level signal software-generated by gate L6 of the Halt Flag circuit. When either $\overline{RESET}$ or $\overline{VGRST}$ is low, $\overline{DISRST}$ is set low. When low, $\overline{DISRST}$ clears State Machine latch P4, DAC Reference and Bipolar Current Sources latch E8, R-G-B Output latch K10, Vector Scaling latch D7, Z Intensity and Blanking latch E6 and counter M3. In addition, $\overline{DISRST}$ presets the HALT signal from latch L5 to the high level.

**DVG0-DVG7**

Data bits on Vector-Generator Data Bus lines DVG0-DVG7 are software-generated by the selected Vector Read-Only Memory or Vector Random-Access Memory. If Vector Memory Data Buffer P8 is enabled ($\overline{BUFFEN}$ is low) and the $\overline{R/WB}$ line is low, the data on lines DVG0-DVG7 is passed through P8 to the Buffered Microprocessor Data Bus to be read by the microprocessor. Otherwise, the data on DVG0-DVG7 is sent to the Vector Data Shifters and to the Op Code and Intensity Latches.

**DVX3-DVX12, $\overline{DVX12}$**

Data bits on X-Axis Vector Data lines DVX3-DVX12 and $\overline{DVX12}$ are software-generated by Vector Data Shifters A8, B8, C8, and by latch C6 of the Op Code and Intensity Latches circuit. DVX3-DVX11 and $\overline{DVX12}$ are the input signals to digital-to-analog converter (DAC) A/B9 of the X-Axis Output circuit. The data carried on these lines represents the X-axis change from the current location of the display beam. If $\overline{DVX12}$ is low, DAC A/B9 operates only in its lower 512 positions, which means a negative direction of change on the display. If $\overline{DVX12}$ is high, DAC A/B9 operates only in its upper 512 positions for a positive direction of change on the display.

In addition, DVX11 and DVX12 are exclusive-ORed by gate B6 of the Normalization Flag circuit.

**DVY0-DVY12, $\overline{DVY12}$**

Data bits on Y-Axis Vector Data lines DVY0-DVY12 and $\overline{DVY12}$ are software-generated by Vector Data Shifters F8, H8, J8, and by latch D6 of the Op Code and Intensity Latches circuit. DVY3-DVY11 and $\overline{DVY12}$ are the input signals for digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit. The data carried on these lines represents the Y-axis change from the current location of the display beam. If $\overline{DVY12}$ is low, DAC F9 operates only in its lower 512 positions, which means a negative direction of change on the display. If $\overline{DVY12}$ is high, DAC F9 operates only in its upper 512 positions for a positive direction of change on the display.

In addition, DVY0-DVY7 are applied to latch E8 in the DAC Reference and Bipolar Current Sources circuit. These signals, together with VCTR and $\overline{VCTR}$, set the X REF and Y REF voltage levels (via DAC D9).

Lines DVY0-DVY2 carry data representing the eight different color signals for latch K10 of the R-G-B Output circuit.

Lines DVY4-DVY7 carry data representing the Z-intensity signals for latch E6 of the Z Intensity and Blanking circuit.

Data on DVY8-DVY10 are applied to latch D7 of the Vector Scaling circuit. The data carried on these lines represents the number (in binary) that the Vector Scaling circuit uses to divide into the vector drawing time. The vector drawing time n is divided by 2 , where n equals the number represented on DVY8-DVY10.

In addition, DVY11 and DVY12 are exclusive-ORed by gate B6 of the Normalization Flag circuit.

**$\overline{EAROMCON}$**

The Electrically-Alterable ROM Control signal is an active low-level signal software-generated by Address Decoder P3 at address 8900. $\overline{EAROMCON}$ is the clock signal for latch K2 in the High-Score Table circuit. $\overline{EAROMCON}$ allows K2 to pass data bits on lines DB0-DB3 to the control lines of EAROM M2.

**$\overline{EAROMRD}$**

The Electrically-Alterable ROM Read Enable is an active low-level signal software-generated by Address Decoder R2 at address 7000. $\overline{EAROMRD}$ is the read-enable signal for buffer H2 of the High-Score Table circuit. $\overline{EAROMRD}$ allows the eight data bits from EAROM M2 to be passed through buffer H2 to the microprocessor data bus.

**$\overline{EAROMWR}$**

The Electrically-Alterable ROM Write Enable is an active low-level signal software-generated by Address Decoder P3 at address 8940. $\overline{EAROMWR}$ is the clock signal for latches J2 and P2 in the High-Score Table circuit. $\overline{EAROMWR}$ allows address bits on lines AB0-AB5 and data bits on lines DB0-DB7 to pass to the address and data input pins of EAROM M2.

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## Black Widow PCB Signal Name Descriptions



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# Black Widow PCB Signal Name Descriptions, cont.

**ENORM**

The active low-level Normalization Flag is software-generated by gate K4 of the Normalization Flag circuit. If OP0 is high, SA is high, and the output from gate J5 is high, ENORM is set low when STROBE0 goes high. ENORM is applied through gate E7 to the S1 input pins of Vector Data Shifters A8, B8, C8, F8, H8, and J8. ENORM multiples the rate of change of the X and Y vector data in the Vector Data Shifters (via shift left operations) at the same $2^n$ factor specified by data on lines DVY8-DVY10. The n number is incremented at a 12-MHz rate until either DVX11 or DVY11 changes state, which then sets ENORM to the high level.

**GO**

The Go flag is an active high-level signal software-generated by gate M5 of the Go Flag circuit when either VCTR or CNTR are high. GO is gated with HALT* by gate N5 of the State Machine circuit to produce the A7 input address bit for State Machine ROM N4.

GO is also used as the enable signal for Vector Timer R6. When GO is high, the Vector Timer starts its count. The Vector Timer counts to 256 if OP1 is high and OP1 is low. If OP1 is low and OP1 is high, the Vector Timer counts to 16K.

**GREEN**

Green is a game PCB output signal developed from the data on line DVY1 in the R-G-B Output circuit. When DVY1 is high and latch K10 is clocked by STATCLK, the data bit on DVY1 is inverted and latched to pin 6 of K10. If both BLANK and Z BLANK are low, this data bit is again inverted by gate L10 to turn on Q8. Transistor Q8 generates the GREEN signal for the display.

**HALT**

The active high-level Halt Flag is software-generated by latch L5 of the Halt Flag circuit. HALT is applied through buffer M9 of the Coin Door and Control Panel Input circuit (when SINP1 is low) to permit Microprocessor C2 to read the status of HALT on line DB6. In addition, HALT is applied to latch P4 of the State Machine circuit to develop HALT*.

**HALT***

The active high-level Delayed Halt Flag is software-generated by latch P4 of the State Machine circuit. HALT* is generated when the HALT signal has been delayed by one pulse of inverted VGCK (1.5 MHz), which in turn has been delayed by one pulse of 12 MHz. HALT* is ORed with GO by gate N5 of the State Machine circuit to produce the A7 input address bit for State Machine ROM N4.

**HALT**

The active low-level Halt Flag is software-generated by latch L5 of the Halt Flag circuit. HALT is the clear signal for Vector Flag latch E5 and Center Flag latch E5. In addition, HALT is ORed with CNTR by gate L6 of the Center Flag circuit to produce CENTER.

**INTACK**

Interrupt Acknowledge is an active low-level signal software-generated from Address Decoder P3 at address 88C0. This signal is an acknowledgment from Microprocessor C2 that an interrupt request has been received. INTACK resets counter J4.

**INVERT X**

Invert X is an active high-level signal developed from the data bit on line DB6. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB6 to pin 12 of R9. When high, INVERT X closes switch B10 through inverter K9 in the X-Axis Output circuit. This inverts the X-axis vector instruction to the display.

**INVERT Y**

Invert Y is an active high-level signal developed from the data bit on line DB7. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches DB7 to pin 15 of R9. When high, INVERT Y closes switch E10 through inverter K9 in the Y-Axis Output circuit. This inverts the Y-axis vector instruction to the display.

**IO**

The Input/Output signal is an active low-level signal software-generated by Address Decoder R2 during addresses 8000 through 8FFF. IO is gated with R/WB by gate J6 to produce the direction signal for bi-directional data buffer N9 of the Coin Door and Control Panel Input circuit. IO determines the direction of data flow through buffer N9.

**I/OS**

I/OS is an active high-level signal software-generated from Address Decoder R2 during addresses 6000 through 6FFF. The I/OS signal is ORed with the ROM signal by gate R4 to enable bi-directional data bus buffer F2 to pass data. When I/OS is high, data buffer F2 is turned off, which allows custom audio chips B3 and C/D3 to pass data to the data bus.

**I/O0**

I/O0 is an active low-level signal software-generated by Address Decoder R2 at address 6800. I/O0 is the chip-select enable for custom audio chip C/D3 in the Option Switch Input and Audio Output circuit.

**I/O1**

I/O1 is an active low-level signal software-generated by Address Decoder R2 at address 6000. I/O1 is the chip-select enable for custom audio chip B3 in the Option Switch Input and Audio Output circuit.

**LATCH**

Latch is an active low-level signal generated by Address Decoder P3 at address 8800. LATCH is the clock signal for latch R9 in the Coin Door and Control Panel Output circuit. When low, LATCH allows the data bits on lines DB0-DB7 to pass through R9.

**LATCH0**

Latch 0 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH0 is applied through inverter F7 to the S0 input pins of shift registers F8 and J8 in the Vector Data Shifters circuit. LATCH0 causes the data bits on lines DVG0-DVG7 to be latched by F8 and J8 to lines DVY0-DVY7 when F8 and J8 are clocked by the 12-MHz clock signal.

**LATCH1**

Latch 1 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH1 is applied through inverter F7 to the S0 input pin of shift register H8 in the Vector Data Shifters circuit. LATCH1 causes the data bits on lines DVG0-DVG3 to be latched by H8 to lines DVY8-DVY10 when H8 is clocked by the 12-MHz clock signal.

LATCH1 is also the clear signal for Vector Data Shifters A8, B8, C8, F8, J8, and for Op Code and Intensity Latch C6.

In addition, LATCH1 is the clock signal for Op Code and Intensity Latch D6. When LATCH1 goes low, the data bits on lines DVG4-DVG7 are latched by D6 to lines OP0-OP2, OP0-OP2, DVY12, and DVY12.

**LATCH2**

Latch 2 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH2 is applied through inverter F7 to the S0 input pins of shift registers A8 and C8 in the Vector Data Shifters circuit. LATCH2 causes the data bits on lines DVG0-DVG7 to be latched by A8 and C8 to lines DVX3-DVX7 when A8 is clocked by the 12-MHz clock signal.

**LATCH3**

Latch 3 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH3 is applied through inverter F7 to the S0 input pin of shift register B8 in the Vector Data Shifters circuit. LATCH3 causes the data bits on lines DVG0-DVG3 to be latched by B8 to lines DVX8-DVX11 when B8 is clocked by the 12-MHz clock signal.

LATCH3 is also the clock signal for Op Code and Intensity Latch C6. When LATCH3 goes low, the data bits on lines DVG4-DVG7 are latched by C6 to lines Z0-Z2, Z1-Z2, DVX12, and DVX12.

**NORM**

The active high-level Normalization Flag is software-generated by latch A6 in the Normalization Flag circuit. If OP0 is high, NORM is set high when STROBE0 goes high. NORM is gated with SCALE by gate K5 in the Vector Timer circuit to produce the load-enable signal for Vector Timers M6, N6, P6, and R6. If the Vector Timers are enabled, NORM initiates the divide-by-$2^n$ operation of the vector drawing time. (The n factor is specified by the data on lines DVY8-DVY10 to Vector Scaling latch D7.)

**OPTION 0-OPTION 2**

The Option 0, Option 1, and Option 2 signals are hardware-generated by DIP switch P10. They are applied to switch input buffer L9 of the Coin Door and Control Panel Input circuit. When L9 is enabled by SINP2, OPTION 0-OPTION 2 are passed to Buffered Microprocessor Data Bus lines DB5-DB7.

**OP0**

The Op Code 0 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. If the data on line DVG5 is high, OP0 is set high when D6 is clocked by LATCH1. OP0 is multiplexed with AM4 by N3 in the State Machine circuit to produce the A4 input address bit for State Machine ROM N4.

If OP0 is high, HALT from Halt Flag latch L5 is set high when L5 is clocked by STROBE3.

If OP0, OP2, STROBE3, and VGCK are all low, VCTR from Vector Flag latch E5 is set high when E5 is clocked by the 12-MHz clock signal.

**OP0**

The Complementary Op Code 0 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. This signal is opposite in state to OP0. If OP0 is low, NORM from Normalization Flag latch A6 is set high when STROBE0 clocks A6. OP0 is also the OP0 and OPX input signal for Vector Address Controller J9.

**OP1**

The Op Code 1 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. If the data on line DVG6 is high, OP1 is set high when D6 is clocked by LATCH1. OP1 is multiplexed with AM5 by N3 in the State Machine circuit to produce the A5 input address bit for State Machine ROM N4. In addition, OP1 is the OP1 signal for Vector Address Controller J9.

In the Vector Timer circuit, OP1 is gated by K5 and E3 to enable a 1 to be loaded into the D input pin of Vector Timer P6 (if NORM or SCALE is low).

**OP1**

The Complementary Op Code 1 signal is sofware-generated by latch D6 in the Op Code and Intensity Latches circuit. This signal is opposite in state to OP1. OP1 is the clear signal for Vector Timers N6 and M6. When OP1 goes low, the count from N6 and M6 is stopped, causing a lowered count from the Vector Timer circuit. This low count is used to draw short vectors on the display. OP1 is also gated with the outputs of the Vector Timers by gates L3 and H3 to set STOP to the low level.

**OP2**

The Op Code 2 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. If the data on line DVG7 is high, OP2 is set high when D6 is clocked by LATCH1. OP2 is multiplexed with AM6 by N3 in the State Machine circuit to produce the A6 input address bit for State Machine ROM N4.

If OP2, OP0, STROBE3, and VGCK are all low, VCTR from Vector Flag latch E5 is set high when E5 is clocked by the 12-MHz clock signal.

When STROBE1 goes low, if OP2 is low, it is applied through gates B7 and F3 of the Vector Scaling circuit as the load signal for counter C7. This allows the data latched from DVY8-DVY10 by D7 to be loaded into counter C7. When STROBE1 goes high, counter C7 counts down until it reaches the minimum count. At the same time, the Vector Timer circuit does a divide-by-2 (shift right) operation for each count of C7. (This is caused by SCALE being at the high state.) When C7 reaches its minimum count, it sets pin 12 high, dropping SCALE to the low state.

If OP2 and DVY12 are low, SCALELD from gate J6 is set low when STROBE2 goes low. This allows Vector Scaling latch D7 to latch the new data on DVY8-DVY10.

If OP2 and DVY12 are low, STATCLK from J6 is set low when STROBE2 goes low. This allows latch E6 of the Z Intensity and Blanking circuit to latch the data on DVY4-DVY7.

**OP2**

The Complementary Op Code 2 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. This signal is opposite in state to OP2. If OP2, STROBE3, and VGCK are low, CNTR from Center Flag latch E5 is set high when E5 is clocked by the 12-MHz clock signal. OP2 is also ORed with SA by gate R4 to produce the OP2 input for Vector Address Controller J9.

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**Black Widow PCB Signal Name Descriptions**



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# Black Widow PCB Signal Name Descriptions, cont.

**PLAYER 1 LED**

The Player 1 LED On signal is developed from the data bit on line DB4. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on line DB4 to pin 19 of R9. This signal is applied through R103 to light the Player 1 LED on the game Control Panel.

**PLAYER 2 LED**

The Player 2 LED On signal is developed from the data bit on line DB5. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB5 to pin 16 of R9. This signal is applied through R102 to light the Player 2 LED on the game Control Panel.

**POR**

The active high-level Power-On Reset signal is hardware-generated at pin 4 of F7 in the Power-On Reset circuit. POR is the clock signal that starts the count of E4 of the Clock circuit.

**$\overline{\text{POR}}$**

The active low-level Power-On Reset signal is hardware-generated at pin 6 of inverter F7 in the Power-On Reset circuit. $\overline{\text{POR}}$ is generated when the voltage at pin 3 of R8 is less than about 7 volts or when the RESET test point is shorted to ground. $\overline{\text{POR}}$ is developed into the $\overline{\text{RESET}}$ signal to protect Microprocessor C2.

**$\overline{\text{RAM}}$**

The Random-Access Memory Enable is an active low-level signal software-generated by Address Decoder R2 during addresses 0000 through 07FF. $\overline{\text{RAM}}$ is the chip-enable signal for Random-Access Memory N/P1. When low, $\overline{\text{RAM}}$ allows data to be read from or written to N/P1, depending upon the state of $\overline{\text{WRITE}}$.

**RED**

Red is a game PCB output signal developed from the data on line DVY2 in the R-G-B Output circuit. When DVY2 is high and latch K10 is clocked by $\overline{\text{STATCLK}}$, the data bit on DVY2 is inverted and latched to pin 3 of K10. If both BLANK and Z BLANK are low, this data bit is again inverted by gate L10 to turn on Q6. Transistor Q6 generates the RED signal for the display.

**$\overline{\text{RESET}}$**

Reset is an active low-level signal generated at pin 6 of K3 from either the Watchdog circuit or the Power-On Reset circuit. The Power-On Reset circuit sets $\overline{\text{RESET}}$ to an active low level either when the RESET test point is shorted to ground or during the time that the power-supply voltages are reaching their stabilized, regu-lated levels. This ensures that the Microprocessor Address Bus is stabilized before the microprocessor begins operation.

The Watchdog circuit sets $\overline{\text{RESET}}$ to an active low level if the microprocessor fails to output address 0D00 before Watchdog counter H4 has reached its maximum count.

$\overline{\text{RESET}}$ is also the clear signal for latch R9 in the Coin Door and Control Panel Output circuit.

In addition, RESET is gated with $\overline{\text{VGRST}}$ by gate L6 in the Halt Flag circuit to produce $\overline{\text{DISRST}}$.

**ROM**

The Read-Only Memory Enable is an active high-level signal software-generated from Address Decoder R1 during addresses 9000 through 9FFF. ROM is ORed with $\overline{\text{I/OS}}$ by gate R4 to enable bi-directional data bus buffer F2 to pass data.

In addition, ROM is ANDed with $\overline{\text{DIS DAT}}$ to enable data buffer E2.

**$\overline{\text{ROM0}}$**

Read-Only Memory Chip Select 0 is an active low-level signal software-generated by Address Decoder R1 at addresses 9000-9FFF. $\overline{\text{ROM0}}$ is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM0}}$ allows ROM D1 to be addressed and to pass data to buffer E2.

**$\overline{\text{ROM1}}$**

Read-Only Memory Chip Select 1 is an active low-level signal software-generated by Address Decoder R1 at addresses A000-AFFF. $\overline{\text{ROM1}}$ is the chip-select signal for ROM E/F1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM1}}$ allows ROM E/F1 to be addressed and to pass data to buffer E2.

**$\overline{\text{ROM2}}$**

Read-Only Memory Chip Select 2 is an active low-level signal software-generated by Address Decoder R1 at addresses B000-BFFF. $\overline{\text{ROM2}}$ is the chip-select signal for ROM H1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM2}}$ allows ROM H1 to be addressed and to pass data to buffer E2.

**$\overline{\text{ROM3}}$**

Read-Only Memory Chip Select 3 is an active low-level signal software-generated by Address Decoder R1 at addresses C000-CFFF. $\overline{\text{ROM3}}$ is the chip-select signal for ROM J1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM3}}$ allows ROM J1 to be addressed and to pass data to buffer E2.

**$\overline{\text{ROM4}}$**

Read-Only Memory Chip Select 4 is an active low-level signal software-generated by Address Decoder R1 at addresses D000-DFFF. $\overline{\text{ROM4}}$ is the chip-select signal for ROM K/L1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM4}}$ allows ROM K/L1 to be addressed and to pass data to buffer E2.

**$\overline{\text{ROM5}}$**

Read-Only Memory Chip Select 5 is an active low-level signal software-generated by Address Decoder R1 at addresses E000-EFFF. $\overline{\text{ROM5}}$ is the chip-select signal for ROM M1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM5}}$ allows ROM M1 to be addressed and to pass data to buffer E2.

**R/$\overline{\text{WB}}$**

The Buffered Read/Write Enable is generated by Microprocessor C2, buffered by B1, and applied as the read/write enable signal for custom audio chips B3 and C/D3 of the Option Switch Input and Audio Output circuit. In the high state, R/$\overline{\text{WB}}$ is the read enable for the custom audio chips; in the low state, it is the write enable for these chips.

**$\overline{\text{R}}$/WB**

The Buffered Read/Write Eanble is generated at pin 2 of F3 in the Microprocessor circuit by inverting R/$\overline{\text{WB}}$. $\overline{\text{R}}$/WB is ANDed with BΦ2 and 3 MHz by gate K4 to produce $\overline{\text{WRITE}}$. $\overline{\text{R}}$/WB is the direction signal for Vector Memory Data Buffer P8 and determines the direction of data flow through P8. In the high state, $\overline{\text{R}}$/WB allows data to pass through P8 from the data bus to the vector generator data bus; in the low state, it allows data to pass in the reverse direction.

**SA**

The active high-level Signature Analysis Flag signal is hardware-generated at pin 12 of inverter J3 when test point $\overline{\text{SA}}$ at pin 13 is grounded. SA is used to place the game PCB in the mode to generate signatures for reading by a Signature Analyzer or the ATARI CAT Box.

**$\overline{\text{SA}}$**

The active low-level Signature Analysis Flag is hardware-generated when test point $\overline{\text{SA}}$ at pin 13 of J3 is grounded. $\overline{\text{SA}}$ is used to place the game PCB in the mode to generate signatures for reading by a Signature Analyzer or the ATARI CAT Box.

**SACLK**

Signature Analysis Clock is a test point at pin 8 of gate B7 in the State Machine Clock Logic circuit. SACLK is used to apply the clock signal from the Signature Analyzer or ATARI CAT Box for the reading of game PCB signatures.

**SAEN**

Signature Analysis Enable is a test point at pin 8 of gate M5 in the Vector Address Selector circuit. SAEN is generated by gating $\overline{\text{VRAM}}$ with the data bit on line AM10 by gates J3 and M5. SAEN is used to enable a Signature Analyzer or the ATARI CAT Box for the reading of game PCB signatures.

**SCALE**

Scale is an active high-level signal generated by gate B7 of the Vector Scaling circuit. When OP2 is high and counter C7 is counting down, SCALE is set high. SCALE is ORed with NORM by gate K5 of the Vector Timer circuit to produce the load signal for Vector Timers M6, N6, P6, and R6. When SCALE is high, the Vector Timers perform a load operation for each count of C7 (at a 12-NHz rate). This results in a vector drawing time divided by a factor of $2^n$, where n equals the total counts of C7. When C7 reaches its minimum count, SCALE is set low.

SCALE is gated with VCTR, CNTR, DVY11-DVY12, and DVX11-DVX12 of the Normalization Flag circuit to produce the clear signal for latch A6.

**$\overline{\text{SCALELD}}$**

Scale Load is an active low-level signal software-generated by gates N5, L3, and L6 of the Vector Generator circuit. When $\overline{\text{STROBE2}}$, OP2, and $\overline{\text{DVY12}}$ are all low, $\overline{\text{SCALELD}}$ is set low. $\overline{\text{SCALELD}}$ is the clock signal for Vector Scaling latch D7. When $\overline{\text{SCALELD}}$ goes high, the data on lines DVY8-DVY10 are latched to the output pins of D7.

**$\overline{\text{SINP1}}$**

Switch Input 1 is an active low-level signal software-generated by Address Decoder R2 at address 7800. $\overline{\text{SINP1}}$ is the direction signal for bi-directional data buffer M9 of the Coin Door and Control Panel Input circuit and determines the direction of data flow through buffer M9.

**$\overline{\text{SINP2}}$**

Switch Input 2 is an active low-level signal software-generated by Address Decoder R2 at address 8000. $\overline{\text{SINP2}}$ is the direction signal for bi-directional data buffer L9 of the Coin Door and Control Panel Input circuit and determines the direction of data flow through buffer L9.

**$\overline{\text{STATCLK}}$**

State Clock is an active low-level signal software-generated by gates N5, L3, and J6 of the Vector Generator circuit. When $\overline{\text{STROBE2}}$, OP2, and DVY12 are all low, $\overline{\text{STATCLK}}$ is set low. $\overline{\text{STATCLK}}$ is the clock for latch K10 in the R-G-B Output circuit and latch E6 in the Z Intensity and Blanking circuit. When $\overline{\text{STATCLK}}$ goes high, the data bits on DVY0-DVY2 are latched by K10, and those on DVY4-DVY7 are latched by E6.

**$\overline{\text{STOP}}$**

Stop is an active low-level signal generated by gate H3 of the Vector Timer circuit. $\overline{\text{STOP}}$ is set low when Vector Timers N6, M6, P6, and R6 have reached their maximum count. If $\overline{\text{STOP}}$ is low, VCTR from Vector Flag latch E5 and CNTR from Center Flag latch E5 are both set low when E5 is clocked by the 12-MHz clock signal.

**$\overline{\text{STROBE0}}$**

Strobe 0 is an active low-level signal software-generated by State Machine decoder H7. $\overline{\text{STROBE0}}$ is the clock signal for Normalization Flag latch A6. It is also the $\overline{\text{STROBE0}}$ input for Vector Address Controller J9.

**$\overline{\text{STROBE1}}$**

Strobe 1 is an active low-level signal software-generated by State Machine decoder H7. If OP2 is low, when $\overline{\text{STROBE1}}$ goes low, the data latched at the outputs of D7 in the Vector Scaling circuit are loaded into counter C7. When $\overline{\text{STROBE1}}$ goes high, C7 begins counting down.

$\overline{\text{STROBE1}}$ is the $\overline{\text{STROBE1}}$ input for Vector Address Controller J9.

**$\overline{\text{STROBE2}}$**

Strobe 2 is an active low-level signal software-generated by State Machine decoder H7. If OP2 and $\overline{\text{DVY12}}$ are both low, $\overline{\text{SCALELD}}$ from gate J6 is set low when $\overline{\text{STROBE2}}$ goes low. If OP2 and DVY12 are both low, $\overline{\text{STATCLK}}$ is set low when $\overline{\text{STROBE2}}$ goes low.

$\overline{\text{STROBE2}}$ is the $\overline{\text{STROBE2}}$ input for Vector Address Controller J9.

**$\overline{\text{STROBE3}}$**

Strobe 3 is an active low-level signal software-generated by State Machine decoder H7. $\overline{\text{STROBE3}}$ is the clock signal for Halt Flag latch L5 and is the $\overline{\text{STROBE3}}$ input for Vector Address Controller J9.

If OP0, OP2, $\overline{\text{OP2}}$, and VGCK are all low, VCTR from Vector Flag latch E5 and CNTR from Center Flag latch E5 are both set high when $\overline{\text{STROBE3}}$ goes low.

**ST0-ST2**

State signals ST0-ST2 are active high-level signals that are software-generated by State Machine ROM N4. These signals, together with ST3, are decoded by H7 of the State Machine circuit to produce $\overline{\text{LATCH0}}$-$\overline{\text{LATCH3}}$ and $\overline{\text{STROBE0}}$-$\overline{\text{STROBE3}}$. ST2 is used to develop ST3 and is also the ST2 input for Vector Address Controller J9.

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**Black Widow PCB Signal Name Descriptions**



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## Black Widow PCB Signal Name Descriptions, cont.

**ST3**

State signal ST3 is an active high-level signal hardware-generated by Decoder Disable latch A7. ST3 is opposite in state to VGCK, and is delayed by one pulse of the 12-MHz clock signal if the Q4 output from State Machine ROM N4 is low and $\overline{\text{VMEM}}$ is high. If the Q4 output from N4 is high, ST3 is high. When ST3 is high, State Machine decoder H7 is disabled. When ST3 is low, H7 decodes the data on lines ST0-ST2 to produce $\overline{\text{LATCH0}}$-$\overline{\text{LATCH3}}$ and $\overline{\text{STROBE0}}$-$\overline{\text{STROBE3}}$.

**VCTR, $\overline{\text{VCTR}}$**

The Vector Flag signals are software-generated by Vector Flag latch E5. If OP0, OP2, $\overline{\text{STROBE3}}$, and VGCK are low and $\overline{\text{HALT}}$ is high, VCTR is set high and $\overline{\text{VCTR}}$ is set low when E5 is clocked by the 12-MHz clock signal. VCTR is ORed with CNTR by gate M5 to set GO high.

SCALE, CNTR, DVY11-DVY12, and DVX11-DVX12 are gated with VCTR to produce the clear signal for Nomalization Flag latch A6.

In the Z Intensity and Blanking circuit, VCTR is the clock signal for latch H6 and the serial input signal for shift register M3.

VCTR and $\overline{\text{VCTR}}$ are used by the DAC Reference and Bipolar Current Sources circuit to set the X BIP, Y BIP, X REF, and Y REF levels.

**VGCK**

The Vector Generator clock signal is generated at pin 18 of buffer B1 in the Microprocessor circuit. VGCK is derived from the 1.5 MHz clock signal and is applied to AND gate J5 of the State Machine Clock Logic circuit. VGCK is the basic timing signal of the State Machine circuit.

**$\overline{\text{VGGO}}$**

The Vector Generator Go signal is an active low-level signal software-generated by Address Decoder P3 at address 8840. $\overline{\text{VGGO}}$ is the clear signal for latch L5 of the Halt Flag circuit. When low, $\overline{\text{VGGO}}$ sets HALT to the inactive low level.

**$\overline{\text{VGRST}}$**

Vector Generator Reset is an active low-level signal software-generated by Address Decoder P3 at address 8880. $\overline{\text{VGRST}}$ is ORed with $\overline{\text{RESET}}$ by gate L6 of the Halt Flag circuit to produce $\overline{\text{DISRST}}$.

**$\overline{\text{VMEM}}$**

The Vector Memory Select Enable is an active low-level signal software-generated by Address Decoder R1 during addresses 2000 through 5FFF. $\overline{\text{VMEM}}$ is the select-enable signal for Vector Address Selectors K8, L8, M8, and N8. When low, $\overline{\text{VMEM}}$ allows the Vector Address Selectors to produce $\overline{\text{VW}}$, $\overline{\text{BUFFEN}}$, and the AM0-AM12 multiplexed address bits. $\overline{\text{VMEM}}$ is also applied to gate K5 of the State Machine Clock Logic circuit where it is used to generate ST3.

**$\overline{\text{VRAM}}$**

The Vector Random-Access Memory Chip Enable is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 2000-27FF. When low, $\overline{\text{VRAM}}$ enables Vector Random-Access Memory K7 to be addressed to either receive or transmit data, depending upon the state of $\overline{\text{VW}}$. $\overline{\text{VRAM}}$ is also used to produce the SAEN signal from M5 of the Vector Address Selector circuit.

**$\overline{\text{VROM0}}$**

Vector Read-Only Memory Chip Select 0 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 2800-2FFF. $\overline{\text{VROM0}}$ is the chip-select signal for ROM L7 of the Vector Read-Only Memory circuit. When low, $\overline{\text{VROM0}}$ allows ROM L7 to be addressed and to pass data to the Vector Generator Data Bus.

**$\overline{\text{VROM1}}$**

Vector Read-Only Memory Chip Select 1 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 3000-3FFF. $\overline{\text{VROM1}}$ is the chip-select signal for ROM M/N7 of the Vector Read-Only Memory circuit. When low, $\overline{\text{VROM1}}$ allows ROM M/N7 to be addressed and to pass data to the Vector Generator Data Bus.

**$\overline{\text{VROM2}}$**

Vector Read-Only Memory Chip Select 2 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 4000-4FFF. $\overline{\text{VROM2}}$ is the chip-select signal for ROM N/P7 of the Vector Read-Only Memory circuit. When low, $\overline{\text{VROM2}}$ allows ROM N/P7 to be addressed and to pass data to the Vector Generator Data Bus.

**$\overline{\text{VROM3}}$**

Vector Read-Only Memory Chip Select 3 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 5000-5FFF. $\overline{\text{VROM3}}$ is the chip-select signal for ROM R7 of the Vector Read-Only Memory circuit. When low, $\overline{\text{VROM3}}$ allows ROM R7 to be addressed and to pass data to the Vector Generator Data Bus.

**$\overline{\text{VW}}$**

The Vector Write Enable is an active low-level signal software-generated from Vector Address Selector K8, ANDed with $\overline{\text{B}\Phi 2}$ by gate J6, and applied as the write-enable signal for Vector Random-Access Memory K7. When low, $\overline{\text{VW}}$ allows data to be written to K7; when high, $\overline{\text{VW}}$ permits data to be read from K7.

**$\overline{\text{WDCLR}}$**

Watchdog Clear is an active low-level signal software-generated by Address Decoder P3 at address 8980. $\overline{\text{WDCLR}}$ is ORed with $\overline{\text{POR}}$ by gate E3 to clear the count of Watchdog counter H4.

**$\overline{\text{WDDIS}}$**

Watchdog Disable is a test point at pin 9 of AND gate L4 in the Watchdog circuit. When $\overline{\text{WDDIS}}$ is grounded, $\overline{\text{RESET}}$ is prevented from going to an active low level (except when the RESET test point is grounded).

**$\overline{\text{WRITE}}$**

Write Enable is an active low-level signal generated by gate K4 of the Microprocessor circuit. $\overline{\text{WRITE}}$ is used to enable Address Decoder P3 and Random-Access Memory N/P1. $\overline{\text{WRITE}}$ is also applied to pin 11 of K8 in the Vector Address Selector circuit to develop $\overline{\text{VW}}$.

**X BIP**

The X-Axis Bipolar Current is set by R99 of the DAC Reference and Bipolar Current Sources circuit. This is the current source for pin 18 of X-axis digital-to-analog converter (DAC) A/B9 of the X-Axis Output circuit.

**X OUT**

X Output is a game PCB output signal generated by the X-Axis Output circuit. X OUT carries the horizontal beam deflection signal for the drawing of vectors on the display.

**X REF**

The X-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 14 of X-axis digital-to-analog converter (DAC) A/B9 of the X-Axis Output circuit.

**Y BIP**

The Y-Axis Bipolar Current is set by R98 of the DAC Reference and Bipolar Current Sources circuit. This is the current source for pin 18 of Y-axis digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit.

**Y OUT**

Y Output is a game PCB output signal generated by the Y-Axis Output circuit. Y OUT carries the vertical beam deflection signal for the drawing of vectors on the display.

**Y REF**

The Y-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 14 of Y-axis digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit.

**Z0-Z2, $\overline{\text{Z1}}$-$\overline{\text{Z2}}$**

Z Intensity signals Z0-Z2 and $\overline{\text{Z1}}$-$\overline{\text{Z2}}$ are software-generated by latch C6 in the Op Code and Intensity Latches circuit. These signals are derived from the data on lines DVG51-DVG7 when C6 is clocked by $\overline{\text{LATCH3}}$. If the binary count carried by Z0-Z2 is not equal to 1, these signals are the input signals for latch F6 in the Z Intensity and Blanking circuit. If the binary count carried by Z0-Z2 is 1, Z Intensity signals Z0, $\overline{\text{Z1}}$, and $\overline{\text{Z2}}$ are ANDed by gate F5 of the Z Intensity and Blanking circuit to produce the select signal for latch F6. This select signal causes the latched data from E6 to be applied as the input signals for latch F6.

**Z OUT**

Z Intensity Output is a game PCB output signal generated by the Z Intensity and Blanking circuit from either DVY4-DVY7 or Z0-Z2. The Q output signals from latch H6 are summed at the base of Q7. Transistors Q7 and Q9 buffer Z OUT before it is sent to the game display circuitry to control the display intensity.

**3 KHZ**

The 3 kHz clock signal is generated at pin 6 of Clock counter F4 and is applied through switch input buffer M9 of the Coin Door and Control Panel Input circuit (when $\overline{\text{SINP1}}$ is low). The 3 kHz clock is read by the microprocessor on data line DB7. This frequency is the time reference for the Microprocessor C2.

**12 KHZ**

The 12 kHz clock signal is generated at pin 4 of Clock counter F4 and is applied to reset A4 of the High-Score Table.

**3 MHZ**

The 3 MHz clock signal is generated at pin 2 of Clock counter F4. The 3 MHz signal is ANDed with $\overline{\text{R/WB}}$ and B$\Phi$2 by gate K4 to produce $\overline{\text{WRITE}}$. It is also applied to AND gate J5 of the State Machine Clock Logic and to shift register M3 of the Z Intensity and Blanking circuit.

**6 MHZ**

The 6 MHz clock signal is generated at pin 3 of Clock counter F4 and is applied to gate J5 of the State Machine Clock Logic circuit.

**12 MHZ**

The 12 MHz clock signal is generated at pin 10 of inverter F3 in the Clock circuit. This signal clocks the Vector Timer Shifters, the Vector Flag latch, and the Center Flag latch.

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**Black Widow PCB Signal Name Descriptions**



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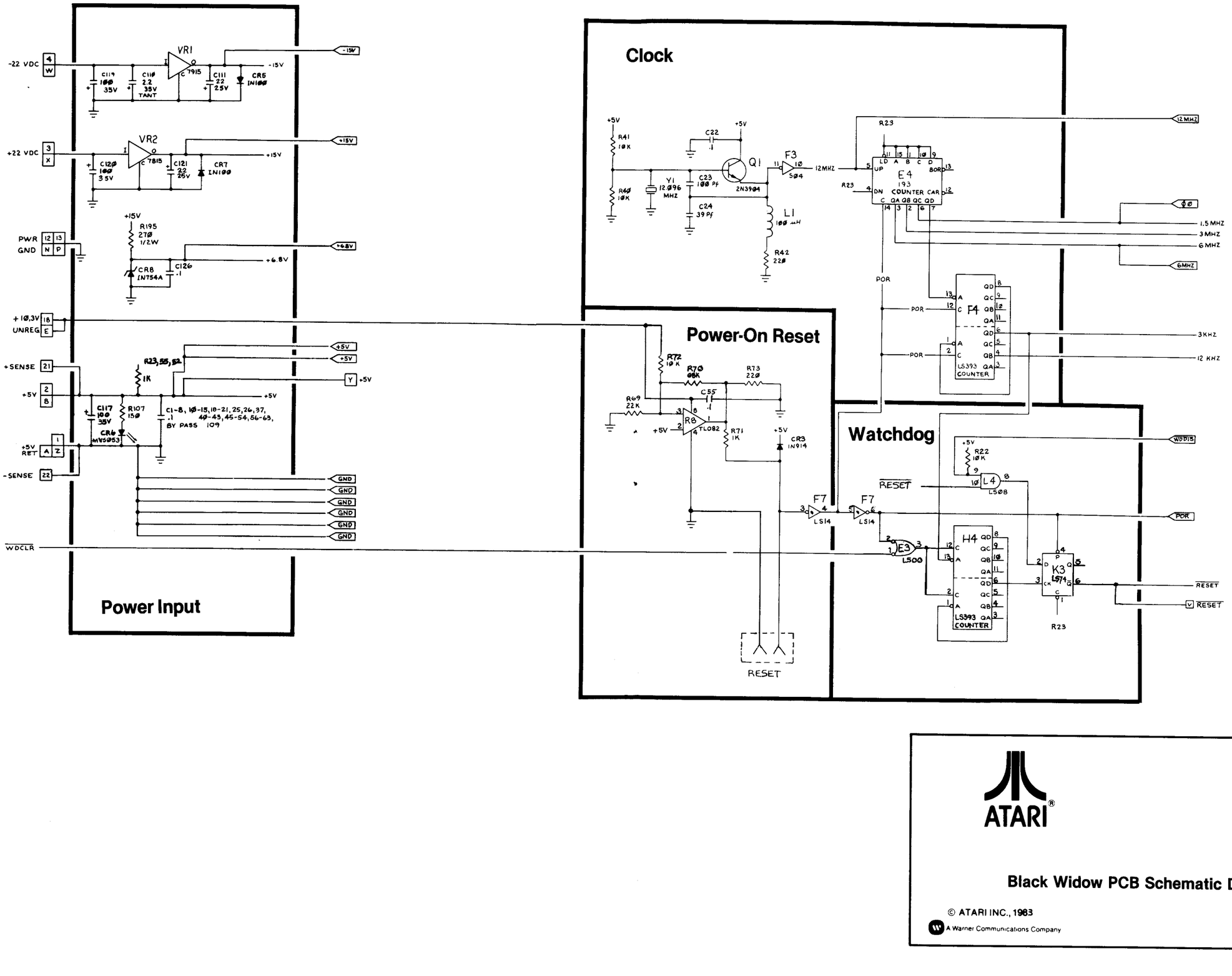


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## Black Widow PCB Schematic Diagram



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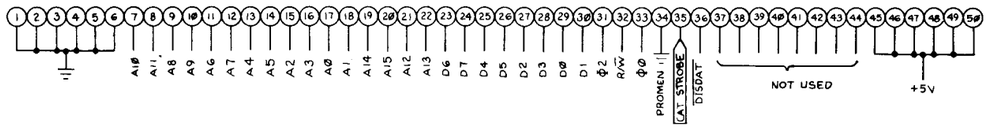
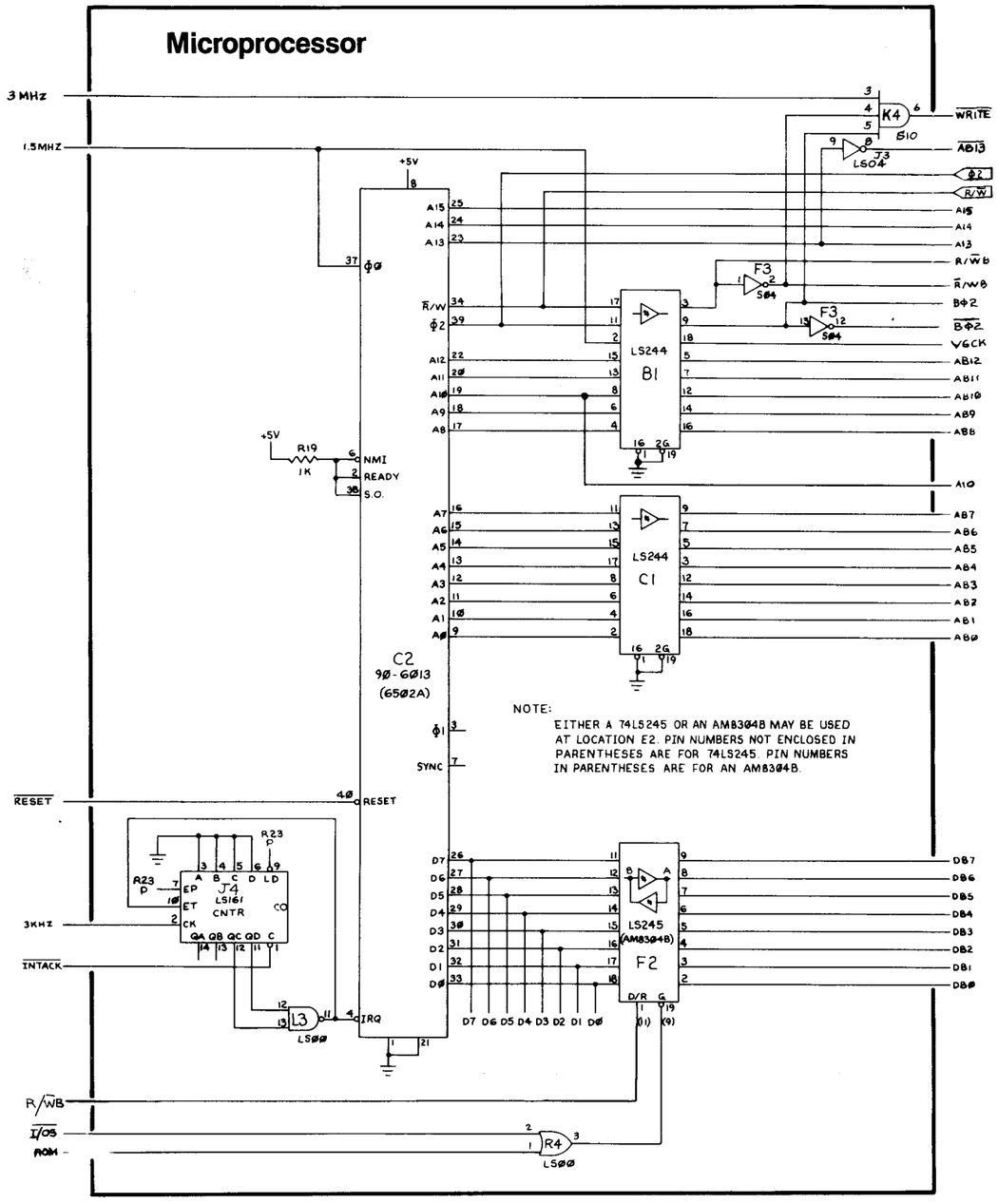
1st printing

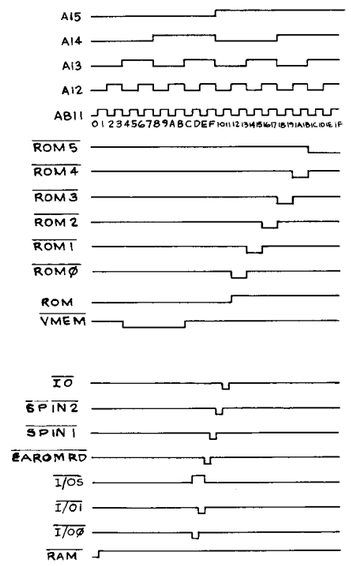
## Test Connector



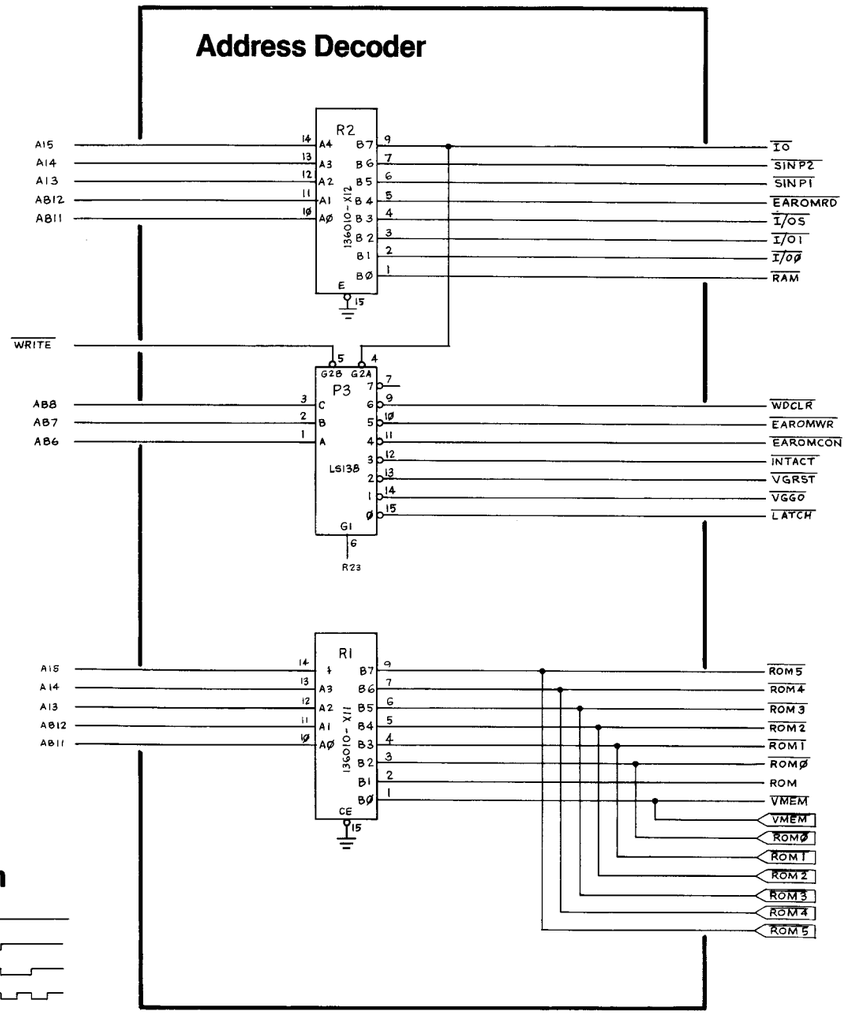

## Microprocessor




## Timing Diagram




## Address Decoder

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# Black Widow PCB Schematic Diagram



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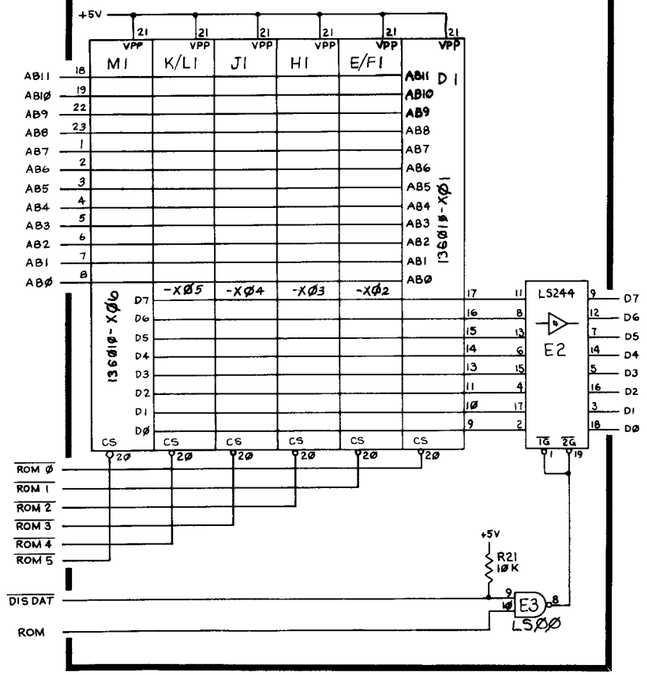
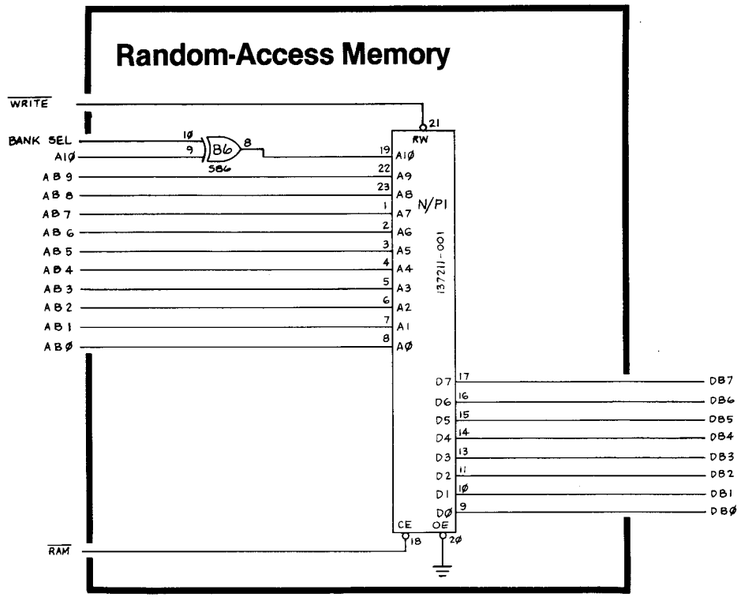
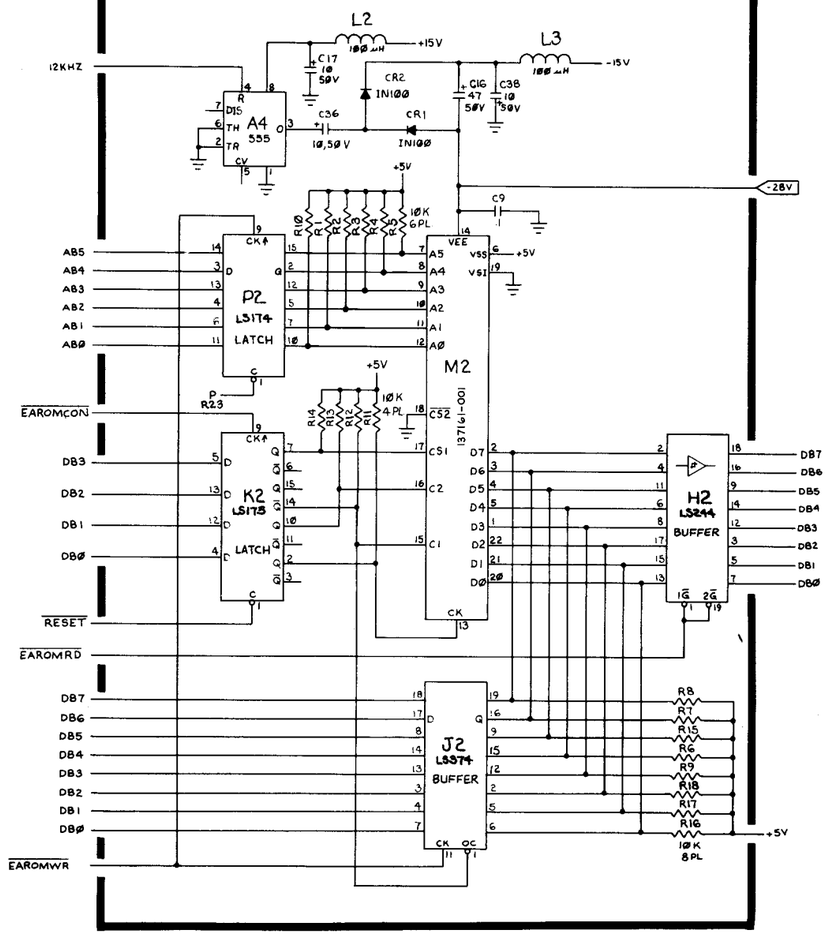
## Read-Only Memory




## Random-Access Memory




## High-Score Table

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# Black Widow PCB Schematic Diagram



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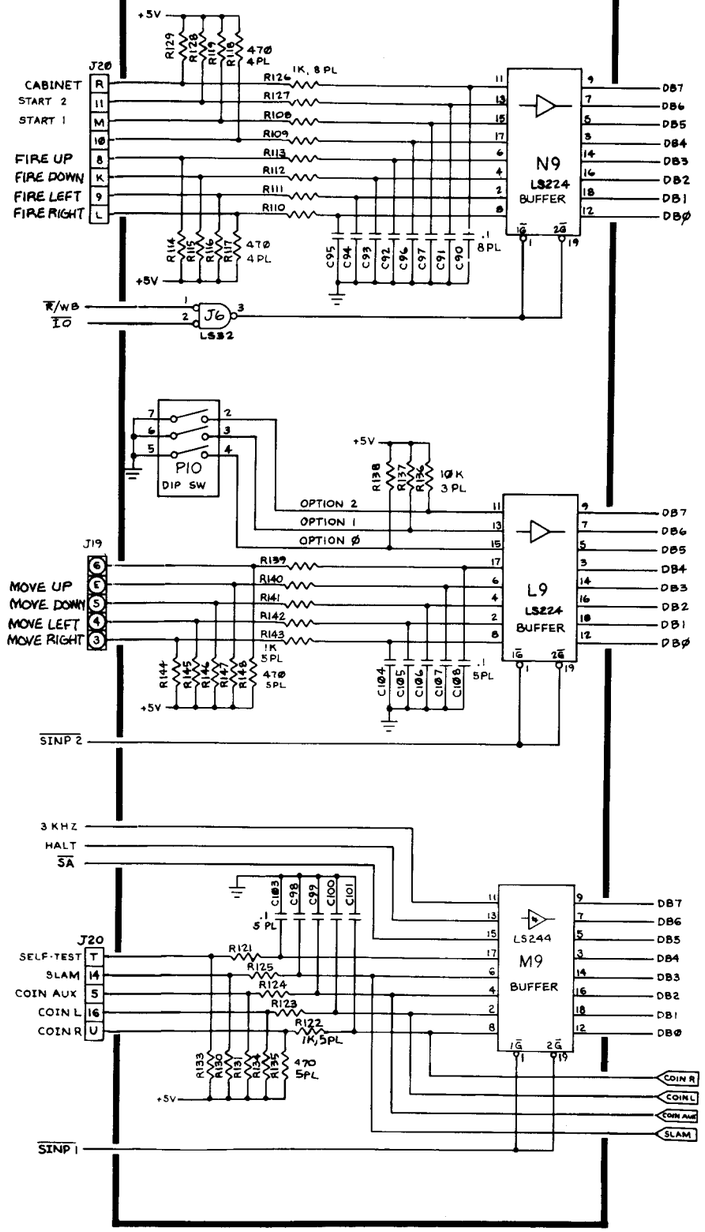
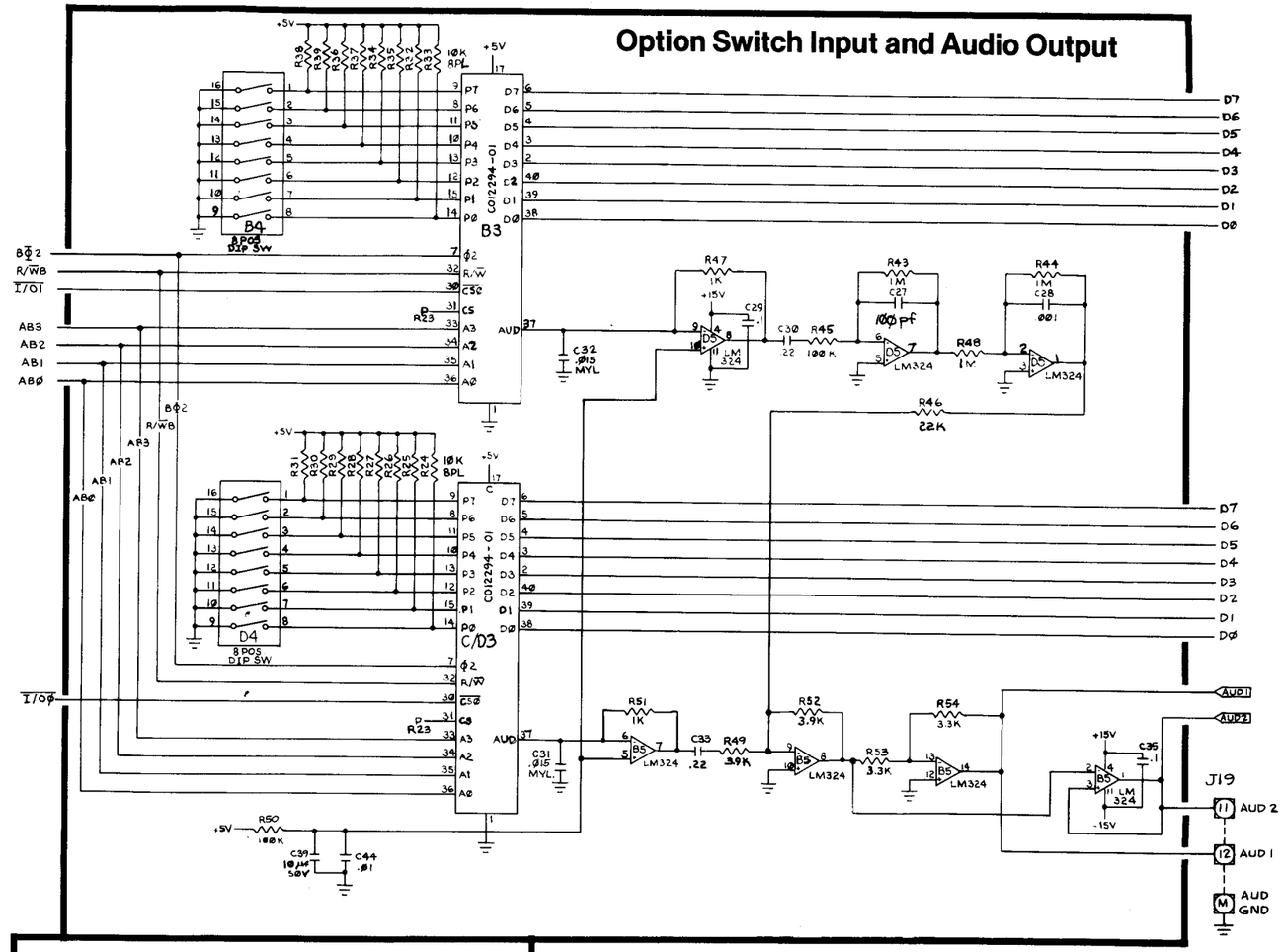
1st printing

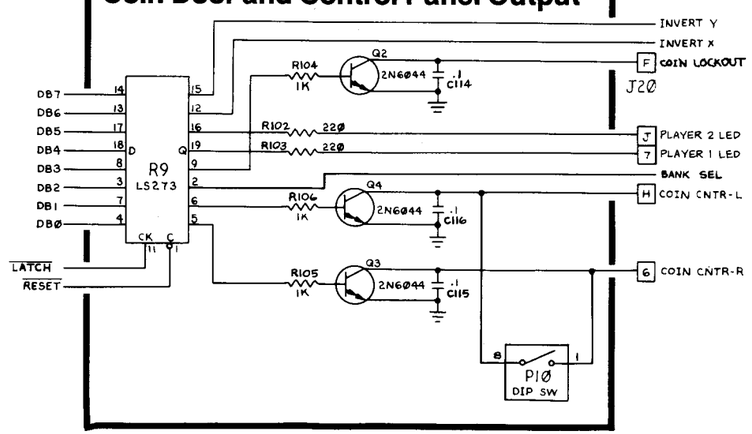
## Coin Door and Control Panel Input




## Option Switch Input and Audio Output




## Coin Door and Control Panel Output

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# Black Widow PCB Schematic Diagram



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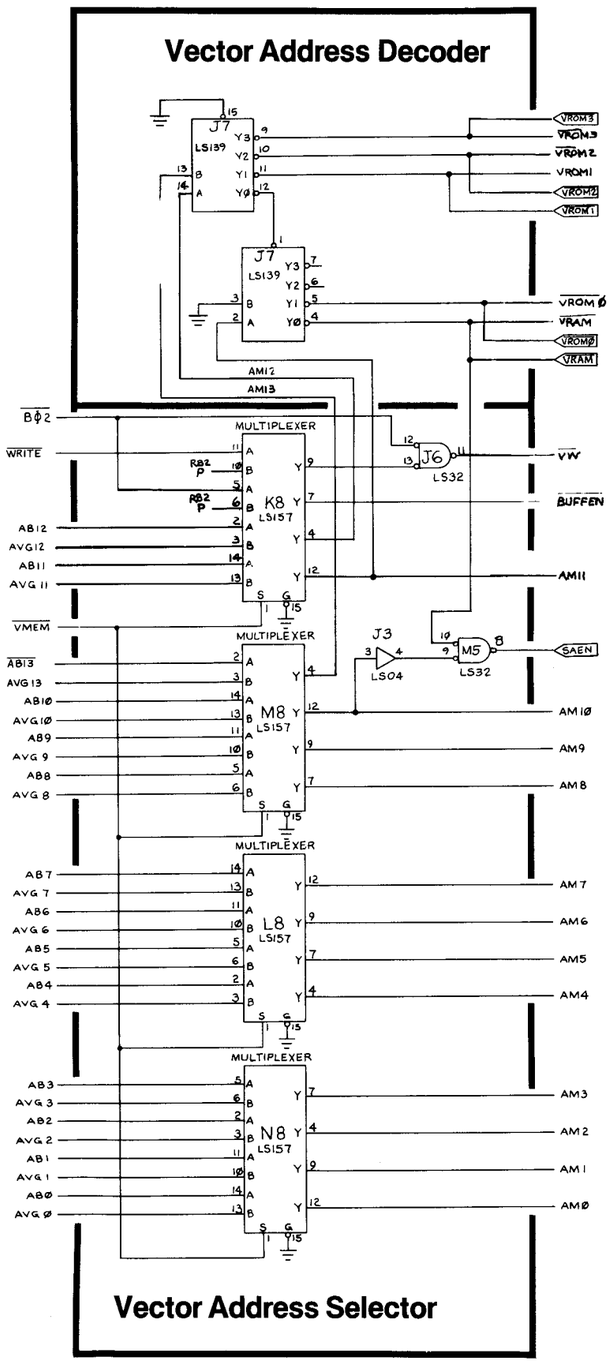
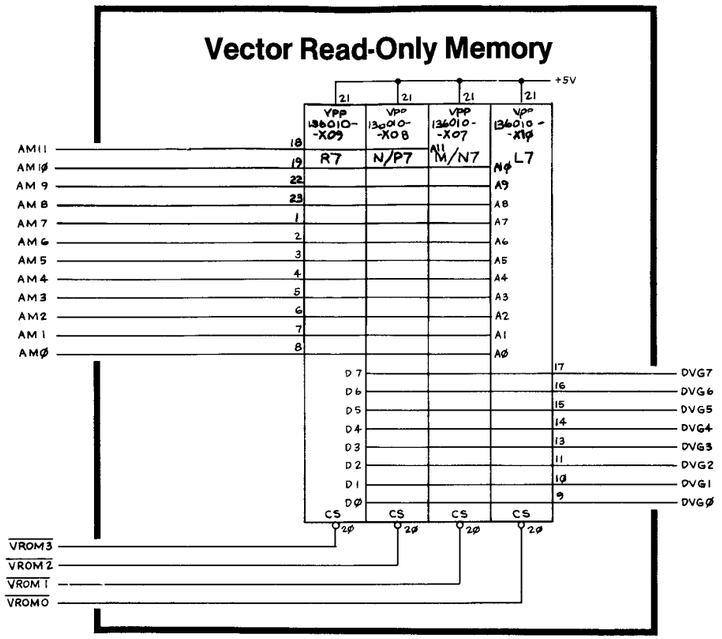
## Vector Address Decoder

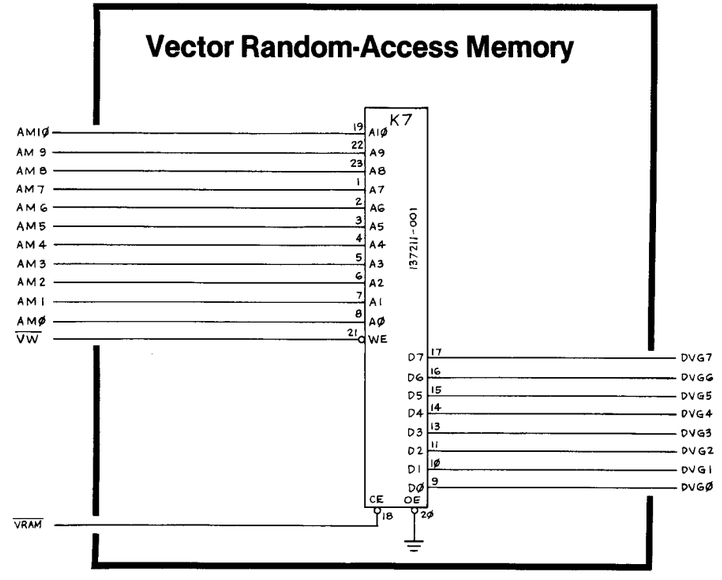



## Vector Address Selector

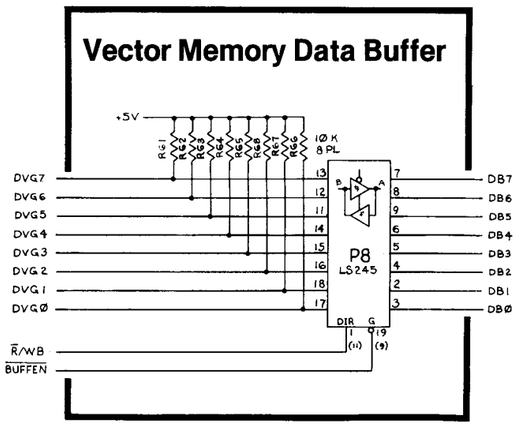
## Vector Read-Only Memory




## Vector Random-Access Memory




## Vector Memory Data Buffer

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# Black Widow PCB Schematic Diagram



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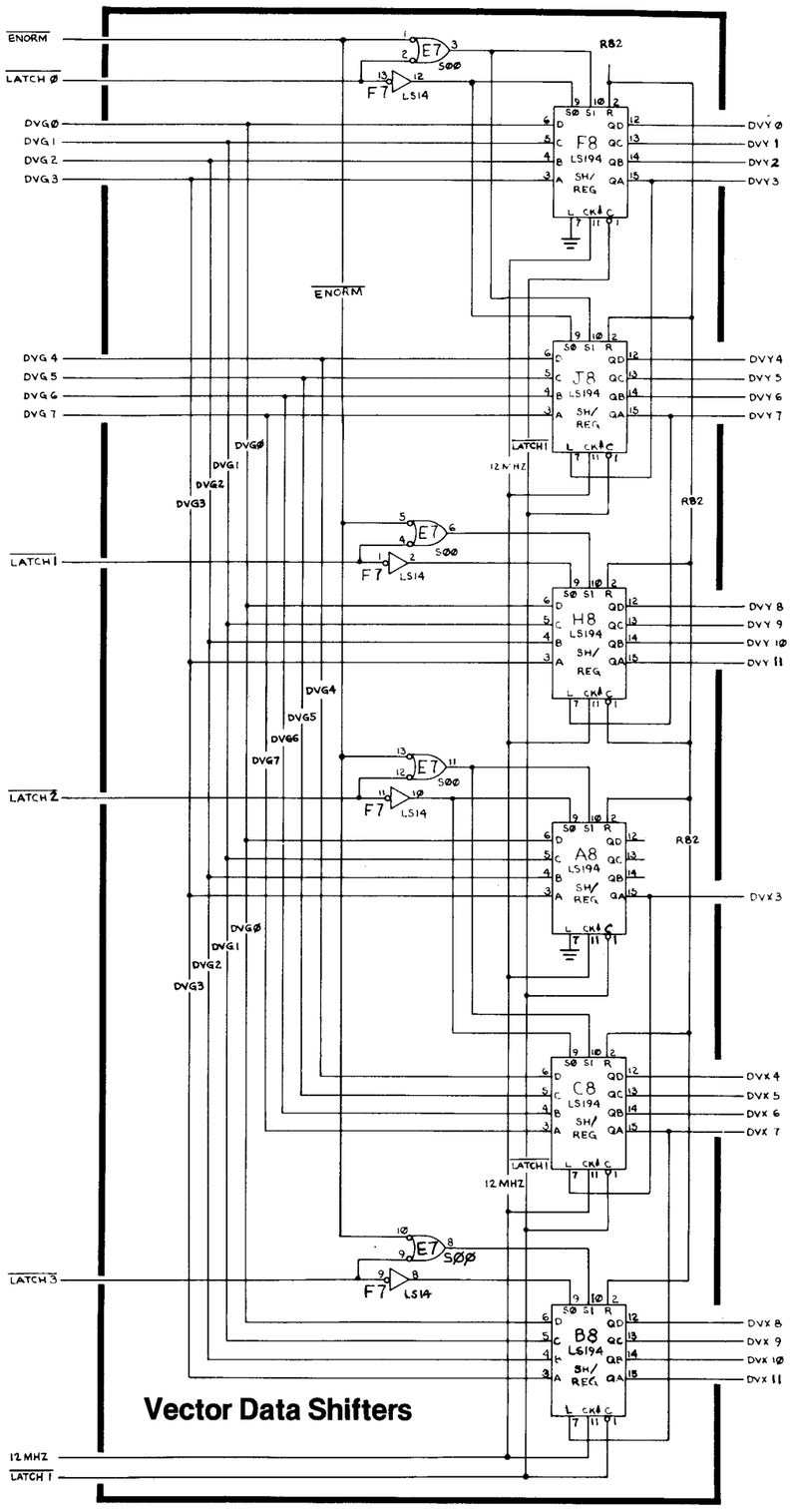
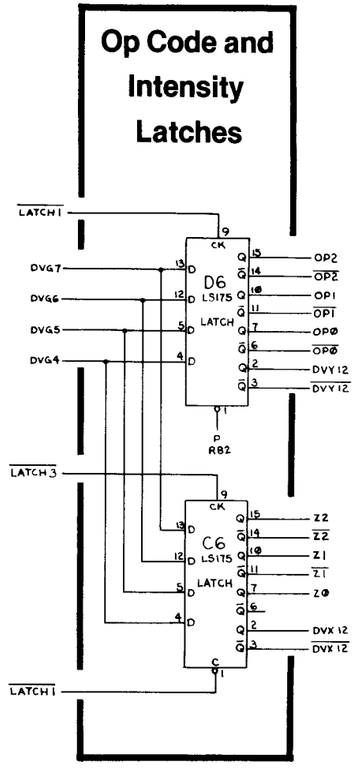
1st printing




## Vector Data Shifters




## Op Code and Intensity Latches

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# Black Widow PCB Schematic Diagram



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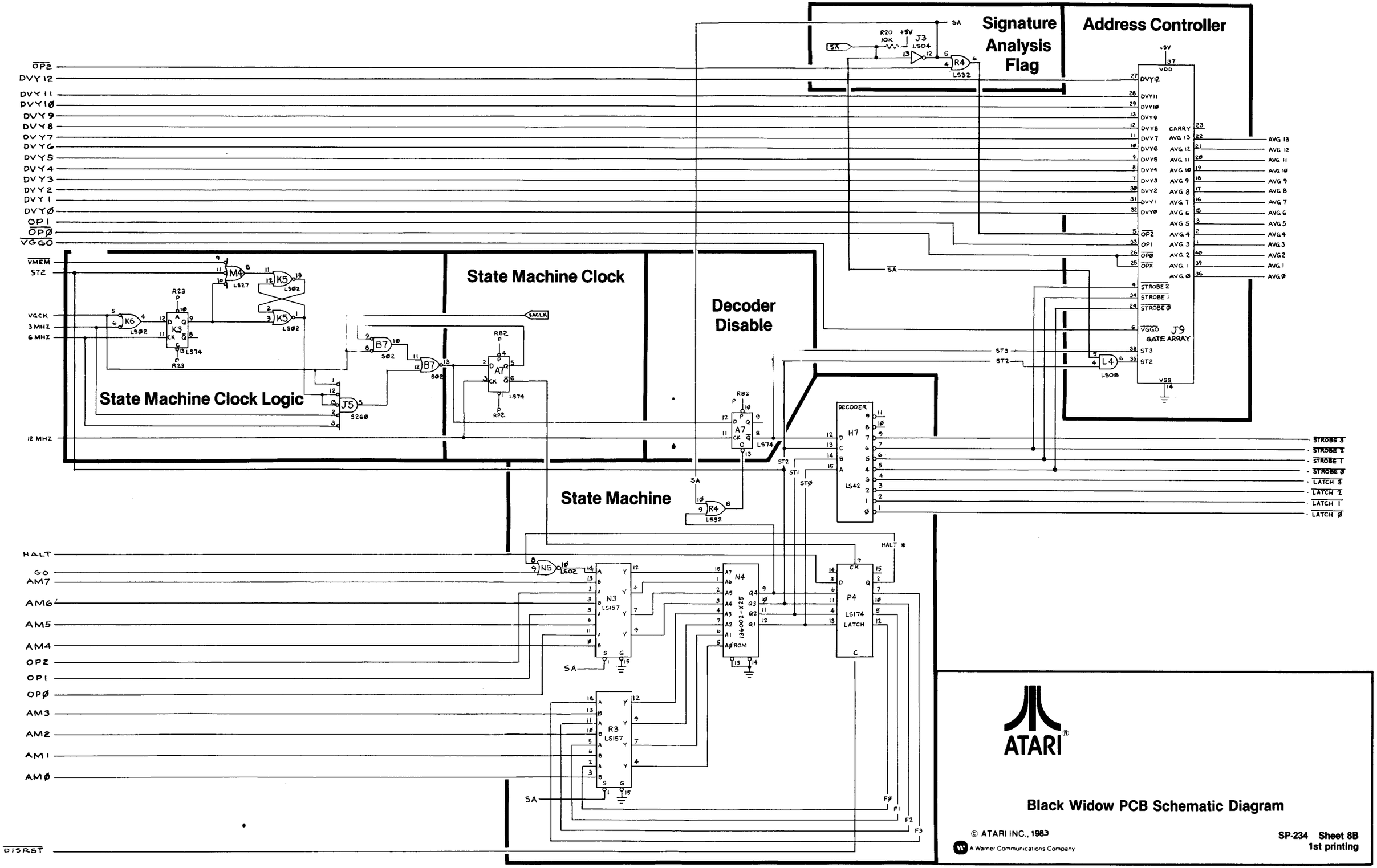


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# Black Widow PCB Schematic Diagram



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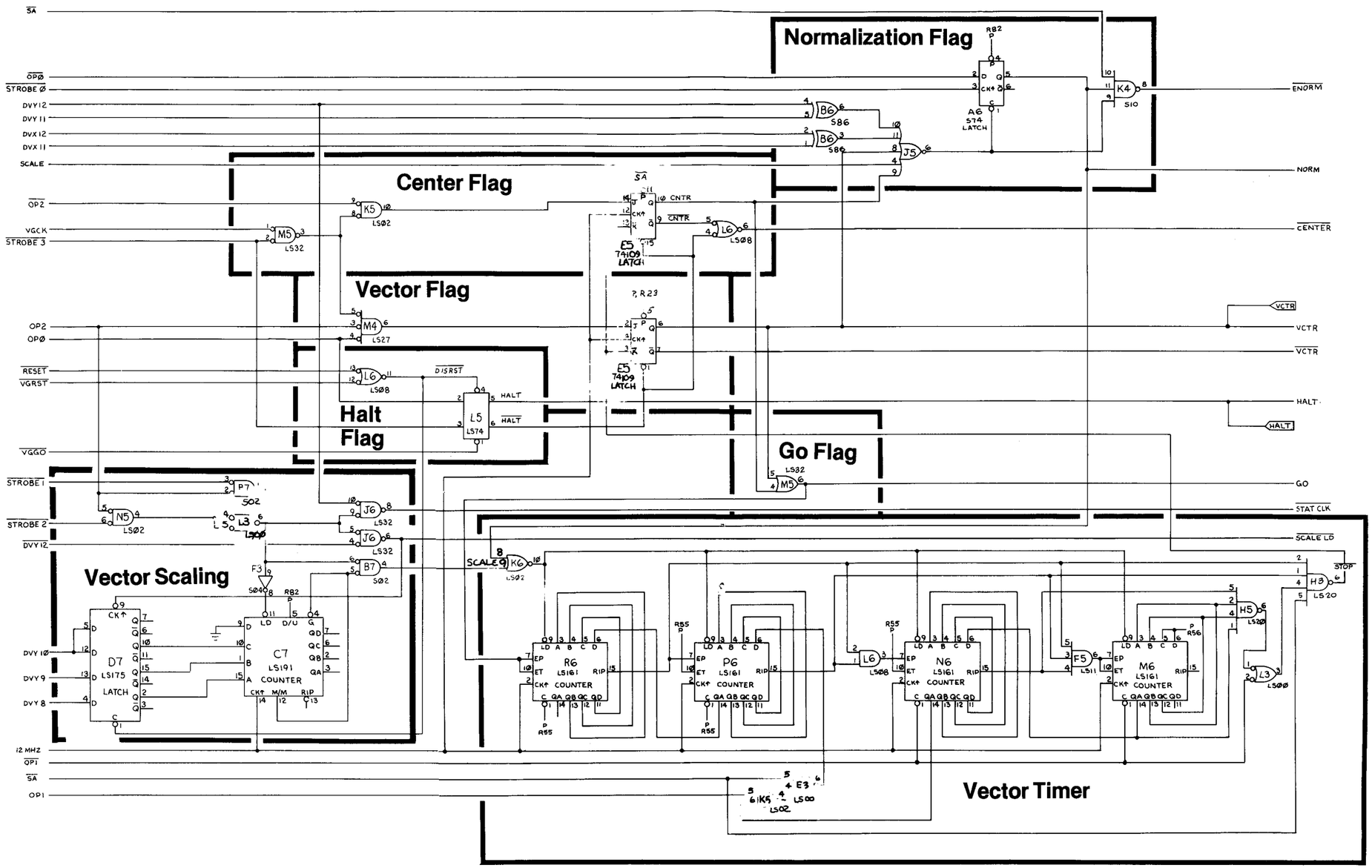
1st printing

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## Black Widow PCB Schematic Diagram



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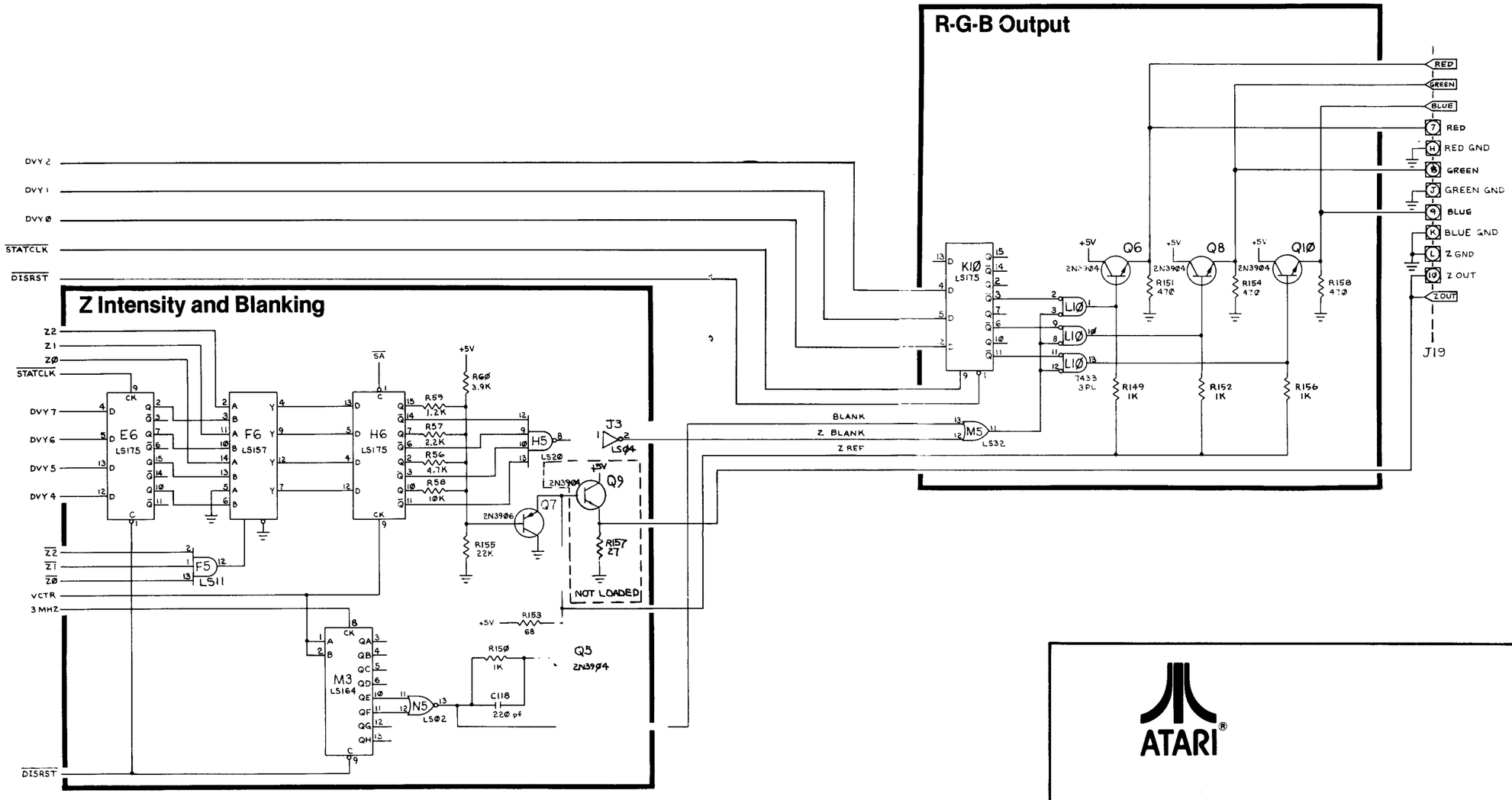
1st printing

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# Black Widow PCB Schematic Diagram



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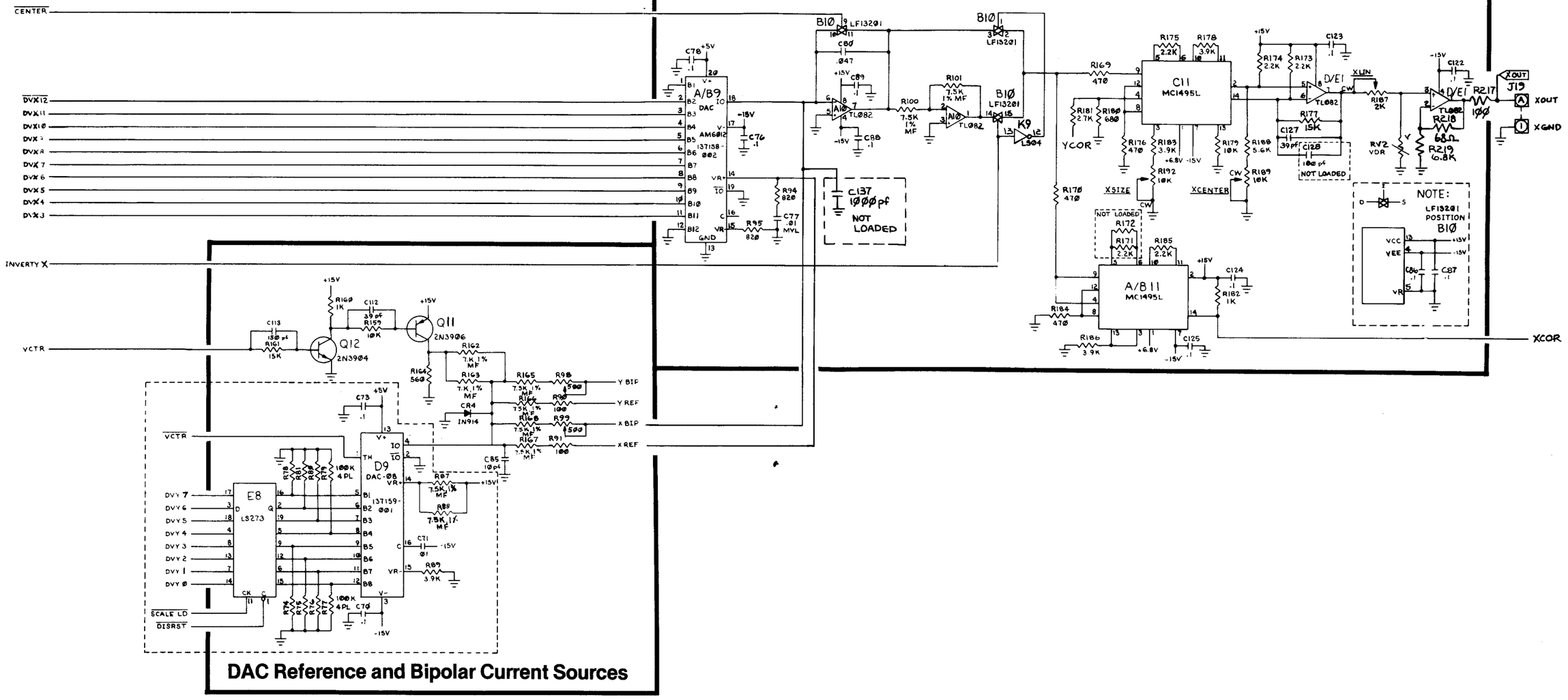
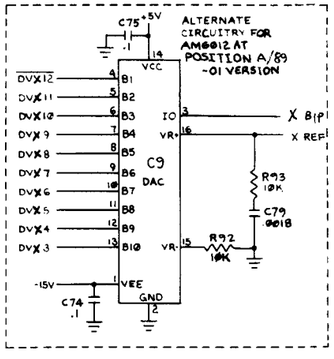
## X-Axis Output




## DAC Reference and Bipolar Current Sources

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**Black Widow PCB Schematic Diagram**



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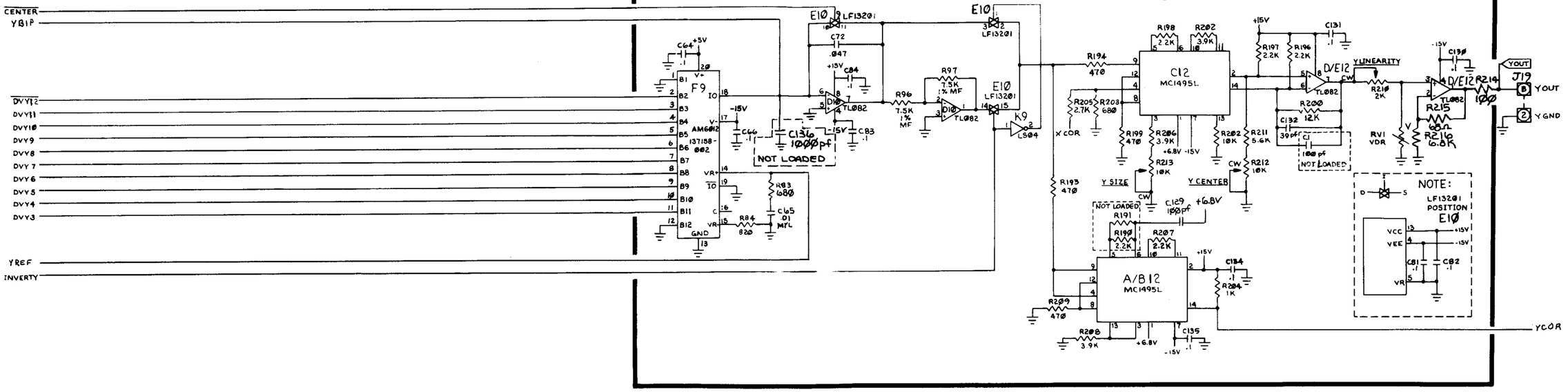
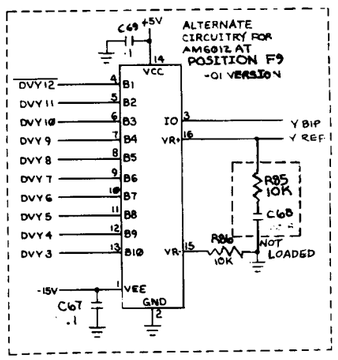
**SP-234 Sheet 10A**
**1st printing**




## Adjusting X- and Y-Axis Video Potentiometers

If you replace the main Gravitar PCB or the display, you may have to make the following adjustments:

1. Enter self-test and advance to diagonal crosshatch pattern (Screen 2).
2. *Centering Pots:* Adjust X CENTER (R189) and Y CENTER (R212) so that the crosshatch pattern is located at the middle of the screen.
3. *Size Pots:* Adjust XSIZE (R192) and YSIZE (R213) so that the crosshatch pattern exactly covers the whole visible screen.
4. *Linearity Pots:* Adjust XLIN (R187) and YLIN (R210) so that the diagonal lines are straight. Since the LIN pots change the size of the displayed picture on the screen, you may have to readjust the SIZE pots in order to get the correct adjustment.
5. *Bipolar Pots:* Advance to the self-test raster pattern (Screen 4). Adjust XBIP (R99) and YBIP (R98) for a 1-inch high horizontal raster in the center of the screen. Be sure the raster ends are square with the sides of the outer rectangle.

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**Black Widow PCB Schematic Diagram**



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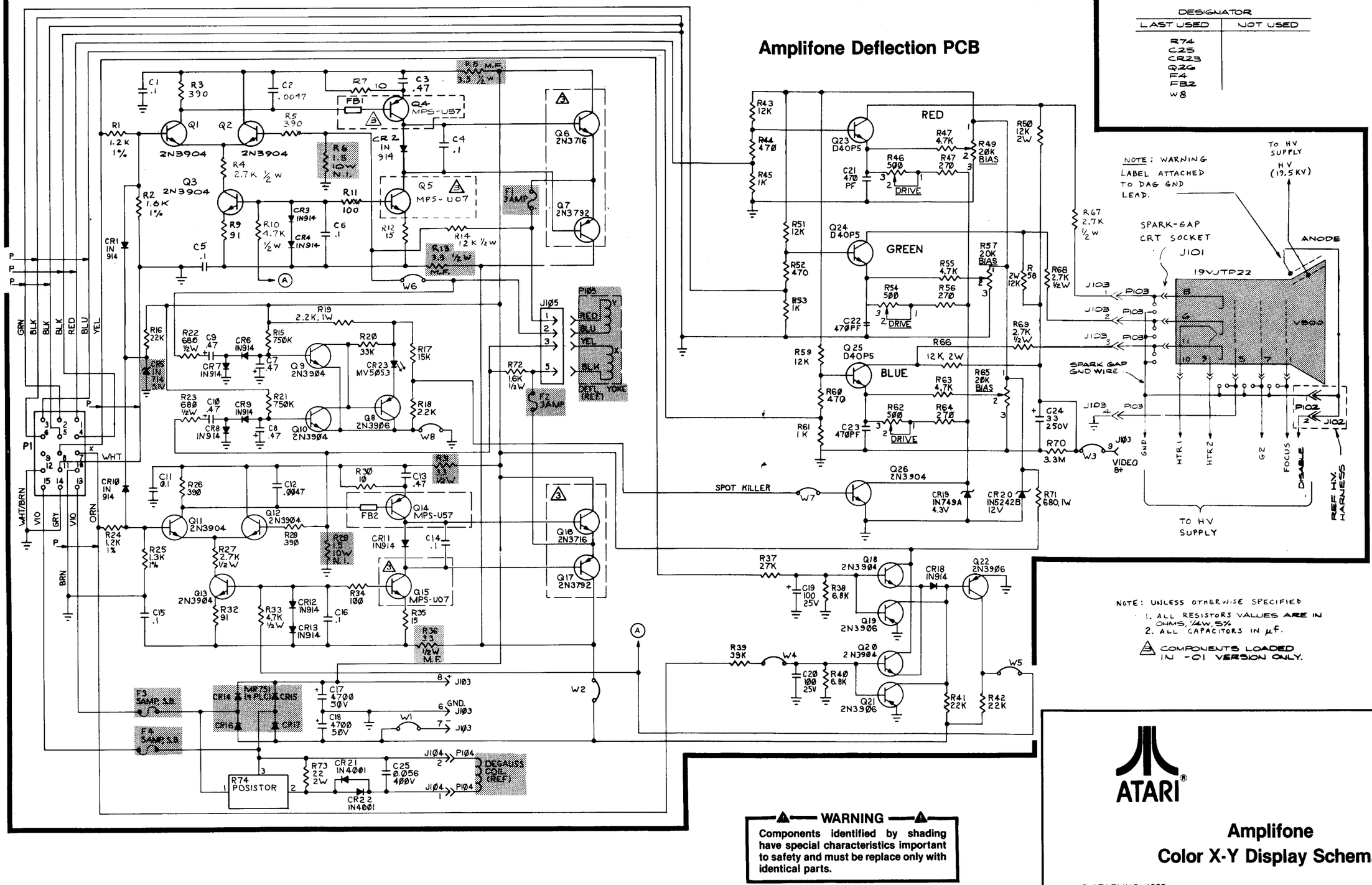
# Amplifone Deflection PCB

| DESIGNATOR | |
|---|---|
| LAST USED | NOT USED |
| R74 | |
| C25 | |
| CR23 | |
| Q26 | |
| F4 | |
| FB2 | |
| W8 | |




NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS VALUES ARE IN OHMS, ¼W, 5%
2. ALL CAPACITORS IN μf.
⚠3 COMPONENTS LOADED IN -01 VERSION ONLY.

**⚠ WARNING ⚠**

**Components identified by shading have special characteristics important to safety and must be replace only with identical parts.**

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# Amplifone
# Color X-Y Display Schematic



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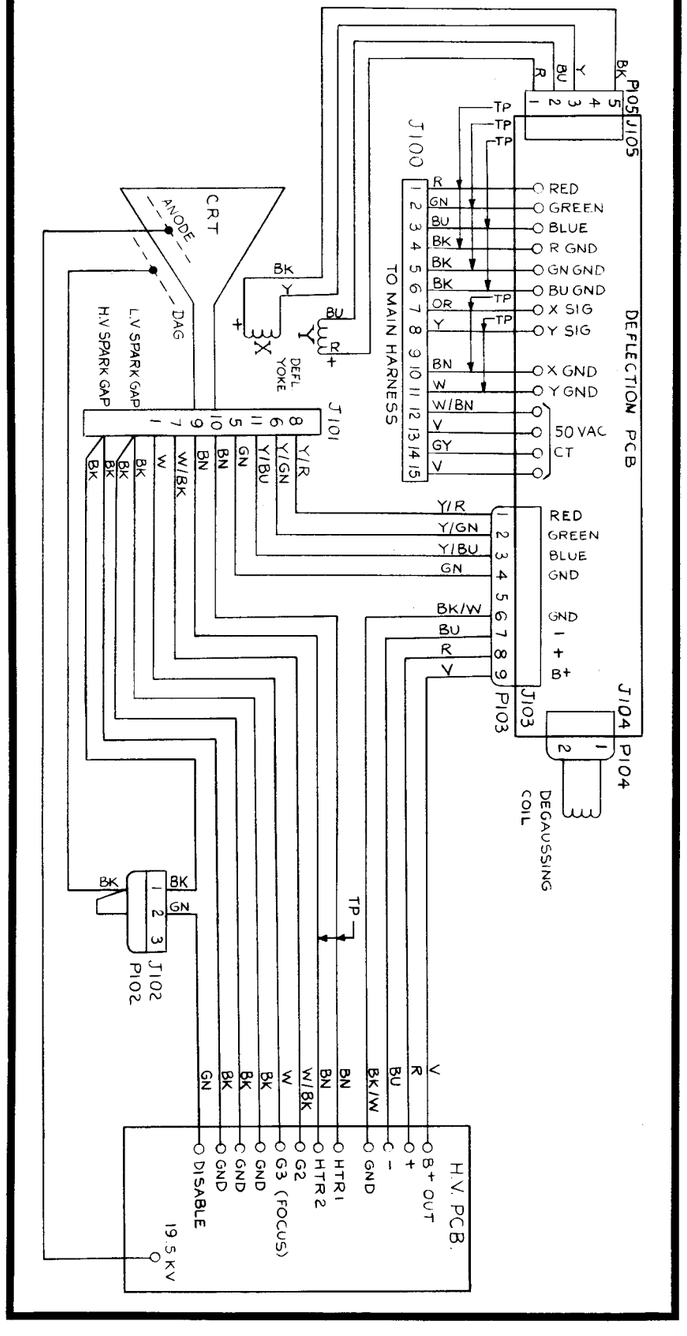
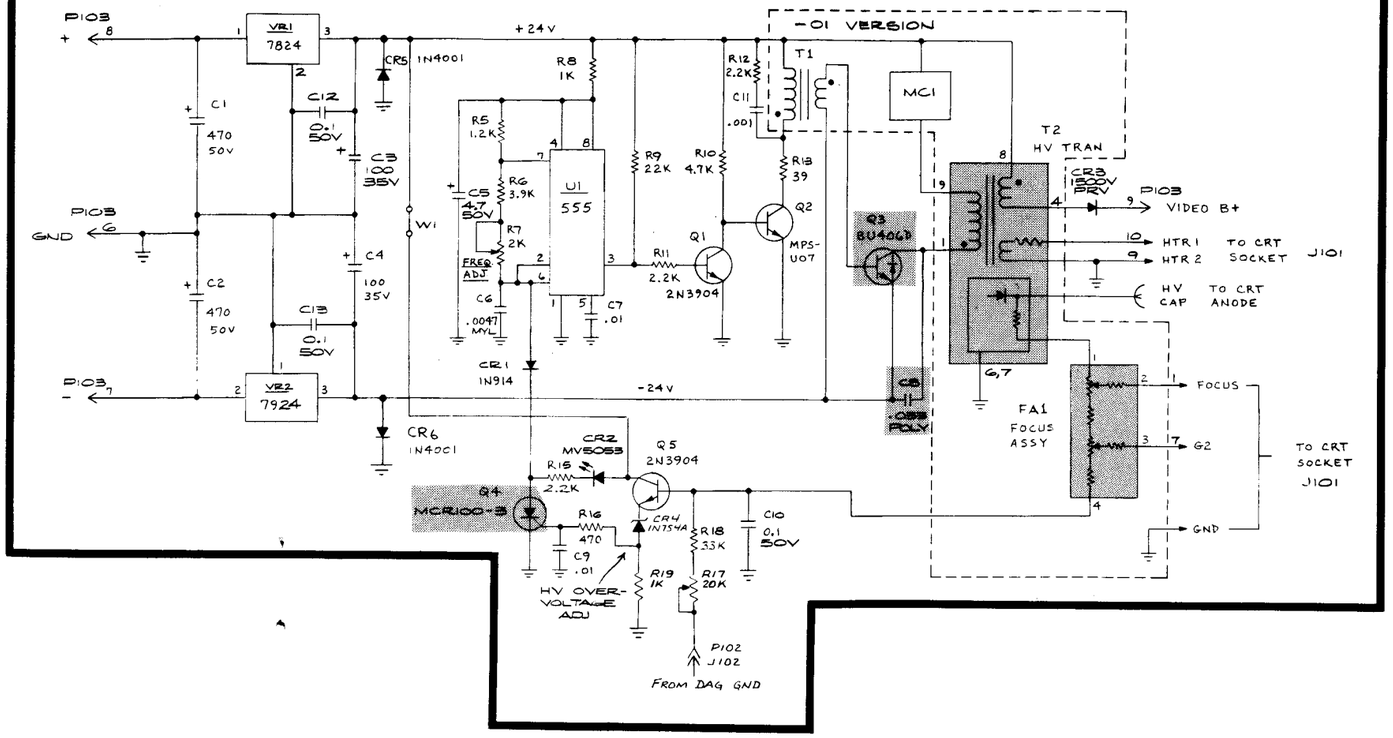
## Amplifone Main Wiring Diagram




## Amplifone High-Voltage PCB




Note: Unless otherwise specified-
1. All resistor values are in ohms, ¼ W, 5%
2. All capacitor values are in μF.

| DESIGNATOR | |
|---|---|
| LAST USED | NOT USED |
| R19 | R1-4, 14 |
| C13 | |
| Q5 | |
| VR2 | |
| T2 | |
| FA1 | |
| J1- | |
| MG1 | |
| CR6 | |
| W1 | |

**WARNING**

**Components identified by shading have special characteristics important to safety and must be replaced only with identical parts.**

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# Amplifone
# Color X-Y Display Schematic



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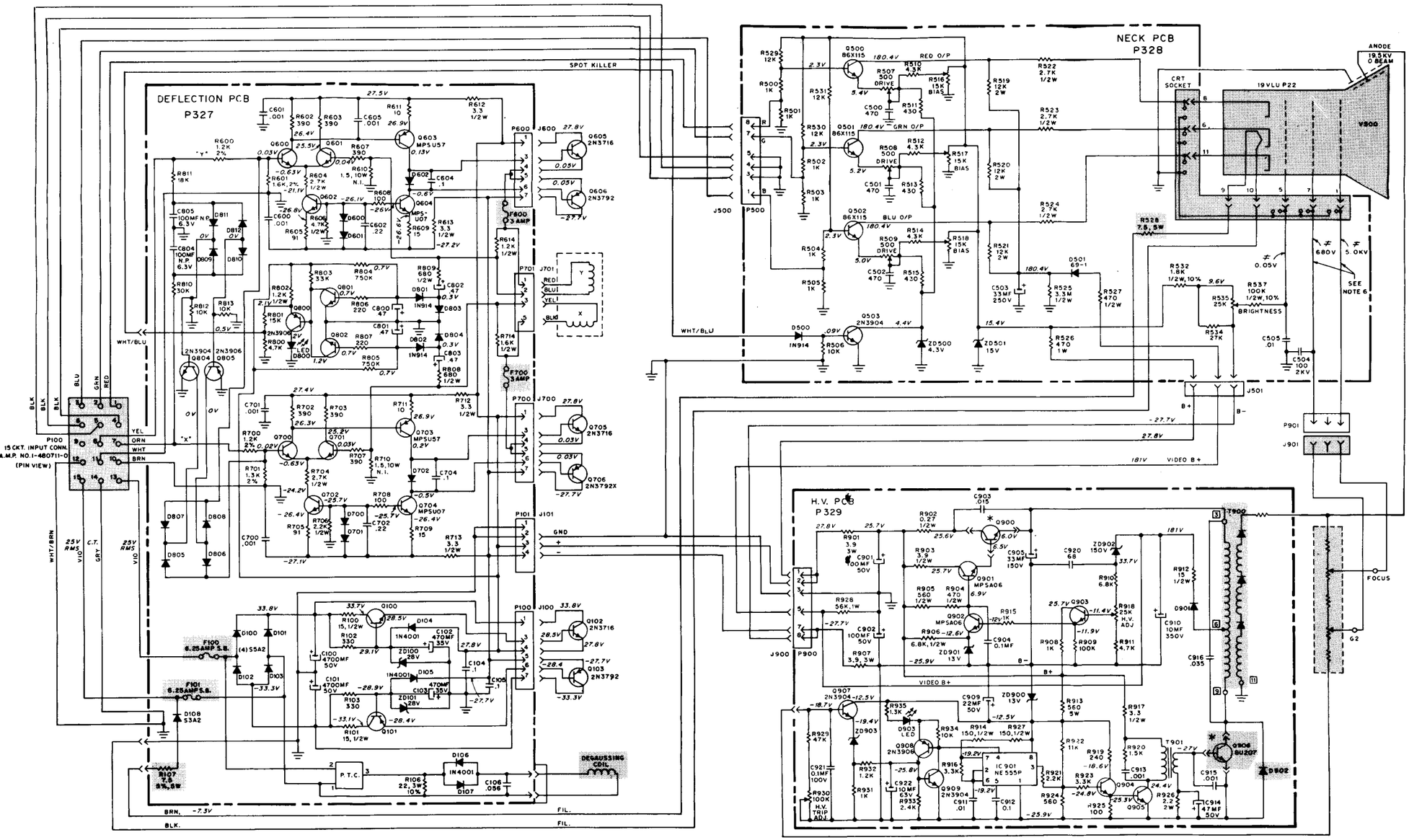


**WARNING**

**Components identified by shading have special characteristics important to safety and should be replaced only with identical types.**

## GENERAL NOTES

1. Resistance values in ohms, ¼ watt, ±5%, unless otherwise noted. K = 1,000, M = 1,000,000
2. Capacitance value of 1 or less is in microFarads, above 1 in picoFarads, unless otherwise noted.
3. *Q900 and Q906 are not in High-Voltage PCB.
4. All D.C. voltages are ±10% measured from point indicated to ground, using a high-impedance meter. Voltages are measured with no signal input and controls are in a normal operating position.
5. Circled numbers indicate location of waveform reading.
6. ZD100-101 uses (66X0040-007) zener diode in series with (340X2331-934) 330-ohm resistor in early production models.
7. Use a 1,000:1 probe when measuring G2 (screen) or focus voltage.

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# Color X-Y Display Schematic Diagram



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